Q-1) [10 pts. 2pt each: 1pt attempt and 1pt for accurate response.]
   a) Driving a 5k load requires a 2-stage amplifier; otherwise the low load resistance will kill the DC gain. NMOS is the best choice. PMOS might just work, but the input common mode needed is pretty close to the edge with $V_{DD}=1.6V$.
   b) NMOS input is the easier choice for common mode swing reasons, but PMOS should work as well. Single stage or two stage is probably best if using an NMOS device to supply the load, due to output swing considerations. Any topology is fine with a PMOS supplying the load (LDO), although it’s easiest to use a single stage and not much gain is required.
   c) Must use an NMOS here – PMOS common mode input won’t work at 1.6V.
   d) Must use an NMOS input folded cascode, as that’s the only one where the input common mode includes the top rail.
   e) Must use a PMOS input folded cascade (and a second stage as we saw later)

Q-2) [35 pts. ai) 5pts. for correct values in the table a.ii) 4pts for each 8 node voltages with -0.5pt penalty for incorrect answer. a.iii) 4pts for correctly filled out table. b) 6pts. 2pts for each with 1pt for eqn and 1pt of correct value for. c) 4pts. 1pt each for input max/min and output max/min. d) 5pts. 1 for $V_{g3,\text{min}}$ and 1 pt each for input max/min and output max/min. e.i) 2pts: 1pt each for $\omega_P$ and $\omega_{ut}$ e.ii) 2pts. 1 pt of PM expression and 1pt for value. e.iii) 3pts. 1pts for each 2 poles and 1 zero.]

For the PMOS-input folded cascode op-amp below, assume the quadratic model with the following specs $\mu_{nCox}=200\mu A/V^2$, $\mu_{pCox}=100\mu A/V^2$, $\lambda=1/(10V)$, $-V_{tp}=Vtn=0.3V$, $C_{ox}=5fF/um^2$, $C'_{ol}=0.5fF/um$.

![Diagram of PMOS-input folded cascode op-amp](image_url)

a) To calculate $V_{ov}$ we first need the bias current carried by each device. Starting from $M_b1$ that carries a reference current of 100$\mu A$, the bias current for all the devices is listed below.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Overdrive voltage ($V_{ov}$)</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_b1$</td>
<td>0.1V</td>
<td>100$\mu A$</td>
</tr>
<tr>
<td>$M_b2$</td>
<td>0.1V</td>
<td>100$\mu A$</td>
</tr>
<tr>
<td>$M_b3$</td>
<td>0.1V</td>
<td>100$\mu A$</td>
</tr>
<tr>
<td>$M_b4$</td>
<td>0.1V</td>
<td>100$\mu A$</td>
</tr>
<tr>
<td>$M_b5$</td>
<td>0.32V</td>
<td>100$\mu A$</td>
</tr>
<tr>
<td>$M_b6$</td>
<td>0.1V</td>
<td>200$\mu A$</td>
</tr>
<tr>
<td>$M_1$</td>
<td>0.1V</td>
<td>100$\mu A$</td>
</tr>
<tr>
<td>Transistor</td>
<td>$g_m$ [mS]</td>
<td>$r_o$ [kΩ]</td>
</tr>
<tr>
<td>------------</td>
<td>------------</td>
<td>------------</td>
</tr>
<tr>
<td>M1</td>
<td>2</td>
<td>100</td>
</tr>
<tr>
<td>M2</td>
<td>4</td>
<td>50</td>
</tr>
<tr>
<td>M3</td>
<td>2</td>
<td>100</td>
</tr>
<tr>
<td>M4</td>
<td>2</td>
<td>100</td>
</tr>
<tr>
<td>M5</td>
<td>2</td>
<td>100</td>
</tr>
</tbody>
</table>

ii. Gate source voltage is given by, $V_{GS} = V_{OV} + V_{TH}$. The resulting bias voltages are annotated in the schematic above.

iii. $g_m = 2I_D/V_{OV}$ and $r_o = 1/\lambda I_D$

\[ g_m = \frac{2}{I_{D}} \]
\[ r_o = \frac{1}{\lambda I_{D}} \]

b) $G_m$, $R_o$ and $A_v$ of the amplifier:

\[ G_m = g_{m1} (g_m \text{ of the input differential pair}) = 2\text{mS} \]
\[ R_o = R_{on} \parallel R_{op} = 6.8\parallel 20 = 5.0\text{MΩ} \]

Here, $R_{op} = g_m r_o^2 = 200\times 100\text{kΩ} = 20\text{MΩ}$ and $R_{on} = g_m r_{o,3} * (r_{o,2}\parallel r_{o,1}) = 200\times 34\text{kΩ} = 6.8\text{MΩ}$.

\[ A_v = G_m \times R_o = 10,000 \text{ V/V} \]

c) Input common-mode range and the output swing are:

\[
\begin{array}{c|c|c}
\text{Input} & \text{Output} \\
\hline
\text{Max} & V_{db} - V_{ov} - V_{gs1} & = 20 - 0.4 - 0.4 = 1.5\text{V} \\
\text{Min} & V_{d1} - V_{tp} & = 0.5 \text{V} \\
\end{array}
\]

\[
\begin{array}{c|c|c}
\text{Input} & \text{Output} \\
\hline
\text{Max} & V_{db} - V_{gs} - V_{ov} & = 20 - 0.4 - 0.1 = 1.5\text{V} \\
\text{Min} & V_{gs} - V_{tn} & = 0.3 \text{V} \\
\end{array}
\]

d) Gate bias for M3:

\[
V_{g3,\text{min}} = V_{g3} + V_{ov} = 0.4 + 0.1 = 0.5\text{V} < 0.62
\]

\[
\begin{array}{c|c|c}
\text{Input} & \text{Output} \\
\hline
\text{Max} & \text{No change} & = 1.5\text{V} \\
\text{Min} & V_{g3} - V_{tn} & = 0.3 \text{V} \\
\end{array}
\]

\[
\begin{array}{c|c|c}
\text{Input} & \text{Output} \\
\hline
\text{Max} & \text{No change} & = 1.5\text{V} \\
\text{Min} & V_{g3} - V_{tn} & = 0.3 \text{V} \\
\end{array}
\]

\[
\begin{array}{c|c|c}
\text{Input} & \text{Output} \\
\hline
\text{Max} & \text{No change} & = 1.5\text{V} \\
\text{Min} & V_{g3} - V_{tn} & = 0.3 \text{V} \\
\end{array}
\]

\[
\begin{array}{c|c|c}
\text{Input} & \text{Output} \\
\hline
\text{Max} & \text{No change} & = 1.5\text{V} \\
\text{Min} & V_{g3} - V_{tn} & = 0.3 \text{V} \\
\end{array}
\]

\[
\begin{array}{c|c|c}
\text{Input} & \text{Output} \\
\hline
\text{Max} & \text{No change} & = 1.5\text{V} \\
\text{Min} & V_{g3} - V_{tn} & = 0.3 \text{V} \\
\end{array}
\]

\[
\begin{array}{c|c|c}
\text{Input} & \text{Output} \\
\hline
\text{Max} & \text{No change} & = 1.5\text{V} \\
\text{Min} & V_{g3} - V_{tn} & = 0.3 \text{V} \\
\end{array}
\]
e) Say the load capacitance $C_L = 1\text{pF}$,

i. Pole and unity gain frequencies:

$$\omega_p = \frac{1}{RO C_L} = 200\text{krad/s}$$

and

$$\omega_u = \frac{g_m}{C_L} = 2\text{Grad/s}$$

ii. Phase Margin: Given the dominant pole above, to calculate the phase margin we should first calculate the non-dominant poles and zero. The two diode connection gives 2 poles and a zero while the cascode contributes 1 non-dominant pole. The respective values are as shown below:

$$\begin{align*}
    C_{gs,15} &= \frac{2}{3} \cdot \text{WL} \cdot \text{Cox} + \text{WCol} \\
    &= \frac{667}{100} = \frac{767}{100} \\
    C_{gs,3} &= \frac{2}{3} \cdot \text{WL} \cdot \text{Cox} + \text{WCol} \\
    &= 3.34 + 50 = 484 \\
\end{align*}$$

Similarly,

$$\begin{align*}
    W_{p,\text{mirror}} &= \frac{g_{m5}}{C_{gs,5}} = 1.3 \text{Grad/sec} \\
    W_{z,\text{mirror}} &= \frac{g_{m5}}{\sqrt{2} \cdot C_{gs,5}} = 1.85 \text{Grad/sec} \\
    W_{p,\text{cascade}} &= \frac{g_{m3}}{C_{gs,3}} = 5.2 \text{Grad/sec} \\
\end{align*}$$

Using these values phase margin can be found as:

$$\begin{align*}
    \theta_m &= 180 - \tan^{-1}\left(\frac{\omega_p}{\omega_u}\right) - 2\tan^{-1}\left(\frac{\omega_u}{W_{p,\text{mirror}}} \right) + \tan^{-1}\left(\frac{\omega_u}{W_{z,\text{mirror}}} \right) - \tan^{-1}\left(\frac{\omega_p}{W_{p,\text{cascade}}} \right) \\
    &= 90 - 89 - 2 \times 60 + 45 - 23 = -8^\circ
\end{align*}$$

iii. Frequencies of the pole/zero doublets from the current mirror: Calculated above
Q-3) [6 pts. a) 2pts for correctly redrawing b) 4pts: 2pts for drawing biasing ckt, 1pt for what gate voltage to bias and 1pt for dimensions and why.]

a) PMOS cascode mirror for low-voltage operation

![PMOS cascode mirror for low-voltage operation](image1)

b) Circuit to generate $V_b$:

Another approach to generate $V_b$ is to use a self-biased cascode as shown below:
Q-4) [5pts: a) 3 pt: 1pt for a chosen approach, 2pt for the expression. b) 2pt: 1pt for identifying negative feedback and 1pt for the argument.]

a) The loop-gain can be derived by breaking the loop at a point where the loading conditions in the loop are unchanged and then finding the ratio of signal that returns.

\[ V_b = V_a \left( \frac{R_2}{R_1+R_2} \right) \]

\[ T = \frac{V_b}{V_T} \]

\[ V_a = -A_V \left( \frac{g_{mp} \left( R_{op} || R_L \right)}{R_{op} || R_L + \left( R_{op} + R_L \right)} \right) V_T \]

\[ \text{PMOS has inverting gain.} \]

\[ T = -A_V \frac{g_{mp} \left( R_{op} || R_L \right)}{R_{op} || R_L + \left( R_{op} + R_L \right)} \frac{R_2}{R_{op} || R_L + \left( R_{op} + R_L \right)} \]

\[ T = \frac{A_V g_{mp} \left( R_{op} || R_L \right) R_2}{\left( R_{op} || R_L + R_{op} + R_L \right)} \]

b) The SENSE value is connected to positive input of the op-amp to provide a net negative feedback. The positive and negative input of the op-amp are with the reference to its own output. As derived above, the PMOS pass-gate device provides an inverting gain. Thus, the op-amp provides \(+A_V\) (because the of SENSE signal connected to its +ve terminal) and PMOS provide \(-g_{mp}R_{eff}\) resulting in overall negative feedback.

Q-5) [8pts: a) 2pts: 1pt gain expression and 1pt for the ratios b) 2pts: 1pt for the expression of gain error and 1pt for finding worst case gain c) 2pts: 1pt for the expression and 1pt for calculating A0 d) 2pts: 1pt for the expression and 1pt for calculating bandwidth]

The schematic is shown on pg-562 of Razavi’s book, 2\textsuperscript{nd} Ed.
a) Close loop gain, \( A_v = C1/C2 \). If we choose \( C2 = Co \) then for gain of 1 to 8 \( C1 \), respectively, should be \( Co, 2Co, 3Co, 4Co \ldots 8Co \).

b) The gain error is given by, 
\[
\varepsilon = -\frac{1}{A_0f}
\]
where the feedback factor \( f \) is related to \( A_v \) by \( f = 1/(A_v+1) \). Thus \( \varepsilon \) is maximum when \( A_0f \) is the smallest, which happens for smallest \( f \) and thus, highest \( A_v=8 \).

c) Assuming \( C_P = 0 \), the gain accuracy of 0.4% translates to \( \varepsilon = 0.004 \). For \( f = 9 \), the minimum DC gain required to achieve the 0.4% accuracy is, \( A_0 \geq 2250 \).

d) Settling time \( t_s \) and error \( \varepsilon \), are related by, 
\[
t_s = \tau \ln(1/\varepsilon)
\]
Thus, for \( \varepsilon = 0.004 \) and \( t_s = 10\mu s \), the required time constant \( \tau = 10\mu s/5.52 = 1.8\mu s \). Now, unity gain bandwidth \( \omega_u = A_v/\tau = 4.4\text{Mrad/sec} \).

Q-6) [2pts: a) 1 pt for bottom rail argument, b) 1pt for correct V+ swing]

a) The top plate voltage of the capacitor DAC is \( V_x \), as we analyzed in the class. Then it is obvious from the figure that the comparator compares the \( V_x \) (V+) node to ground, which is connected on V- terminal of the comparator.

b) Very similar to the analysis done in the class where the \( V_x \) comparison was made to \( V_{REF} (=V_{DDA}) \), here the comparison is made with ground. Hence, for large values of \( V_{in} (>V_{REF}/2) \) the node \( V_x \) would swing below ground potential. Thus, the voltage on the input of the comparator do not stay within the rails.
Grading rubric:

First, please identify whether you belong to EE140/240a.

Rubric for EE140:
Max. points: 66

Q-1) Total: 10pts
   a) 2 b) 2 c) 2 d) 2 e) 2

Q-2) Total: 35pts
   a.i) 5 a.ii) 4 a.iii) 4 b) 6 c) 4 d) 5 e.i) 2 e.ii) 2 e.iii) 3

Q-3) Total: 6pts
   a) 2 b) 4

Q-4) Total: 5pts
   a) 3 b) 2

Q-5) Total: 8pts
   a) 2 b) 2 c) 2 d) 2

Q-6) Total: 2pts
   a) 1 b) 1

Rubric for EE240a:
Max. points: 72

Q-7) Total: 6pts
   a) 2pts b) 4pts

Grading guidelines:

1) It important to get the approach right. You should grade a right approach at 60% for grade.
E.g. 3/5

2) Next, important point is to get right numerical answer. Full grade is reserved for this purpose.
3) Numerical error should cost you 20%
   E.g. 1 numerical error in a 5pt problem is 4/5
4) If approach is correct and problem has multiple numerical error, you at least get 60%
   E.g. 3 numerical error in a 5pt problem is 3/5
5) If the error propagate, you should be penalized only once.
   E.g. Say you have error in value of gm then only that part gets penalized as per 3). Later if you
   are required to calculate gain, \( Av = -\text{gm} \)ro and \( \text{UGB} = \text{gm}/\text{Cc} \), these values would also be wrong
   but should not be penalized