EE140: Lab 3 Part 2

2 stage bipolar op-amp

Due: Mar 13, 2018 (9 am)

Instruction

For this lab, you may consult the professor, the TAs, your friends, the textbook, the internet, and any other living or inanimate objects, with the exception of your peers' lab reports. You may obtain data in pairs, but must **submit your own written report**. Be concise. Hand calculations should be to 1 or at most 2 digits of precision. Don't use a calculator – I won't let you use one on the exam and it's good to get in practice.

Objective

This lab is meant to familiarize you with 2-stage op-amps, and in particular unity-gain feedback.

SPICE model parameters. You can see the parameters that LTSPICE uses by right clicking on an element and selecting "Choose new device". The parameters that you need for your hand analysis are:
2N3904 NPN (VAF=100 Bf=300 CJC=4p CJE=8p)
2N3906 PNP (VAF=100 Bf=200 CJC=5p CJE=10p)

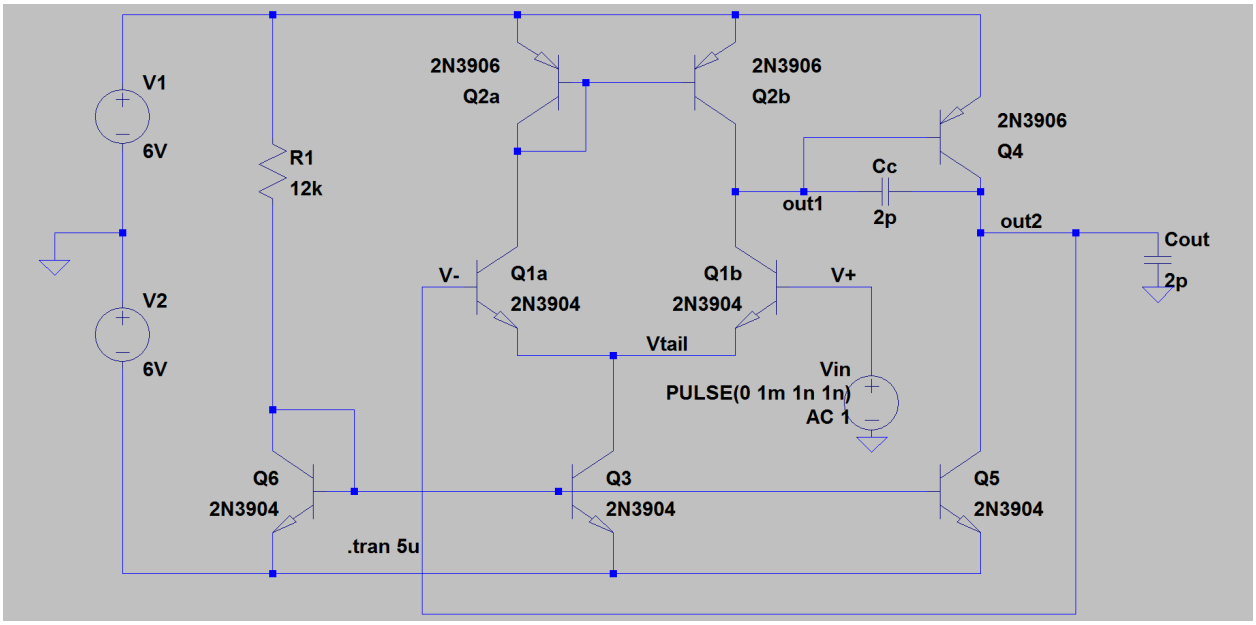

Figure 1 The op-amp in unity gain feedback. Capacitors Cc and Cout represent typical parasitics for a breadboard.

1. Use LTspice on the file BJTopampUnityFB.asc to simulate the amplifier in unity gain feedback, as shown in Figure 1. This amplifier is unstable in unity-gain feedback.
   a. [Writeup] The input is a 1mV step. What should the output be?
   b. Use the cursor tool to measure the frequency of the fully-developed oscillation (where the amplitude is roughly 300mV peak-to-peak).
   c. Use the cursors to measure the period of the first several oscillations (when the amplitude grows from 0 to ~200mV peak-to-peak).
   d. [Writeup] How does the frequency of oscillation change as the amplitude of the oscillation increases?
   e. Use the cursors to measure the amplitude of each half cycle (peak-to-trough, trough-to-peak) of the oscillation during the first several oscillations. Plot using excel or other tool. You should see an exponential growth.
   f. [Writeup] Estimate the location of the complex conjugate poles of the closed-loop amplifier, and how they move as the output rings up.

2. Still using LTspice on the file BJTopampUnityFB.asc, we now want to stabilize the amplifier by moving the poles around.
   a. Increase Cout to 1000pF. Measure the negative slew rate in simulation. Look at the current in Q4 and Q5 during the beginning of oscillation (first hundred ns), and after the oscillation is fully developed.
   b. [Writeup] Estimate the negative slew rate assuming Q4 is off. What is the amplifier doing that allows the positive-going rate of change to be so much larger than the negative?
   c. Increase Cout to 20,000pF=20nF. Estimate the closed-loop pole locations. Is the amplifier settling to the right value? What is the rise time (time to get to 95% of the final value)? What is the settling time (time to get within 5% of the final value, and **stay** within 5%)?
   d. Increase Cout to 200,000pF=200nF. Estimate the closed-loop pole locations, rise time, settling time.
   e. Increase Cout to 1,000,000pF=1uF. Try again with 2uF and 5uF. At what capacitor value does the system start to look like a single-pole system?
   f. [Writeup] Compare estimated pole locations, rise time and settling time for the different capacitor values. Thinking qualitatively about the different responses, if you were designing a toy to move a mouse to entertain your cat, which type of response would you choose? If you were designing a control system for a robot dental drill, which would you choose?

https://en.wikipedia.org/wiki/Settling_time
https://en.wikipedia.org/wiki/Rise_time

Now set **Cout back to 2pF**, and we'll try using Cc instead.

   g. Set Cc=100pF. Estimate the closed-loop pole locations, rise time, settling time.
   h. Set Cc=600pF. Estimate the closed-loop pole locations, rise time, settling time.
   i. With Cc=600pF, look at the first 50ns of the response, with V+ plotted as well. The first 1ns of rise in Vout is largely due to capacitive coupling. The decrease over the next 5ns is due to the right-half-plane zero (zero means derivative of

input, RHP means negative sign on the output impact) due to Cc. Choose a resistance in series with Cc that has the same conductance as the transconductance of Q4. Does it help? Set this resistor to 0 for the rest of the problem.

j. [Writeup] Compare the size of the capacitor needed to stabilize the amplifier, and the resulting settling times.
k. Change the input step to be 1000mV instead of 1mV. What is the slew rate? Plot the collector currents in Q1AB and Q2AB, and Q4 & Q5.
l. Change the input step to be -1000mV. What is the slew rate? Plot the same currents.
m. [Writeup] Redraw the circuit once for positive and once for negative slewing, drawing only those transistors carrying current. Label the collector currents (in mA), and the current in Cc. Compare the simulated slew rates to hand calculated slew rates, and in each case explain why each transistor is carrying the current it does.
n. **Set Cc=2pF**, and add a capacitor C_1 from out1 to ground. What value of C_1 is needed make the amplifier stable in unity gain feedback? What happens if you increase C_2 a lot with that value of C_1?

Lab

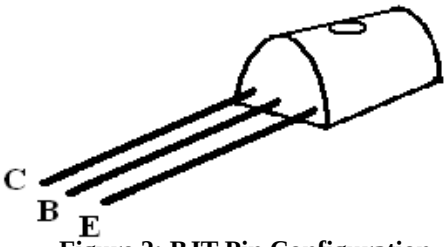

Figure 2: BJT Pin Configuration

1. Measurements
   a. Put the amplifier in unity-gain feedback, and drive the input with a small square wave at low frequency. Watch it ring. Take an oscilloscope screen capture.
   b. Add capacitance at the output. Can you replicate the behaviors that you saw in the simulation (saw tooth, stable but ringing, stable and no overshoot)? What is the best settling time you can get? Measure the negative slew rate. Take a screen capture of each behavior, and note the corresponding capacitance.
   c. Remove the capacitance at the output, and add capacitance across the second stage (C_c). Can you replicate the behaviors that you saw in the simulation (stable but ringing, stable and no overshoot)? What is the best settling time you can get? Take a screenshot of each behavior, and note the corresponding capacitance. Measure positive and negative slew rates.
   d. [Writeup] Compare the amount of capacitance used at Cout and Cc, and its effect on the closed-loop step response.