

EE140: Lab 4, Project Week 1

PVT-Insensitive Biasing

version 1.7; Due: Mar 23, 2018 (late 9am Sat 3/25)

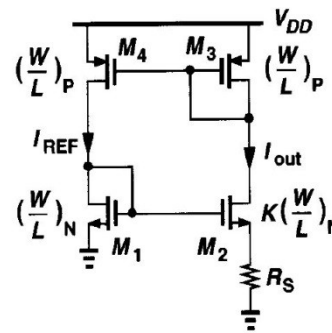
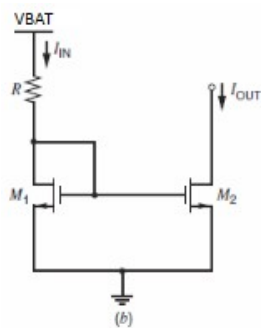
Introduction

For this lab, you will be developing the background and circuits that you will need to get your final project to work. This lab is to be done individually. The report will be in the format of a PowerPoint presentation which addresses the deliverables at the end of this document. The members of each project group will present their results to one another and grade each other's presentation. This is your opportunity to help each other make your final project presentation the best it can be.

Objective

The goal is to design and simulate several reference circuits and compare their performance. In each case, you will vary the supply voltage V_{BAT} from 0.8V to 1.6V (corresponding to an alkaline batteries), and vary the temperature from -40 to +85 Centigrade (the typical industrial temperature specification). For this lab we won't be exploring process variation.

Current References



(Left) Resistor-Biased Current Mirror

(Right) g_m reference (Figure 12.3 from Razavi 2nd edition, or 11.3 from the 1st edition)

The simple resistor-biased current mirror is included as a reference to see how bad things can be. The V_t referenced source is a step in the right direction, and is good enough for some applications. Design both circuits to have a nominal output current I_{OUT} of 10 μ A.

- Plot the output current and gate bias voltage on M1 in both circuits vs. temperature and battery voltage. You can set up a DC sweep for temperature and use Parametric Analysis to vary battery voltage from 0.8V to 1.6V in steps of 200mV.
- Tabulate the worst-case variation.

Bandgap Reference

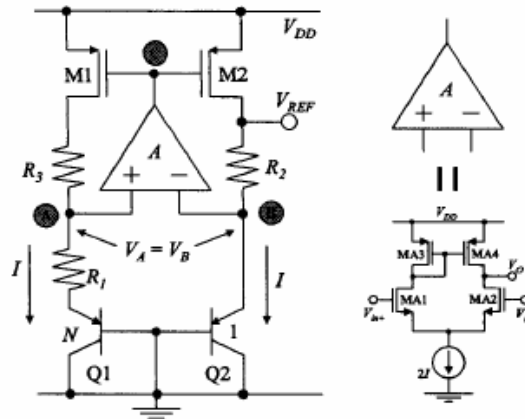


Fig. 6: A CMOS bandgap voltage reference using error-amplifier-based current mirror.

Mok, Philip KT, and Ka Nang Leung. "Design considerations of recent advanced low-voltage low-temperature-coefficient CMOS bandgap voltage reference." Custom Integrated Circuits Conference, 2004. Proceedings of the IEEE 2004. IEEE, 2004. [http://web.mit.edu/Magic/Public/papers/IEEEXplore\(14\).pdf](http://web.mit.edu/Magic/Public/papers/IEEEXplore(14).pdf)

Now you will design the bandgap circuit shown above to generate $V_{REF} = 1.2V$.

- We will set $R_3 = R_2$.
- Your op-amp may be a simple differential pair or a two stage opamp. It needs to run off of V_{BAT} because at this point you don't have any other voltages to work from.
- The bipolar PNP transistors are actually diodes. Use "pdio" from the gpdk45 toolkit. Make Q1 and Q2 the same dimensions and then use the "multiplier" field to put copies of each in parallel. The ratio of the size of Q1 to Q2 should be a rational number.
- The resistors should have a temperature coefficient. You can start with analogLib resistors, but you must replace them with "ressnpoly" (N+ poly resistor without salicide) resistors from the gpdk45 toolkit. Choose the same segment width and length for the resistors and adjust the number of segments to get the desired resistance value.
- Show that the current in both branches is:

$$I = \frac{\Delta V_{BE}}{R_1}$$

- Write an expression for V_{REF} in terms of ΔV_{BE} , V_{BE} , R_1 and R_2 .
- Now rewrite your expression for V_{REF} in terms of I_s , V_{BE} , V_t , R_1 , R_2 , and n .
- Choose values for n and for the ratio of R_2/R_1 to get close to a zero temperature coefficient. Use only rational numbers for n and the R_2/R_1 ratio. (We do this so that we make the resistors and capacitors match very well during layout by constructing them from unit elements).
- Choose a starting size for Q2. We will iterate and adjust this later.

- Calculate what V_{BE2} should be in order to generate $V_{REF} = 1.2V$ given your previous choices.
 - Simulate a copy of the Q2 diode to find out how much current is required to give the value of V_{BE2} you calculated.
 - Calculate the size of R2 now that you know the current through it and voltages across it.
 - Calculate the size of R1 using the ratio you picked earlier. Note that we have a tradeoff here between the size of the resistors and the bias current through the diodes. If your resistors are extremely large (many mega-ohms) you can adjust your diode size and recalculate.
 - Size the PMOS transistors to deliver the calculated current with an overdrive of a few hundred millivolts.
 - Now that you have finished sizing all the components, you can return to your choices made earlier and adjust if necessary.
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- Set a value for V_{BAT} and run a DC simulation sweeping the temperature from $-40C$ to $+85C$. Plot V_{REF} .
 - Ideally the output should look parabolic with a slope of zero near $25C$. You will likely need to make adjustments.
 - If you need to make adjustments, think about what the slope of your output is telling you. You likely have too much of either the positive temp coefficient or the negative one. Make adjustments to your circuit to balance these opposing temp coefficients so they add up to zero near $25C$.
 - Once you have a relatively flat temperature response, re-run the simulation varying V_{BAT} from $0.8V$ to $1.6V$ in steps of $200mV$.

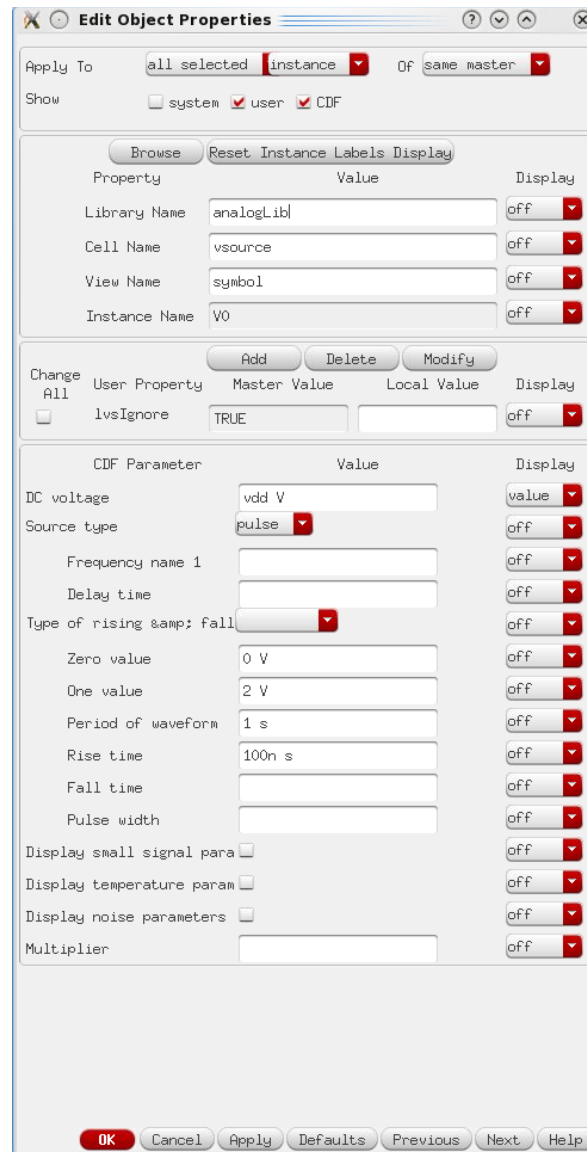
Bandgap Startup and Stability

- Thus far we have only checked our bandgap with DC simulations. It is important to make sure that when power is first applied the circuit begins to properly operate and that it is stable.
- We can test this by using a "vsource" from analogLib for VBAT to create a voltage ramp from $0V$ to $2V$. Set your vsource up as shown below and then run a transient simulation.
- Your circuit should properly startup and settle to V_{REF} . If it does not (ie it starts oscillating) add compensation capacitance to stabilize it.
- How long does your circuit take to start up?

Deliverables

- Your final schematics should have no analogLib components.
- Schematic of simple current mirror with sizes annotated.
- Schematic of V_t referenced current source with sizes annotated.
- Plots of output current and gate bias voltage vs. temperature and battery voltage for simple current mirror.
- Plots of output current and gate bias voltage vs. temperature and battery voltage for V_t referenced current source.

- Schematic of bandgap reference with sizes annotated (including opamp schematic). Plot of V_{REF} vs. temperature (-40C to +85C) for battery voltage from 0.8V to 1.6V in steps of 200mV.



- Schematic of bandgap-based current reference with sizes annotated (including opamp schematic).
- Plots of output current vs. temperature and battery voltage for bandgap-based current reference.
- Table comparing worst case variations of reference currents for all three circuits (1. Simple current mirror 2. V_t reference 3. Bandgap reference). Give the max and min deviation for each reference and note at what temp/ V_{BAT} it occurs.
- Plot of transient bandgap showing stable startup.

A Note on Plots in Cadence

- The default plotting options in Cadence are garbage for presentations.
- The pro-level thing to do is export the data and plot with MATLAB, Excel, etc.
- Cadence plots are only acceptable for submission if at a minimum the following steps have been performed:
 - Graph > Properties > Set background to white > OK
 - Graph > Properties > Graph Options > Font > Fixed [Sony] > Size 18
 - Right click on traces > Width > Extra Thick
- Even with these adjustments, the plots are still not great for presentation. You can experiment with other settings, but they will never look as good as if you had exported.

A Note on Schematics in Cadence

- Like with default plots, schematics in Cadence are poor.
- Drawing your circuits neatly goes a long way in making them understandable.
- If you want really nice schematics, use Adobe Illustrator.
- Otherwise to get decent schematics from Cadence, follow these steps:
- File > Export Image
 - > Background > White
 - > Foreground > Black
 - Bi-color
 - Selected Area > Select > Draw a box around your circuit (It is not click'n'drag)
 - Choose a name, then Save to File
- Annotate sizes and nodes onto schematics by adding labels in post-processing.