Debussing
- Project
- Present results
- Test barriers
- Regulators

Integration
- Ideal module done ASAP
- VCVS op-amps, comparator
- Start integration

Presenting results
- Bandgap works
- ADC doesn't work

 debugging
- DC voltages
- DC currents
- Gain, Ra values
- Run DC sweeps
- Be careful of high gain amplifiers

\[ V_{out} = V_{in} \quad \frac{1}{V_{ref}} > V_o \]

If \( A_v = 10^4 \) what is the width of the useful input voltage range?

\[ V_{BG} = 0.8V \]

\[ V_{MIN} \]
test harness

Regulator
- Most circuits like to run at a fixed voltage
- Battery varies a lot
- Use a voltage regulator

Old days:

Today: reference voltage + op-amp + transistor

Low drop out regulator (LDO)

Bash case, need $V_s > V_{reg} + V_{BE}$
(probable worse w/ op-amp swing)

30mV overhead or "drop out"
2.6mA = 2660 μA
10 mV
DC

Stability
1) op-amp very slow
2) op-amp fast, dominant pole at output

PMOS gate tracks average current

Lots of gates switch on rising edge of CLK
Leakage plus lots of spikes during:

\[ Q = 4 \cdot 16 \cdot 10^3 \text{pC} = 64 \text{pC} \]

\[ I = 1 \text{mA} + 0.1 \text{mA} = 1.1 \text{mA} \]

\[ V_{reg} < V_{ref} \]

\[ V_{reg} > V_{ref} \]