Project

FINAL DESIGN due < 2 weeks (9 AM Monday 4/30)
all cadence files to enable testing

File presentation in RRR week: upload before presn.
2nd presn to me next week: sign up

Wafer sort - acceptance testing
binning based on performance
14%? trim y/OTP
= die cost? BEST - memories

LTC 1968 - 4 op-amps, comparator, switches D to 10 diskeys in 1000s

during p

\[ f = \frac{C_2}{\frac{1}{\zeta} + C_L + C_{in}} \]

even if \( C_{in} = 0 \) \( f \neq \frac{1}{\text{gain}} \)

\[ C = 8 \implies f = \frac{C_2}{8C_L + C_L} = \frac{1}{9} \]

if \( C_{in} \approx C_L \implies f = \frac{1}{10} \)

small effect on both time constant and precision

PGA Issues

Gain = 8, \( f = ? \) \( 1/8 ? \) no.

\[ V_o = \frac{C_L}{C_2} \]

\[ V_{in} = \frac{1}{1 + Af} \]

\[ V_{out} = \frac{C_1}{C_2} \left( \frac{1}{1 + Af} \right) \text{ eqn 13.52} \]

time constant

\[ T = \frac{1}{fG_m} \left( C_L + f(C_L + C_{in}) \right) \text{ eqn 13.59} \]

High freq.: \[ V_o = \frac{1}{G_m} \]

\[ V = fV_{in} \]

\[ \frac{1}{fG_m} \]

Fig 13.52
SWAP V+ -

Pull to ground

$V_{in} = -V_{in} = V_{Cin}$

Ideally: input offset, finite gain

There's input offset on Q-

$Q_1$.

Connect 1st stage output to NMOS or PMOS?

Connect NMOS or PMOS?

If FC has a gain of 1000, then $V_{out} = 1 mV$

Will the output of the FC 1st stage:

If CMOS may work too, but Si CMOS has

pull Vp down

probably doesn't work.

If $V_{out} = V_{LSB}$

connect PMOS

lead to self latch

store output:

$V_{out} = 2 V_{LSB}$