Regulators:

- DREG: 2 dominant poles at Vreg.
- DAC-REG: Don't know capacitance 100nA current - do we need a 2nd stage?

If DREG tracks I_{DD} perfectly (V_{DD} has no ripple) then how much ripple on V_x?

\[ AV_x = (15)(4mA) = 4mV \]

Problem? Maybe.

Consider:

- \( A_{G \rightarrow D} = -9mV_R \)
- \( A_{S \rightarrow D} = +9mV_R \)

4mV ripple @ 10MHz

If \( V_c \) is constant, could be a big ripple on V_{REG}. Can be trouble for 3rd gap as well.

Power Supply Rejection Ratio:

Charge injection:

\[ Q_{channel} = (V_{DO} - V_{TN})COX \]

Fast falling edge of clock: assume charge splits

\[ \frac{1}{2}Q_c \]

Slow clock:

\[ Q = COX V_{TN} \]

\[ \frac{1}{2} \]

No charge when \( V_c = V_{TN} \) switch is now off.
say $C_{OE} = 1\, \mu F/mm$, $W = 1\, \mu m \Rightarrow C_{OE} = 1\, \mu F$

\[ Q_- = -V_{in} C_1 + V_{in} C_{OE} \]

but now $+V_{DDA}$ $C_{OE}$

slow clock $\Rightarrow$

when $V_6 = V_{tn}$

\[ Q_- = -V_{in} C_1 + V_{tn} C_{OE} \]

\[ V_o = \frac{-Q_-}{C_{OE}} = \frac{C_1}{C_{OE}} \cdot V_{in} - \frac{C_{OE}}{C_{OE}} \cdot V_{tn} \]

so make switches as small as possible

use big enough $C_2$

note that both of these make discharge of $C_2$, $V_-$ slower - there are limits

What about the other switches? $S_2$

\[ V_{in} \rightarrow S_2 \rightarrow C_1 \]

\[ V_{in} \rightarrow S_1 \rightarrow \frac{1}{3} \cdot \frac{1}{2} \rightarrow \frac{1}{3} \]

charge injection at $S_2$ is irrelevant on P6A

sub on ADC? with $S_3$ after $S_4$

on $S_1$, only a problem if it closes turns off before $S_2$
Strong ARM
for computers, can use op-amp + inverter or
strong ARM clocked comparators
- faster
- lower power

Core elements:
- cross-coupled inverter latch
  - positive feedback
  - bistable - poles in RHP real
  - memory element in SRAM

\[ r = \frac{1}{\tau} = \frac{C_L}{g_m} \]

Phase 1

Phase 2

Phase 3

Phase 4