CMOS version
input resistance

Conceptually OK, bad in practice

Even better: measure input current and subtract it out

CMOS version - 2 stage (workhorse)

Initially

Typically no output stage

diff pair \( 1AB \)
active load \( 2AB \)
gain stage 4.5
bias network 3.5 6
signal path 1, 2, 4

differential gain
common mode gain
input offset
input common mode range
output swing
frequency response
power supply rejection
noise
current drive
slow rate

current mirrors

\[
\text{if } A \text{ and } B \text{ have}
\quad \text{same } W, L, V_T, M_{\text{Cox}}
\text{ and } z = 0 \text{ how diffrd can the current be?}
\text{if both are in saturation?}
\]

A: not at all dffrd
What if \( z \neq 0 \)?

\[
\frac{\Delta I_D}{\Delta V} = \frac{\Delta V}{V} D
\]

\[
I_D = \frac{\Delta V}{V}
\]
How do you set a gain of, say, 100 ± 1%?

Gain so that $V_o = 100$

4x these models are terrible

Output resistance varies $V_o$

Everything varies with Temp, Process, and Supply voltage

EE128 view

not possible

$\frac{-10v}{-15v}$

Resistor & capacitor

$R = 9.9k$

$K = 1k$

Resistor & capacitor

$V = 100V$

but how accurate?

How much gain do we need to add 0.1% accuracy?