DETAILED COURSE SYLLABUS *(TENTATIVE)*

The following comprises a **tentative** syllabus describing the material to be covered in this course. Material to be covered for each dated lecture is indicated along with the corresponding sections of the required and recommended textbooks, where GM = Gray & Meyer's "Analysis and Design of Analog Integrated Circuits" (i.e., the required text), and R = Razavi's "Design of Analog CMOS Integrated Circuits" (i.e., the recommended text). How much of this material we can actually cover is a function of the degree of preparation of the average student in the class, which can vary depending upon which versions of EE 105 were taken.

Date		**Material to be Covered**	**HWs**	**Labs**
Aug.	27	Administrative Information, Introduction/Overview: Op Amps		
Sept.	1	Dev. Operation & Models: BJT & MOS; G&M: §1.1-1.6, R: Chpt. 2		No Lab
	3	Dev. Operation & Models, Inspection Analysis; G&M: §1.1-1.6, R: Chpt. 2		
	8	Bipolar Inspection Analysis; G&M: §3.1-3.3, R: §3.1-3.4, §6.1-6.4	HW#1 Due	No Lab
	10	MOS Inspection Analysis; G&M: §3.4, R: §3.5-3.6		
	15	Freq. Response Inspection Analysis I; G&M: §7.1-7.3, R: §6.5	HW#2 Due	No Lab
	17	Freq. Response Inspection Analysis II; Active Loads; G&M: §4.3		
	22	Active Loads: 1-Tx and Multi-Tx Loads; G&M: §4.3	HW#3 Due	Lab #1: 1-Tx MOS Amp.
	24	Current Sources; G&M: §4.2, R: §5.1-5.2, R: §5.1-5.2		
	29	Supply & Temperature Indep. Biasing; G&M: §4.4.2-4.4.3, R: Chpt. 11	HW#4 Due	Lab #1 (cont.)
Oct.	1	High Swing Current Sources I; G&M: §4.2.5.2, R: §5.1-5.2		
	6	High Swing Current Sources II; G&M: §4.2.5.2, R: §5.1-5.2	HW#5 Due	Lab #2-1 Diff. Pair Anal. & Des.
	8	Current Source Matching; G&M: §A.4.1		
	13*	Op Amps: Op Amp Feedback Circuits; ECP, Half Circuits; G&M: §6.1-6.2, §3.5, R: §4.1-4.4	HW#6 Due	Lab #2-2 2nd Gain Stage Des.
	15*	Op Amps: SCP; Current Mirror Load; G&M: §4.3.5		
	20	Op Amps: Input Offset Voltage; Finite Gain-BW Product, Freq. Response in FB; G&M: §3.5.6, §A.4.2, §9.2	HW#7 Due	Lab #2-3 Complete Op-Amp Anal.
	22	Op Amps: High Gain Designs; G&M: §6.3-6.7, R: §9.3-9.4		
	27	Op Amps: Swing, Compensation & Slew Rate (a 1st pass); G&M: §9.4.1-9.4.2, §9.6.1-9.6.2, R: §9.7-9.8		Lab#2 (cont.)
	29	***Midterm Exam***		
Nov.	3	Op Amps: Output Stages; G&M: §5.1-5.5		Lab #3 CMOS Op-Amp Design Project
	5	Compensation: Stability of FB Circuits, Narrowbanding; G&M : §9.4, R: §10.1-10.3		
	10	Compensation: Pole-Splitting Pole/Zero Plots ; G&M: §9.4-9.5, R: §10.4	HW#8 Due	Work on the Design Project
	12	Compensation: For CMOS Op Amps, Choosing C_c; G&M : §9.4.3-9.4.5, R: §10.5-10.6		
	17	Compensation: CMOS Op Amp RHP Zero; G&M : §9.4.3, R: §10.5-10.6	HW#9 Due	Work on the Design Project
	19*	Slew Rate; G&M : §9.6		
	24	Settling Time & PSRR: Handout, R: §9.9	HW#10 Due	Work on the Design Project
	26	Feedback I: Pros & Cons, Inspection Analysis of FB Ckts., Influence on I/O Impedance; Handout, G&M : §8.1-8.2, §8.4, R: §8.1-8.2		
Dec.	1	Feedback II: Feedback Loading; G&M : §8.5-8.6, R: §8.1-8.3	HW#11 Due	Work on the Design Project
	3	Feedback III: Examples; G&M : Chpt. 8, R: §8.1-8.3		
	8	***Reading/Review/Recitation***		Work on the Design Project
	10	***Reading/Review/Recitation***	Project Due	
	16	***Final Exam: Wednesday, Dec. 16, 8:00-11:00 a.m. (Exam Group 9)***		

* Dates with an asterisk next to them represent those days that I will not be in town. On these dates I will make appropriate arrangements for the lecture. These will likely entail make-up lectures, possibly in the evenings, but since this course will be webcast, you can always watch the webcast if you cannot attend on the make-up date.