

PROBLEM SET #7

Issued: Tuesday, Oct. 14, 2014

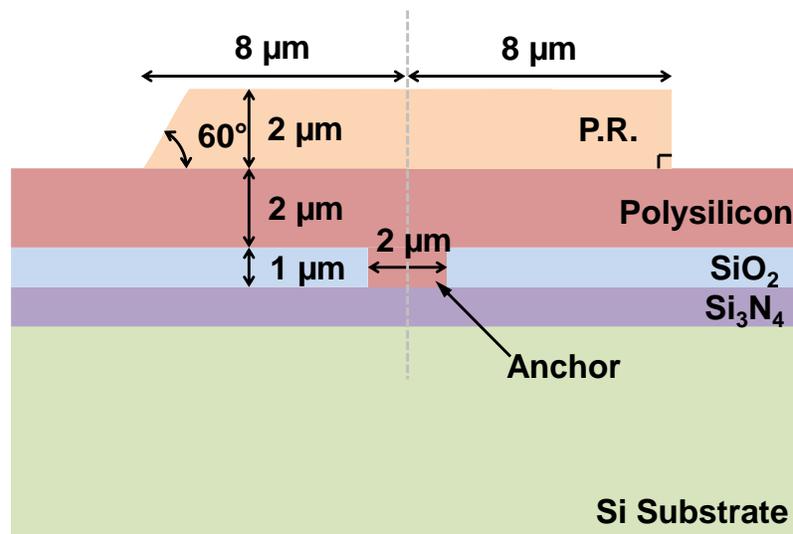
Due: Friday, Oct. 24, 2014, 8:00 a.m. in the EE 143 homework box near 140 Cory

- **Electroplating**

1. Suppose you want to fabricate MEMS clamped-clamped beam structures on a silicon wafer by electroplating nickel through a photoresist mold similar to the process discussed in the electroplating lecture. Assume the exposed area (which is not covered by the photoresist mold) is 15 cm^2 , the applied current is regulated at a constant level of 20 mA, and nickel cations in the electrolyte are Ni^{2+} . Estimate the time required to electroplate a 2- μm thick nickel structural layer. (Ni has an atomic weight of 58.69 g/mol and a density of 8.9 g/cm^3 .)

- **Etching**

2. The cross-section below is to be etched via reactive ion etching (RIE) of polysilicon. Assume that the RIE is 100% anisotropic for all materials and that the RIE etches polysilicon at a rate of $1 \mu\text{m}/\text{min}$ with the selectivity of polysilicon: SiO_2 :photoresist = 5:1:1.



- (a) Draw cross-sections of the structure with dimension labeled after etching for (a) 1 min; (b) 2 min; and (c) 3 min.
- (b) (Continuing from (a)) After etching for 3 minutes in part (a), the sample is then dipped in a liquid HF solution to etch the SiO_2 layer. Assuming the SiO_2 etch rate in HF is $2 \mu\text{m}/\text{min}$, draw the cross-section after etching in HF for 1 min. Estimate the time needed to etch the entire SiO_2 layer.

3. Suppose in the polysilicon gate patterning lab the deposited polysilicon thickness is $T_{Poly} = 400$ nm with a $\pm 10\%$ variation across the wafer and its etch rate in wet polysilicon etchant, $E.R_{Poly}$, has a $\pm 10\%$ variation.
- (a) What is the smallest percent overetch required to ensure that the polysilicon on the field area is removed? (The percent we're looking for is relative to the main etch time given by $T_{Poly}/E.R_{Poly}$)
- (b) Estimate the worst-case undercut distance of the polysilicon gate due to the main etch and overetch calculated in (a). Assume that the photoresist has an infinite selectivity against the polysilicon etchant.
- (c) Continuing from (b), estimate the worst-case variation of the saturation drain current $I_{D(sat)}$ due to the polysilicon undercut on a fabricated NMOS device with a drawn gate length $L = 4$ μm . Assume the lithography step perfectly patterns the photoresist with the same dimensions as that drawn on the mask (i.e., $L = 4$ μm). (Recall that $I_{D(sat)} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_G - V_{th})^2$.)

- **Ion Implantation**

4. Problem 5.3 and 5.8 in the textbook.