

University of California

College of Engineering

Department of Electrical Engineering

and Computer Sciences

EE143: LAB REPORT 1 — FABRICATION

 **STUDENT A:**

|  |  |
| --- | --- |
| **NAME** |  Last First |

|  |  |
| --- | --- |
| **SID** |  |

**STUDENT B:**

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| --- | --- |
| **NAME** |  Last First |

|  |  |
| --- | --- |
| **SID** |  |

**Lab Report Template:**

1. Profiles & Layout:
	1. Thin oxide MOSFET Cross Section
	2. Top Views
	3. Comb-drive MEMS Structure Cross Section
2. Process Procedures:
	1. Process Monitoring Measurements
* Measurement Type and Description
* Over-Etch/Under-Etch
* Misalignment Tolerance

B& C. Batch and Individual Processing Steps:

Week 2: Field Oxidation:

* Batch Processing Problems
* Measurements Taken

Week 3: Field Oxide Cut

* Individual Processing Problems
* Measurements Taken

Week 4: Gate Oxidation

* Batch Processing Problems
* Measurements

Week 5: Poly Deposition

* Batch Processing Problems
* Measurements

Week 6: Gate Definition

* Individual Processing Problems
* Measurements

Week 7: S/D Diffusion and Intermediate Oxidation

* Batch Processing Problems
* Individual Processing Problems
* Measurements

Week 8: Contact Hole Cut

* Individual Processing Problems
* Measurements

Week 9: Metallization

* Batch Processing Problems
* Measurements

Week 10: Metal Definition

* Batch Processing Problems
* Individual Processing Problems
* Measurements
1. Calculations:
2. Questions:
3. Bonus:
4. Appendix:

**Calculations Results Template:**

Film Thicknesses: (\*\*note: Not all lab sections took Linewidths after PR strip, those may skip that column\*\*)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Layer | Theoretical Calculation | Experimental | % Error  | Linewidths (Photoresist) | Linewidths (after PR Strip) | % Overetch |
| Field Oxide |  |  |  |  |  |  |
| Polysilicon |  |  |  |  |  |  |
| Gate Oxide |  |  |  |  |  |  |
| Intermed Oxide |  |  |  |  |  |  |
| Aluminum |  |  |  |  |  |  |

Overetch:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Layer | Measured Linewidth | % Overetch | Theoretical Etch Time | Actual Etch Time | % Overetch |
| Field Oxide |  |  |  |  |  |
| Polysilicon |  |  |  |  |  |
| Gate Oxide |  |  |  |  |  |
| Intermed Oxide |  |  |  |  |  |
| Aluminum |  |  |  |  |  |

Sheet Resistance:

|  |  |  |
| --- | --- | --- |
| Layer | Sheet Resistance | Surface Concentration (Calculated) |
| ACTV After Field Oxidation |  |  |
| Polysilicon |  |  |
| ACTV After Pre-Dep |  |  |
| ACTV After Drive-in |  |  |
| METL |  |  |

Theoretical Junction Depth

|  |  |  |
| --- | --- | --- |
| Layer | Vertical Junction Depth | Lateral Junction Depth |
| ACTV After Pre-Dep |  |  |
| ACTV After Drive-in |  |  |

**EECS 143 Lab Report 1**

Fall 2014

In signing below, I attest to the fact that I have read and have adhered to the policies

and guidelines discussed in the EECS Departmental Policy on Academic Dishonesty,

as found at: <http://www.eecs.berkeley.edu/Policies/acad.dis.shtml>

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Date:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Date:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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