<u>Lecture 6</u>: Process Integration

Announcements:

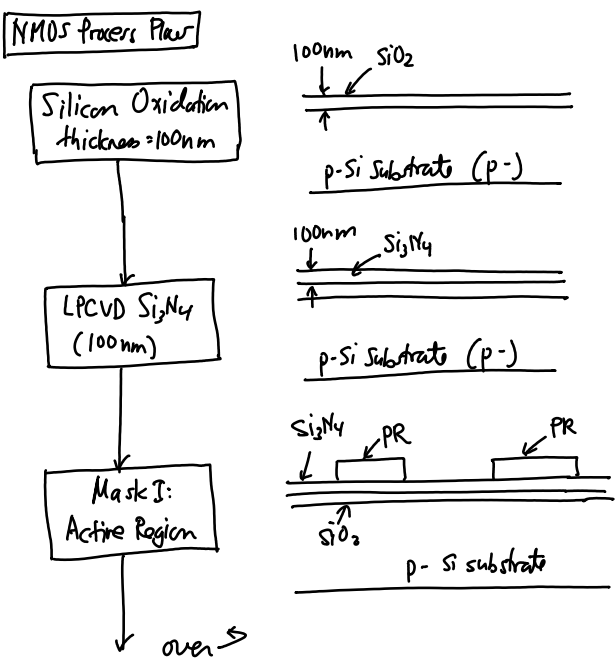
- **Lecture in 180 Tan Hall today and from now on -- ETS can record from this room**
- **ETS recording today**
- **I have Lecture 1 (with poor sound) and Lecture 5 recorded -- will transfer to ETS for posting on YouTube**

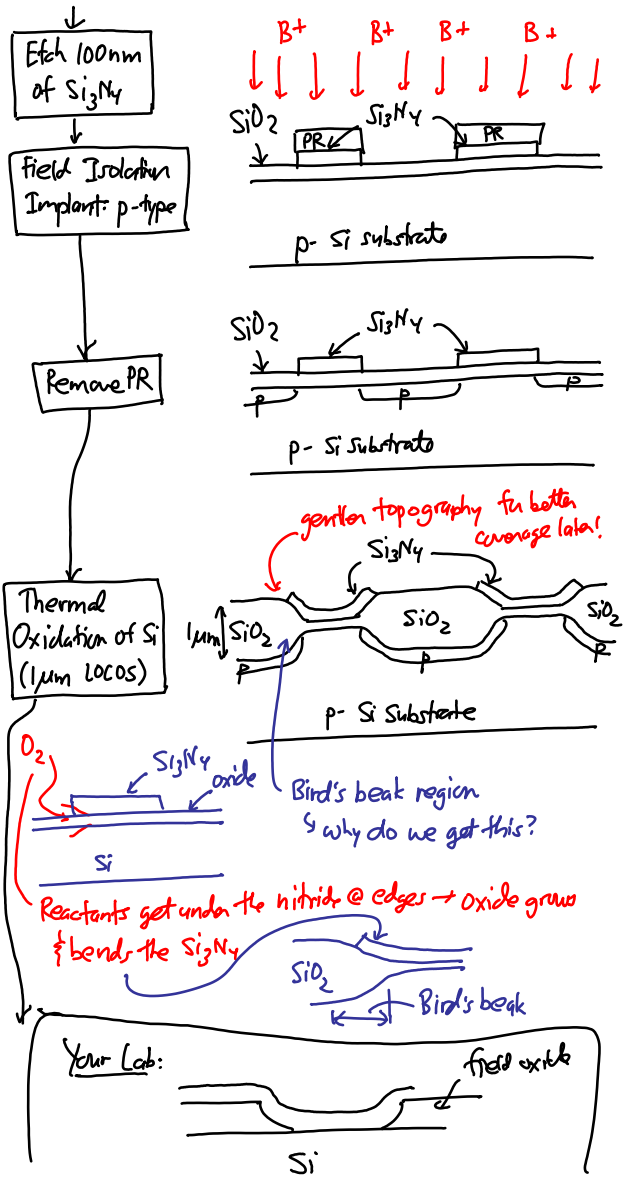
Lecture Topics:

- **Example NMOS Process (finish this)**
- **Masks & Alignment**
- **Design Rules**

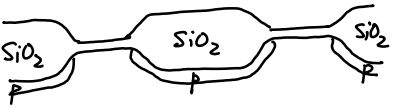
<u>Last Time</u>:

- **Started NMOS process flow**



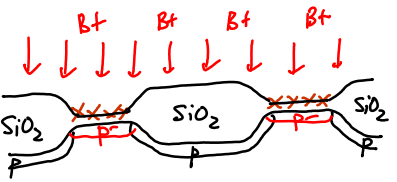

Etch 100nm of Si_3N_4
Field Isolation Implant: p-type
Remove PR
Thermal Oxidation of Si (1μm LOCOS)
B+ B+ B+ B+
SiO_2
Si_3N_4
PR
PR
p- Si substrate
SiO_2
Si_3N_4
p
p
p
p- Si Substrate
gentler topography for better coverage later!
Si_3N_4
1μm
SiO_2
SiO_2
SiO_2
p
p
p
p- Si Substrate
O_2
Si_3N_4
oxide
Si
Bird's beak region
why do we get this?
Reactants get under the nitride @ edges → oxide grows & bends the Si_3N_4
SiO_2
Bird's beak
Your Lab:
field oxide
Si

Etch All Si_3N_4 (blanket wet etch; no mask)



p- Si Substrate

Threshold Voltage Implant: B+ (no mask)



p- Si Substrate

LOCOS oxidation serves as mask
↳ implant only gets into active areas (where it should be)

⇒ Now, the oxide above the active area is damaged → can't use it as the gate oxide, since the gate oxide must be pure & defect free! → must regrow it!

Remove 100nm of Damaged Oxide (wet etch → hydrofluoric acid (HF)

p- Si Substrate

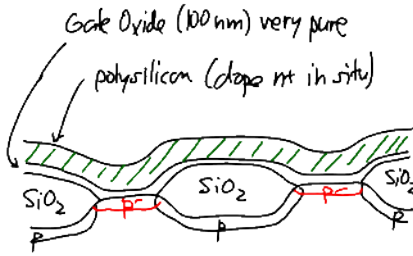
Thermal Oxidation (100 nm gate oxide)

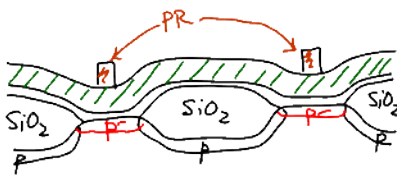
CVD of Doped Gate Polysilicon (500 nm)

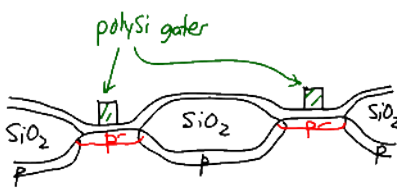
Mask II: PolySi Gate Definition

Dry Etch 500nm polySi

Remove PR

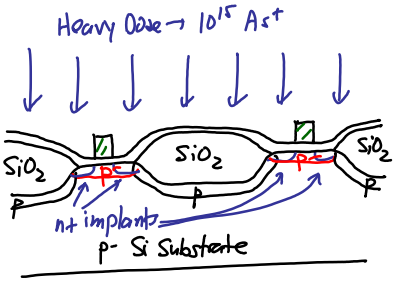




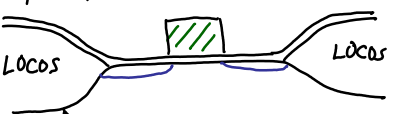


Need to remove PR, since the next step is a high energy I/I → will polymerize the PR and make it difficult to remove!

Drain/Source Ion/Implantation ($n+ \rightarrow P$ or As)



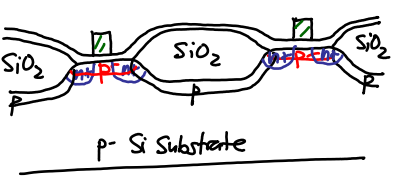
Here, the gate polySi is doped while also serving as a mask for the D/S implantation.



LOCOS serves as the other side of the S/D implant mask.

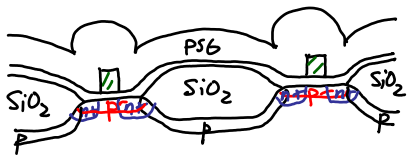
Note how no extra lithography step is needed to mask the implant.

10 nm Oxidation & Drive-In Diffusion Anneal @ 1050°C



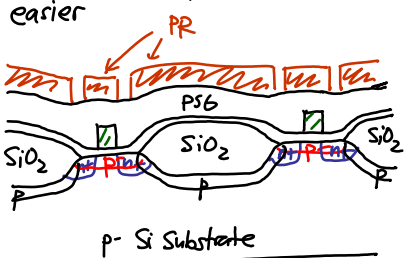
⇒ Note: The initial oxidation repairs the damaged (after implantation) oxide over the S/D regions so that dopants don't escape that way during diffusion.

CVD of Glass (PSG or LTO) (1μm)



PSG ≜ phosphosilicate glass
↳ SiO_2 w/ 7% of phosphorous
↳ the phosphorous helps the oxide to reflow at high temperature
↳ get a more planar surface
↳ makes lithography & other steps easier

Reflow PSG + a Bit More Diffusion



→ This not only drives in the S/D; it also activates the dopants!

Mask III: Contact Hole

← what it really looks like vs.

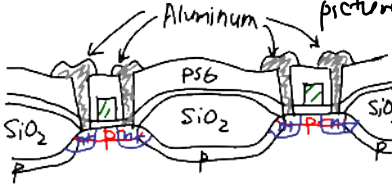
Compressed picture

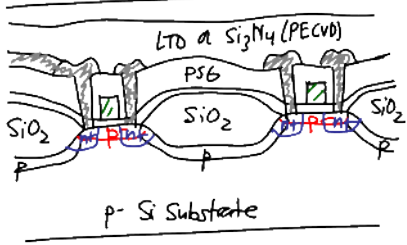
Sputter Al (1 μm)

Mask IV: Metal

Dry Etch the Al

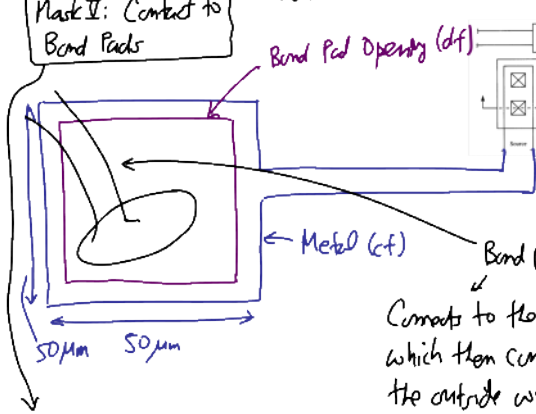
Deposit LTO or PECVD Si_3N_4 to Serve As Passivation





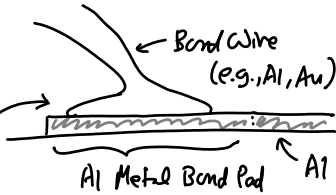
Passivation protects the metal layer from contaminants & erosion.

Mask V: Contact to Bond Pads



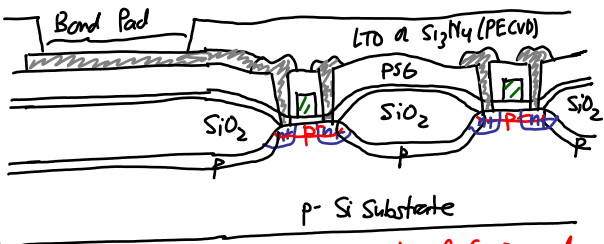
Bond Wire

Connects to the package, which then connects to the outside world



ultrasonic energy often used to insure a good bond & contact between metals

Etch Passivation Layer down to Metal



Optional for Research

Spin Double-Thick PR Over Front Side

Successive Wet Etches to Remove Layers → Expose Backside

To allow bracing of the substrate.

Mask to Cross-Section

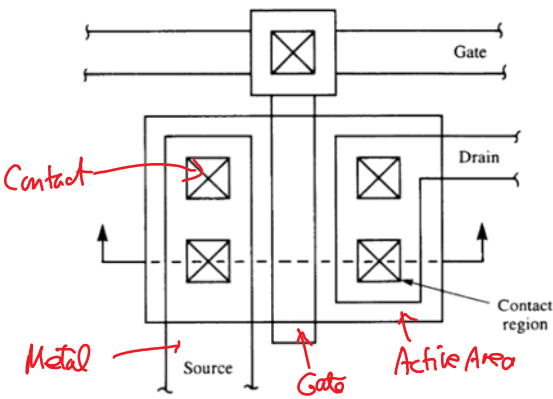
⇒ one skill you must learn:

Given: ① Process Flow
② Mask Layout

Draw the cross-section along various lines and at various steps in the process flow.

Example: NMOS Process

Layout:

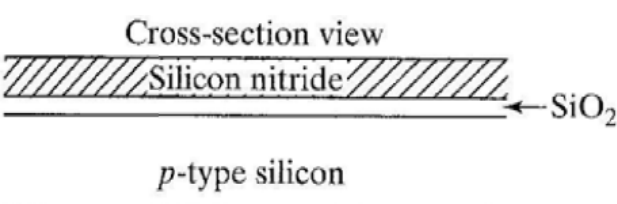


Process Flow:

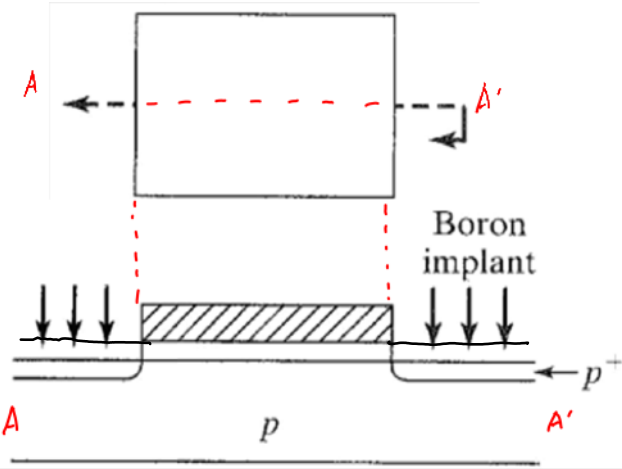
1. Silicon oxidation: target = 100nm
2. LPCVD Si_3N_4: target = 100nm
3. Lithography: Mask I (active area)
4. Etch Si_3N_4 to clear it in field areas
5. Field isolation implant: B+ (p-type)
6. Remove PR
7. Grow 1~~nm~~ μ of SiO_2 by thermal oxidation (LOCOS oxidation)
8. Blanket etch all Si_3N_4 in hot phosphoric acid wet etchant
9. Threshold voltage implant: B+ (no mask)

10. Remove 100nm of damaged oxide via a timed wet etch in hydrofluoric acid (HF)
11. Grow 100nm of gate thermal oxide in an ultra-clean furnace
12. LPCVD situ phosphorous-doped gate polysilicon
13. Lithography: Mask II (gate polysilicon)
14. Dry etch polysilicon to clear the field areas
15. Remove PR
16. D/S ion implantation: P or As (n-type)
17. Oxidize a bit (10nm) and anneal at 1050°C to activate dopants and drive-in diffusion
18. LPCVD PSG: target = 1μm
19. Reflow PSG (& a little bit of diffusion) at 950°C
20. Lithography: Mask III (contact hole)
21. Dry/wet etch SiO_2 down to n+ S/D regions
22. Sputter Al: target = 1μm
23. Lithography: Mask IV (metal)
24. Dry etch Al
25. Deposit via LTO or PECVD Si_3N_4 to serve as passivation
26. Lithography: Mask V (bond pad contacts)
27. Etch passivation layer down to metal
28. (optional) spin double-thick PR over the front side
29. Etch backside layers via successive wet processes (to allow biasing of the substrate)

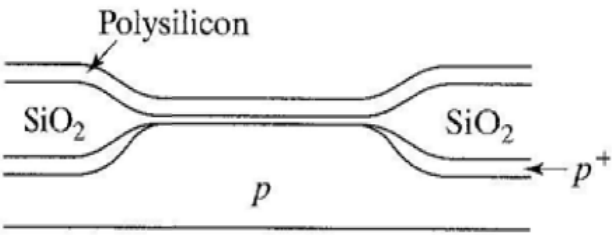
Through step 2:



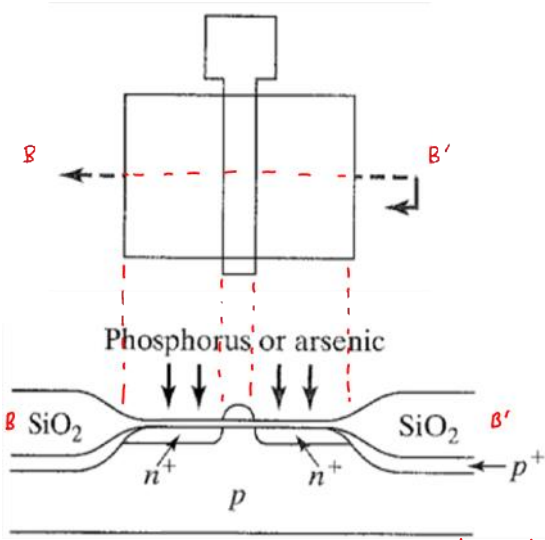
Through step 5:



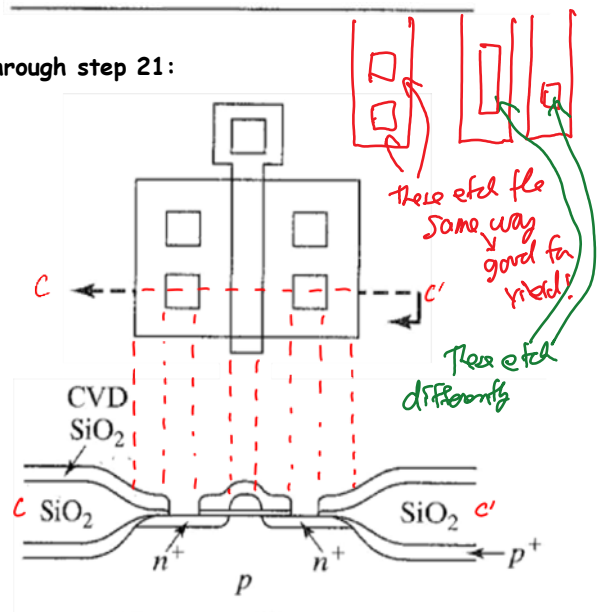
Through step 12:

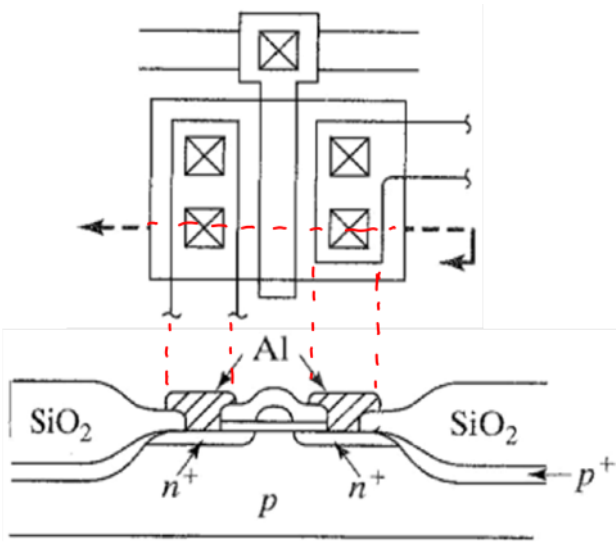


Through step 16:

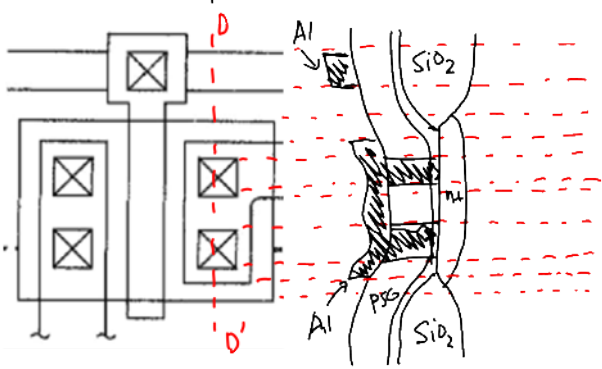


Through step 21:





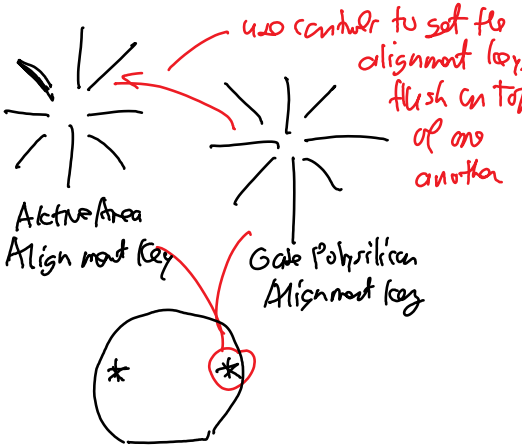
How about a sideways cross-section?

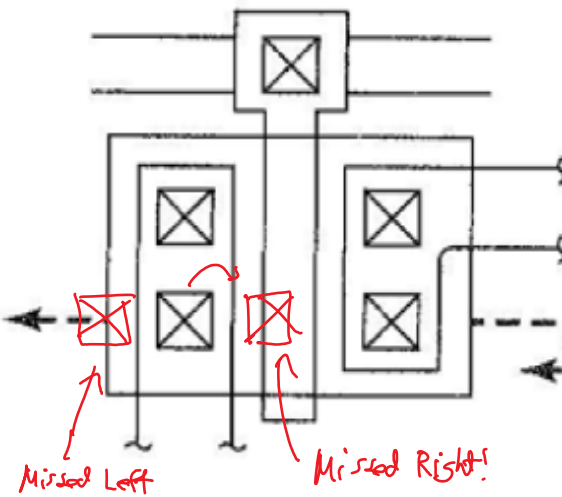


Marks & Alignment

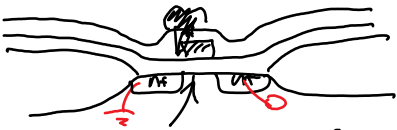
⇒ in NMOS, we have 5 masks

⇒ have 5 targets to align to → alignment keys





If misused right.



Big Problem! Source & Gate are electrically connected!