

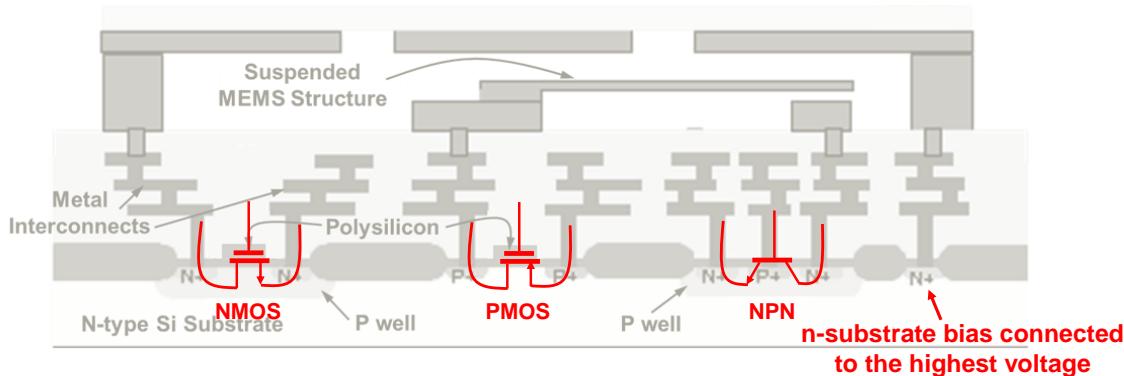
## PROBLEM SET #1 (SOLUTIONS)

*Issued: Tuesday, Sep. 2, 2014*

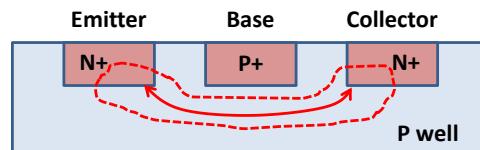
*Due: Wednesday, Sep. 10, 2014, 8:00 a.m. in the EE 143 homework box near 140 Cory*

### I. Device Cross-Sections/Symbols

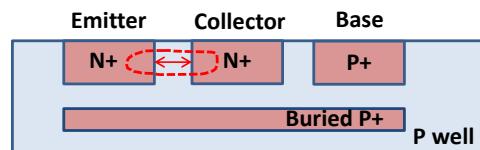
1. Consider the merged MEMS-transistor integrated circuit cross-section shown below. Identify the transistors (i.e., two MOS and one bipolar transistor) and draw the corresponding symbols for each of the transistors on top of the figure in the appropriate positions, i.e., with the “arrow part” of the symbol over the right region, etc.



Note that the bipolar device in the circuit would have a poor performance due to its large base width as shown below.



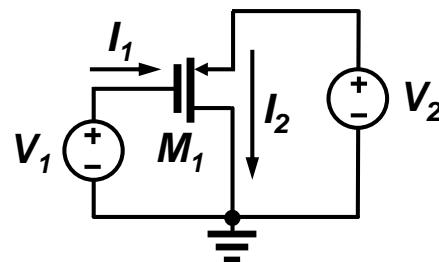
In practice, to make a lateral bipolar device (in contrast to the vertical version discussed in lecture), the configuration of terminals would rather be arranged to minimize the base width, such as



### II. MOSFET Characteristics

2. Consider the following circuit. Assume that transistor  $M_1$  is operated in the saturation region and that its bias voltages,  $V_1$  and  $V_2$ , process parameter  $K$  ( $= \mu$

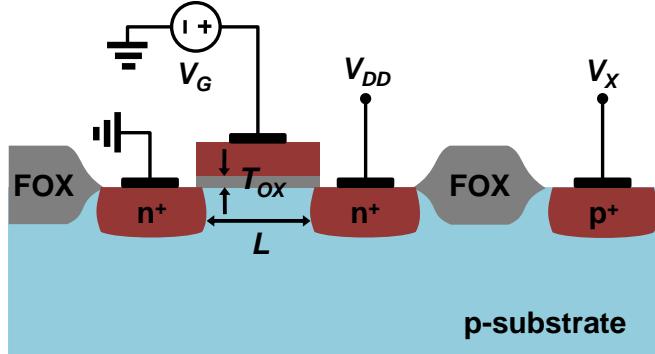
$C_{ox}$ ), and threshold voltage  $V_{th}$  can be changed independently. Assume there are no non-ideal effects except channel length modulation. Indicate in the table how an *increment* in each of these parameters changes the gate current  $I_1$ , and the drain current  $I_2$ . Use symbols:  $\uparrow$  for increase,  $\downarrow$  for decrease, -- for no change.



	$I_1$	$I_2$
$V_1 \uparrow$	--	$\downarrow$
$V_2 \uparrow$	--	$\uparrow$
$K \uparrow$	--	$\uparrow$
$V_{th} \uparrow$	--	$\downarrow$

3. Consider the cross-section of an NMOS device shown below.

Assume the channel length  $L = 0.5 \mu m$ , the channel width  $W = 50 \mu m$ , the gate oxide thickness  $T_{ox} = 9 nm$ , the Fermi level  $\Phi_F = 0.4 V$ , the zero-bias threshold voltage  $V_{th0} = 0.7 V$ , the substrate doping concentration  $= 9 \times 10^{14} cm^{-3}$ , and the relative permittivity of Si = 11.8 and of  $SiO_2$  = 3.9, respectively.



- a. Calculate the threshold voltage when  $V_X = 0.5 V$ ,  $V_{DD} = 5 V$ , and  $V_G = 2 V$ .

$$V_S = 0V, V_B = V_X = 0.5V$$

$$V_{th} = V_{th0} + Y \left( \sqrt{V_{SB} + 2|\phi_f|} - \sqrt{2|\phi_f|} \right)$$

$$C_{ox} = \frac{\epsilon_{SiO2}}{T_{ox}} = 3.84 \times 10^{-7} F/cm^2$$

$$Y = \frac{\sqrt{2q\epsilon_{Si}N_B}}{C_{ox}} = 0.0452 V^{1/2}$$

$$V_{th} = 0.7 + 0.0452(\sqrt{(0 - 0.5) + 0.8} - \sqrt{0.8}) = 0.684 V$$

- b. (Continuing from a.) Calculate the drain current  $I_D$ .

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_G - V_{th})^2 = \frac{1}{2} 350 \times 3.84 \times 10^{-7} \times \frac{50}{0.5} (2 - 0.684)^2 = 11.638 \text{ mA}$$

- c. Repeat b. with  $V_X = 0 \text{ V}$ .

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_G - V_{th0})^2 = 11.357 \text{ mA}$$

- d. Now, suppose  $V_X$  can be varied while other voltage biases are fixed. Calculate the value of  $V_X$  that causes the device to cut off.

Device cuts off when  $V_G = V_{th} = 2 \text{ V}$ ,

$$V_{th} = V_{th0} + Y \left( \sqrt{V_{SB} + 2|\phi_f|} - \sqrt{2|\phi_f|} \right)$$

$$2 = 0.7 + 0.0452 \left( \sqrt{|(V_S - V_B) + 0.8|} - \sqrt{0.8} \right) \Rightarrow V_B = -878.65V$$

\* Obviously, this is an unreasonably large voltage that such transistors can't tolerate. However, in typical transistors the body effect parameter would be in the range of 0.3 to 0.4  $\text{V}^{1/2}$ , which makes the value of  $V_B$  that cuts off the device around a reasonable -15V.

### III. Fabrication Yield/Cost

4. The cost of processing a wafer in a particular process is \$1,000. Assume that 85% of the fabricated dice are good. For this problem, use the figure below (i.e., Fig. 1.1(c) in the textbook) to determine the number of dice.

- a. Determine the cost per good die for a 150 mm wafer.

$$\begin{aligned} \text{A } 150\text{-mm wafer has } &\sim 200 \text{ } 10 \times 10\text{-mm dies } \rightarrow \text{cost/good die} = \\ \$1000 / 200 \times 0.85 &= \$5.88. \end{aligned}$$

- b. Repeat for a 200 mm wafer.

Given the same fabrication cost and yield, a larger wafer results more dies and consequently lower cost per unit.

$$\text{cost/good die} = \$1000 / 300 \times 0.85 = \$3.92.$$

