PROBLEM SET #10

Issued: Tuesday, Nov. 18, 2014

Due: Wednesday, Nov. 26, 2014, 8:00 a.m. in the EE 143 homework box near 140 Cory

1. Referring to the layout and process flow in HW#9, answer the following questions.
   a) Briefly explain the purpose of the sacrificial oxide done in step 15.

      To protect the substrate surface from being damaged in the following implantation steps

   b) Why did we do a backside etch in step 31?

      To allow electrical access/biasing via the backside of the substrate

   c) Identify all control wafers in the process and explain what they are used for.

      - PWELL

      1. Determine the bulk resistivity (0.0)
      2. Monitor the sheet resistance of p-well after well drive-in (5.5)
      3. Use to determine the etch time of pad oxide on p-well region (15.2)
      4. Use to determine the etch time of sacrificial oxide on p-well region (17.3)
      5. Monitor the capacitor oxide thickness on p-well region (20.3)
      6. Monitor the poly sheet resistance after PSG deposition on p-well region (NMOS) (28.4)
      7. Monitor the backside sheet resistance and the sheet resistance at the S/D contact region for NMOS (36.0)

      - PCH

      1. Monitor the sheet resistance of outside the p-well after well drive-in (5.5)
      2. Use to determine the etch time of pad oxide on outside the p-well region (15.2)
      3. Use to determine the etch time of sacrificial oxide outside the p-well region (17.3)
      4. Monitor the capacitor oxide thickness outside the p-well region (20.3)
      5. Monitor the poly sheet resistance after PSG deposition outside the p-well region (PMOS) (28.4)
      6. Monitor the backside sheet resistance and the sheet resistance at the S/D contact region for PMOS (36.0)

      - 1 Tox monitoring wafer for monitoring pad oxide thickness
      - 3 Tox monitoring wafers for monitoring gate oxide thickness
      - Tpoly1 monitoring wafers for monitor gate poly thickness

- Tpoly2 monitoring wafers (from one of the gate oxide monitoring wafer) for monitoring capacitor poly2 thickness
- PSG monitoring wafers for monitoring the PSG thickness

d) What is the total thickness of oxide over the field regions?

Before the oxidation in step 15 and step 17, the field oxide would be etched partially according to the thickness of pad oxide and sacrificial oxide on the monitor wafers, respectively. The final thickness after capacitor oxide growth would be 0.699 μm + 0.7 μm (PSG) = 1.4 μm.

Dry	T	B/A	B	A	Xi	tau	t	Xo	(μm)	step	
	950	0.021252	0.006589	0.310032	0.025	1.271246	1	0.042454		6	pad
Wet	T	B/A	B	A	Xi	tau	t	Xo	(μm)	step	
	950	0.345731	0.235621	0.681515	0	0	4.666667	0.761821		13	locos
Dry	T	B/A	B	A	Xi	tau	t	Xo	(μm)	step	
	950	0.021252	0.006589	0.310032	0.719367	112.3925	0.5	0.721249		15	sac. Ox
Dry	T	B/A	B	A	Xi	tau	t	Xo	(μm)	step	monitor
	950	0.021252	0.006589	0.310032	0.025	1.271246	0.5	0.033929		15	sac. Ox
Dry	T	B/A	B	A	Xi	tau	t	Xo	(μm)	step	
	950	0.021252	0.006589	0.310032	0.68732	104.0424	2	0.695106		17	gate ox
Dry	T	B/A	B	A	Xi	tau	t	Xo	(μm)	step	
	950	0.021252	0.006589	0.310032	0.695106	106.0424	0.916667	0.698651		20	cap ox

e) What is the depth x_{jn} of the NMOS n+ S/D junctions at the end of the process?

After gate oxidation (step 17) and intermediate oxide of capacitor growth (step 20.3), the oxide thickness is about 0.072 μm (2 hrs + 55 min).

Figure 5.3 yields a 0.09 μm projected range and a 0.032 μm straggle (i.e., an equivalent $Dt = \frac{1}{2} \times (0.032 \times 10^{-4})^2 = 5.12 \times 10^{-12} cm^2$) with a 160 keV implant energy for As. Therefore, the peak of concentration would locate at 0.09 – 0.072 = 0.018 μm below the Si/SiO_2 interface. The percentage of dose inside Si over total dose would be $\frac{1}{2} + \frac{1}{2}\text{erf}\left(\frac{0.018}{0.032\sqrt{2}}\right) = 73.1\%$, which corresponds to a dose of $3.65 \times 10^{15}/cm^2$. The arsenic dopants that diffuse toward oxide would bounce off the oxide and then diffuse into Si.

As dopants experience every high temperate step at and after step 25:

step	temp	hour	hour	hour	D	Dt
25	925	1.250			3.375E-16	1.51873E-12
28	450	0.583			4.883E-26	1.02543E-22
	950	0.083	0.333	0.083	6.83E-16	1.22939E-12
35	400	0.333			6.998E-28	8.39743E-25
sum						2.74813E-12

Thus, the total $Dt = 5.12 \times 10^{-12} + 2.75 \times 10^{-12} = 7.87 \times 10^{-12} cm^2$

Considering the punchthrough implants (i.e., P at 145keV w/ dose = 1.2×10^{12}) that yields a 0.18 μm projected range and a 0.06 μm straggle and implants through the initial oxide 0.12 μm (*cf.* HW#9), the punchthrough dose inside Si is approximated as $1.2 \times 10^{12} \times (\frac{1}{2} + \frac{1}{2}\text{erf}\left(\frac{0.06}{0.06\sqrt{2}}\right)) = 1 \times 10^{12} cm^{-2}$, and the P implants experience the same high temperature steps as P-well implants (B) (i.e., the same Dt since B and P have the same diffusion constant D).

The junction depth inside p-well (considering B and P dopants) would be (referring to HW#9)

$$\frac{1.5\times10^{12}-1\times10^{12}}{\sqrt{\pi}\cdot 2.93\times10^{-8}}\exp\left(-\left(\frac{x}{2\sqrt{2.93\times10^{-8}}}\right)^2\right) = \frac{3.65\times10^{15}}{\sqrt{\pi}\cdot 7.87\times10^{-12}}\exp\left(-\left(\frac{x-0.018\mu m}{2\sqrt{7.87\times10^{-12}}}\right)^2\right),$$

$$\Rightarrow x = 0.219\mu m$$

In fact, since the P-well junction is more deeper (i.e., ~5μm) than the S/D junction, the above equation can be approximated as the P-well has a constant concentration $\frac{1.5\times10^{12}-1\times10^{12}}{\sqrt{\pi}\cdot 2.93\times10^{-8}} = \frac{3.65\times10^{15}}{\sqrt{\pi}\cdot 7.87\times10^{-12}}\exp\left(-\left(\frac{x-0.018\mu m}{2\sqrt{7.87\times10^{-12}}}\right)^2\right)$, which yields a very close value of x.

f) What is the depth x_{jp} of the PMOS p+ S/D junctions at the end of the process?

Figure 5.3 yields a 0.1 μm projected range and a 0.035 μm straggle (i.e., the equivalent $t = \frac{1}{2} \times (0.035 \times 10^{-4})^2 = 6.13 \times 10^{-12} cm^2$) with a 30 keV implant energy for boron. Therefore, the peak of concentration would locate at 0.1 – 0.072 = 0.028 μm below the Si/SiO_2 interface. The percentage of dose inside Si over total dose would be $\frac{1}{2} + \frac{1}{2}\text{erf}\left(\frac{0.028}{0.035\sqrt{2}}\right) = 78.8\%$, which corresponds to $3.94 \times 10^{15} / cm^2$. The boron dopants that diffuse toward oxide would bounce off the oxide and then diffuse into Si.

Boron dopants experience high temperate steps listed as below.

step	temp	hour	hour	hour	D	Dt
28	450	0.583			1.988E-25	4.17565E-22
	950	0.083	0.333	0.083	6.527E-15	1.1749E-11
35	400	0.333			2.44E-27	2.92846E-24
						0
sum						1.1749E-11

Thus, the total $Dt = 6.13 \times 10^{-12} + 1.175 \times 10^{-11} = 1.79 \times 10^{-11} cm^2$

The junction depth in the n-substrate (background + punchthrough) would be (referring to HW#9)

$$4 \times 10^{14} + \frac{1\times10^{12}}{\sqrt{\pi}\cdot 2.93\times10^{-8}}\exp\left(-\left(\frac{x}{2\sqrt{2.93\times10^{-8}}}\right)^2\right) = \frac{3.94\times10^{15}}{\sqrt{\pi}\cdot 1.79\times10^{-11}}\exp\left(-\left(\frac{x-0.028\mu m}{2\sqrt{1.79\times10^{-11}}}\right)^2\right)$$

, where the 4×10^{14} is the substrate background concentration.

Again, the punchthrough concentration can be approximated as a constant value around the S/D junction, which leads to a very close value of junction depth

$$4\times10^{14}+\frac{1\times10^{12}}{\sqrt{\pi\cdot2.93\times10^{-8}}}=\frac{3.94\times10^{15}}{\sqrt{\pi\cdot1.79\times10^{-11}}}\exp\left(-\left(\frac{x-0.028\mu m}{2\sqrt{1.79\times10^{-11}}}\right)^2\right),\Longrightarrow x=0.32\ \mu m$$

g) What is the gate-overlap capacitance (i) for NMOS devices? (ii) for PMOS devices?

(i) 160 keV As has a lateral straggle of 0.032 μm (i.e., equivalent to a diffusion step of "DT" $=\frac{1}{2}\times(0.032\times10^{-4})^2=5.12\times10^{-12}cm^2$).

The total $Dt=5.12\times10^{-12}+2.75\times10^{-12}=7.87\times10^{-12}cm^2$

Therefore, the lateral junction depth can be calculated by

$\frac{1.5\times10^{12}-1\times10^{12}}{\sqrt{\pi\cdot2.93\times10^{-8}}}=\frac{3.65\times10^{15}}{\sqrt{\pi7.87\times10^{-12}}}\exp(-\left(\frac{y}{2\sqrt{7.87\times10^{-12}}}\right)^2)$, → y=0.202 μm.

The NMOS overlap capacitance would be $3\mu m*0.202\mu m*\frac{3.9*8.854\times10^{-12}}{59.53\times10^{-9}}=0.352\ fF$. (where $3\mu m$ is the NMOS device width drawn on the layout)

(ii) 30 keV B has a lateral straggle of 0.055 μm (i.e., equivalent to a diffusion step of "DT" $=\frac{1}{2}\times(0.055\times10^{-4})^2=1.51\times10^{-11}cm^2$).

The total $Dt=1.51\times10^{-11}+1.175\times10^{-11}=2.69\times10^{-11}cm^2$

Therefore, the lateral junction depth can be calculated by $4\times10^{14}+\frac{1\times10^{12}}{\sqrt{\pi\cdot2.93\times10^{-8}}}=\frac{3.94\times10^{15}}{\sqrt{\pi2.69\times10^{-11}}}\exp\left(-\left(\frac{y}{2\sqrt{2.69\times10^{-11}}}\right)^2\right)$, → y=0.354 μm..

The PMOS overlap capacitance would be $9\mu m*0.354\mu m*\frac{3.9*8.854\times10^{-12}}{59.53\times10^{-9}}=1.85\ fF$. (where $9\mu m$ is the PMOS device width drawn on the layout)