# PROBLEM SET #4

*Issued: Tuesday, Sep. 24, 2014*

*Due: Wednesday, Oct. 1, 2014*, 8:00 a.m. in the EE 143 homework box near 140 Cory

## • Photolithography

1. The linear coefficient of thermal expansion of the material used for a photolithography mask is given by the expression

$$TC_F = \frac{1}{L}\frac{\partial L}{\partial T} \approx \frac{\Delta L}{L}\frac{1}{\Delta T}$$

where $L$ is a length on the mask and $T$ is temperature. Suppose that an alignment accuracy of 0.5 μm across a 6-inch silicon substrate is required from one layer to the next. Assume the thermal expansion of silicon is negligible in comparison and that all previous masking steps were done with masks at the same temperature as the silicon wafer.

(a) Assuming that a scanning 1:1 projection printer with global alignment is used and that soda-lime glass is used as the mask material which has a coefficient of thermal expansion $TC_F$ = 9 ppm/K, how close should the temperature of the mask be kept relative to the silicon wafer during alignment in order to achieve this accuracy? (i.e., what is the maximum allowable temperature deviation?)

$$TC_F \approx \frac{\Delta L}{L}\frac{1}{\Delta T} = \frac{0.5\mu m}{6inch}\frac{1}{\Delta T} = \frac{9ppm}{℃}$$
$$\rightarrow \Delta T = 0.37℃$$

(b) Repeat (a) for the case of a 10:1 projection stepper with die-to-die alignment. Assume the die size is 1 cm$^2$. Is this better than for the 1:1 projection printer?

$$TC_F \approx \frac{\Delta L}{L}\frac{1}{\Delta T} = \frac{0.5\mu m * 10}{1cm * 10}\frac{1}{\Delta T} = \frac{9ppm}{℃} \rightarrow \Delta T = 5.56℃$$

This is better than 1:1 contact aligner in term of the temperature tolerance.

(c) Repeat (b) but replace soda-lime glass with quartz for the mask material. (Typically, quartz has a coefficient of thermal expansion $TC_F$ = 0.5 ppm/K.)

$$TC_F \approx \frac{\Delta L}{L}\frac{1}{\Delta T} = \frac{0.5\mu m * 10}{1cm * 10}\frac{1}{\Delta T} = \frac{0.5ppm}{℃} \rightarrow \Delta T = 100℃$$

2. Consider the following cross-section and layout of a NMOS device fabricated up to the step upon opening contacts and the remaining process steps. Suppose that a much longer drive-in time than that required was accidentally performed prior to the PSG

deposition, so you decide not to reflow the PSG at high temperatures (which otherwise would diffuse the dopants too much, possibly shorting the S/D regions in some areas).

(a) Assuming that the photoresist is applied with the same thickness over all flat surfaces and that the lens in the photolithography stepper used here has a numerical aperture $NA$ = 0.5, calculate the maximum allowable wavelength that ensures the contact openings can be resolved on both active region and polysilicon gate.

DOF needs to cover the full depth of PR, which is 0.85 µm, or ±0.425 µm.

$$DOF = \pm\frac{\lambda}{2NA^2} \geq \pm 425\ nm \Rightarrow \lambda \geq 212.5\ nm$$

The minimum resolution required to resolve the contacts is 500 nm.

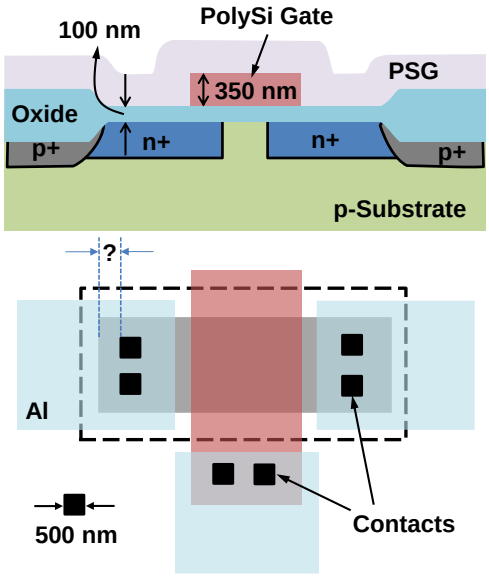
$$F = \frac{0.6\lambda}{NA} \leq 500\ nm \Rightarrow \lambda \leq 416.7\ nm$$

So, the maximum allowable wavelength is 416.7 nm.

(b) Continuing from (a), now suppose the light source has a fixed wavelength of 435.8 nm (i.e., the G-line wavelength used in your labs). What value of numerical aperture is required to successfully expose and open contacts to both the S/D regions and the polysilicon gate? What is the corresponding smallest feature size that can be resolved in this case?

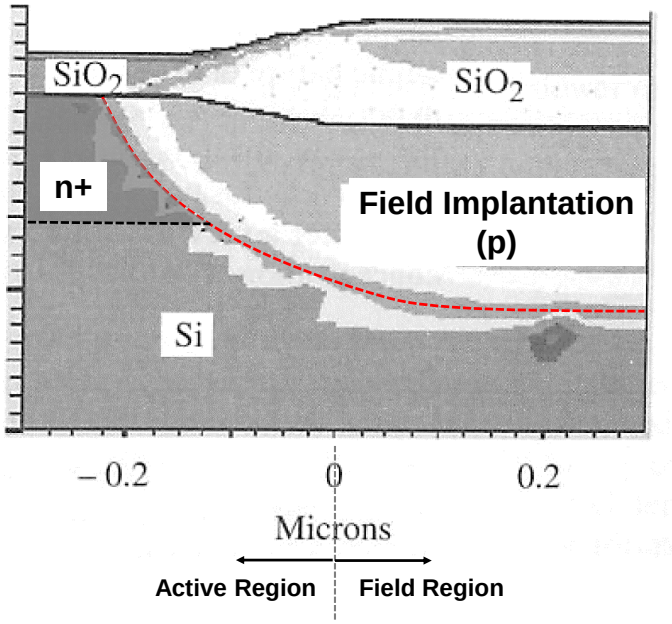
$$DOF = \pm\frac{\lambda}{2NA^2} = \pm 425\ nm \Rightarrow NA = 0.716$$

$$F = \frac{0.6\lambda}{NA} = 365\ nm$$




- ...
- Anneal at 1050°C to activate dopants and drive-in diffusion (drive-in for too long!)
- LPCVD PSG: target = 1 µm ~~and reflow at 950°C~~
- Lithography: Contact (dark field)
- Etch SiO2 down to S/D regions and polysilicon
- Remove PR
- Deposit Al: sputtering target = 1µm
- Lithography: Al Metal (clear field)
- Dry etch Al
- Remove PR

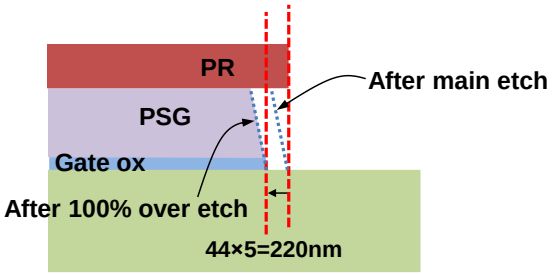
(c) Assume that the stepper has a ±0.25 μm alignment tolerance for *x* and *y* directions, and that oxide dry etching used to open the contact holes has an etch rate of 220 nm/min in the vertical direction with an anisotropy of 5:1 (i.e., 44 nm/min etched in the lateral direction) for both PSG and thermal oxide and does not etch the photoresist. Suppose a 100% over-etch is performed to ensure fully opened contact holes. Assuming that upon contact opening, the Bird's beak region of the device created by the LOCOS process has a cross-section as shown below (where the origin of the *x*-axis aligns to the edge of the active region mask), determine the design rule governing the minimum spacing required for contacts inside the active area.




The minimum spacing for contacts within the active regions accounts for 1) alignment error, 2) undercut of contact holes, and 3) encroachment on the active regions by the LOCOS field oxide.

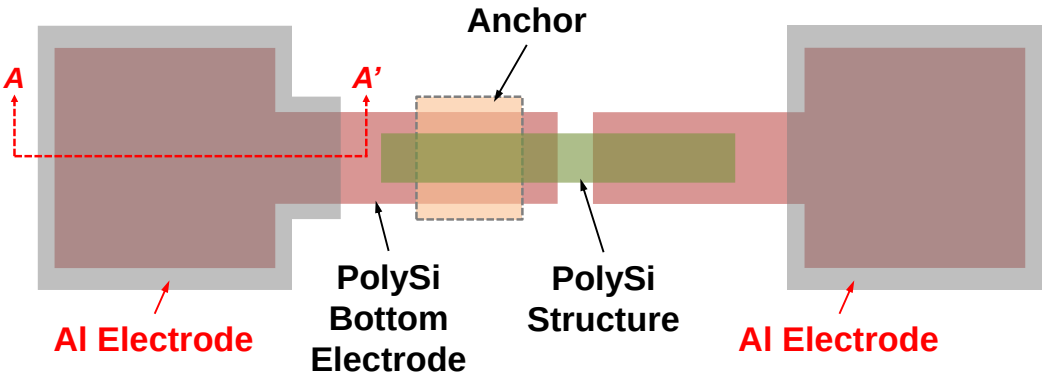
1) The maximum misalignment could be $250\ nm \times 2 = 500nm$, e.g., active regions miss by $+250\ nm$ and contacts miss by $-250\ nm$.
2) Undercut of oxide is $220\ nm$. The oxide opening on the substrate surface would be wider than the edge of PR (i.e., to which the contact opening was supposed to align if there is no lateral etching) by $220\ nm$ due to the additional 100% over-etch.
3) The p field implantation encroaches into active regions by $225\ nm$ due to the LOCOS process.

So, the minimum spacing should be $500 + 220 + 225 = 945\ nm$.



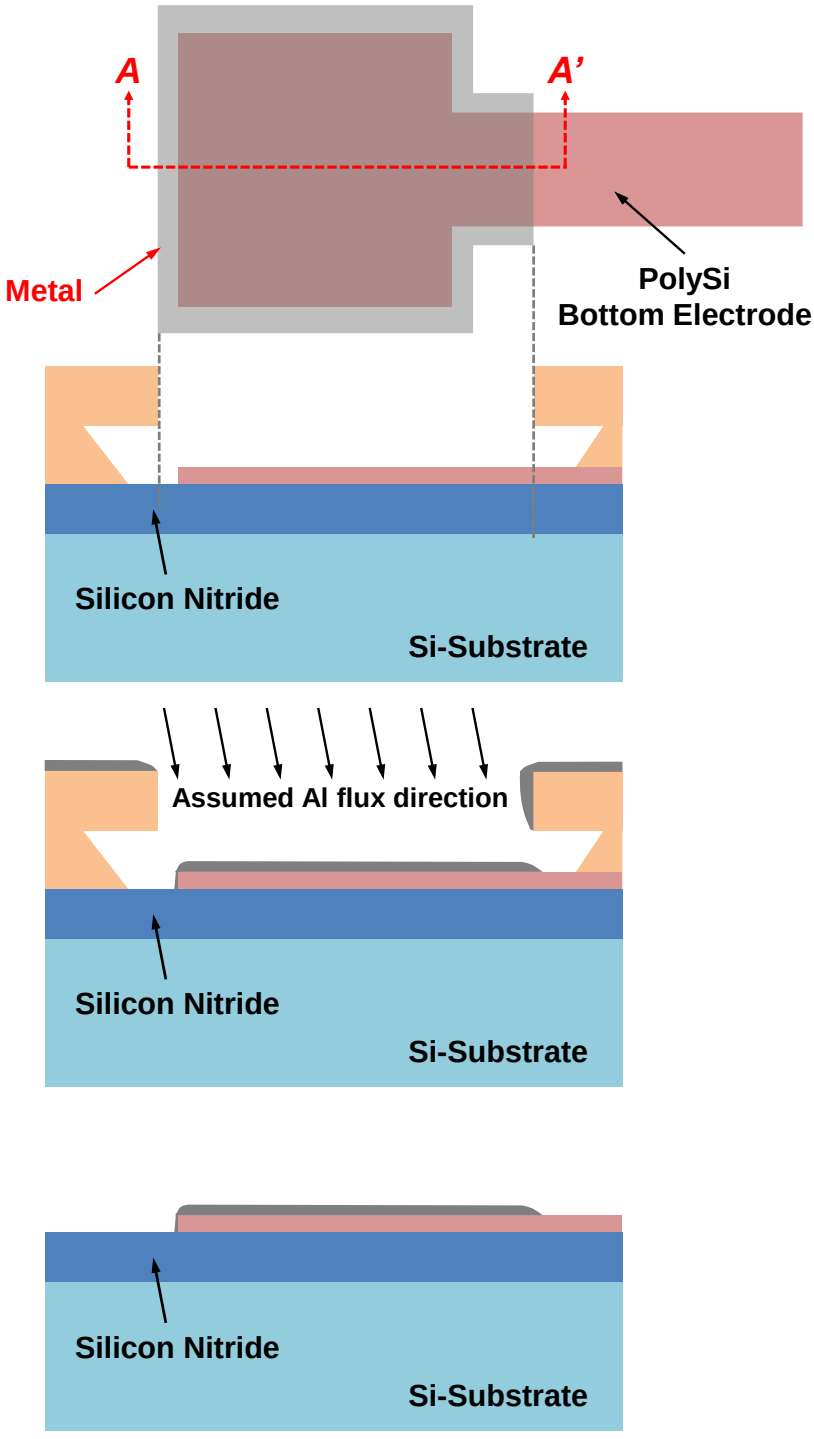

3. HW#3 Problem 2 achieved a MEMS cantilever with underlying bottom electrodes. Suppose that the polysilicon bottom traces exhibit unexpected high resistance, and you want to reduce the resistance by adding a layer of aluminum that covers the polysilicon traces as illustrated in the layout below. To avoid a need to etch aluminum, you pattern the aluminum via "lift-off", which is described in the process flow below.

   Draw the cross-sections along *AA'* plane through step 4), 5), and 6).




Two-Layer Lift-off Process Flow

1) Spin on 1.1 μm g-line photoresist
2) Flush expose (i.e., with no mask)
3) Spin on 1.1 μm g-line photoresist
4) Lithography: Mask IV (Al Electrode, **dark field**): expose and develop
5) Evaporate Al: target = 200 nm
6) Remove photoresist in acetone


A
A'
Metal
PolySi
Bottom Electrode
Silicon Nitride
Si-Substrate
Assumed Al flux direction
Silicon Nitride
Si-Substrate
Silicon Nitride
Si-Substrate