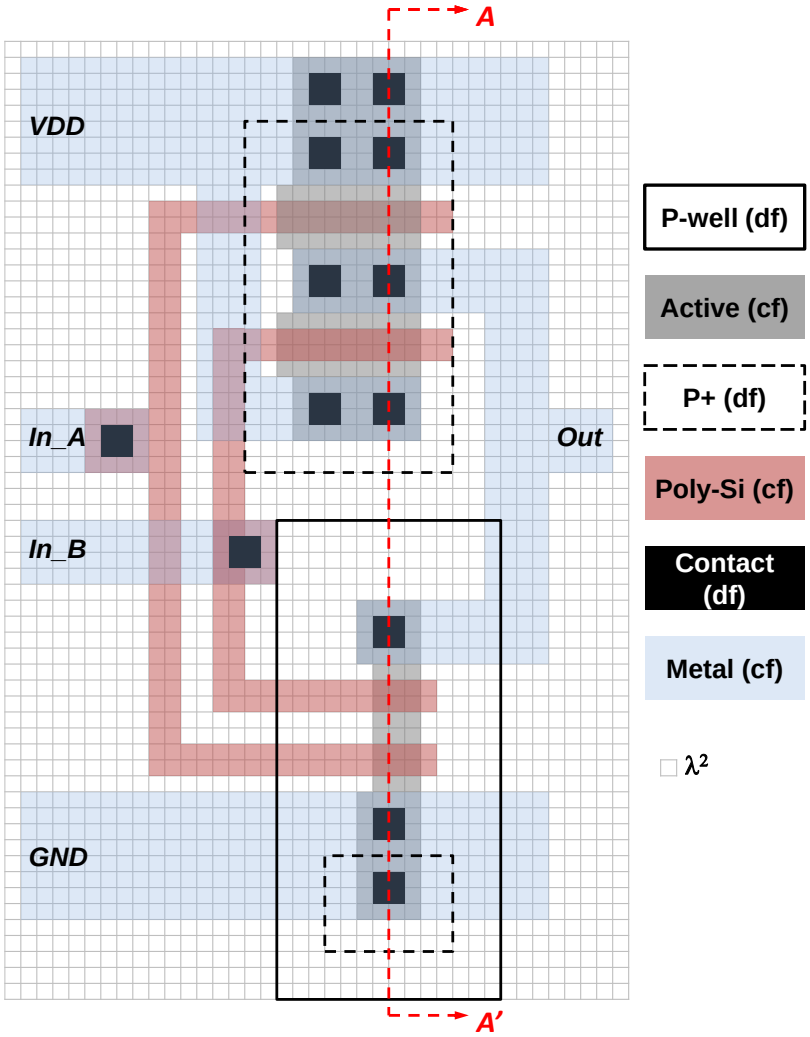
PROBLEM SET #9

Issued: Tuesday, Nov. 11, 2014

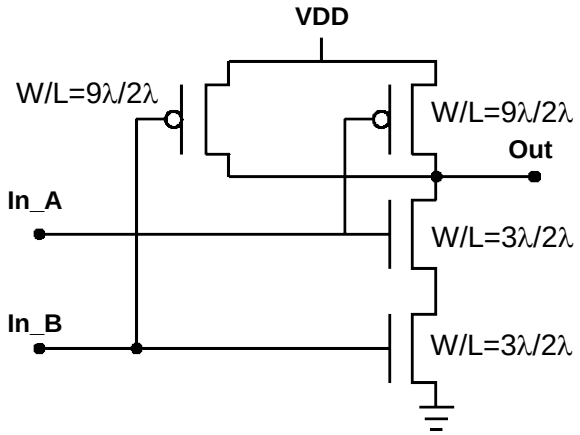
Due: Wednesday, Nov. 19, 2010, 8:00 a.m. in the EE 143 homework box near 140 Cory

1. The following pages comprise an actual pwell CMOS process flow with poly-to-poly capacitors. No details are spared in this flow; even equipment names are given, as are diagnostic steps used to verify each step. LPCVD furnace program names are also given. These details are included to present a more realistic situation. In doing this problem, you must sift through the extraneous information and concentrate on the recipe information (i.e., temperatures, times, implant doses, etc. ...).

   This process flow as applied to the layout below will be the subject of your next few homework assignments. In each of these assignments, you will be asked to answer several questions centered around different points in the process flow.



   a) Draw the circuit schematic implemented by the layout and label the device sizes.



b) Draw a qualitative cross-section corresponding to line *A*-*A*' in the layout above. Identify layers and try to draw thicknesses to scale. (You should distinguish between CVD oxides and thermally grown oxides—i.e., label them.) Note that although capacitors are not used in this layout, you may need to account for the process steps involved with poly-to-poly capacitor formation to get a sufficiently accurate cross-section. (Note that mask layers are identified in the drawing. Again, 'df' = dark field (i.e., box shows where an opening in the PR will be) and 'cf' = clear field (i.e., box shows the portion to be covered by PR).)

c) What is the LOCOS field oxide thickness?

$$X_{ox}^2 + AX_{ox} = Bt + X_i^2 + AX_i$$

$$\frac{B}{A} = 9.7 \times 10^7 * \exp\left(-\frac{2.05}{8.617 \times 10^{-5} \times 1223}\right) = 0.346\ \mu m/hr$$

$$B = 386 * \exp\left(-\frac{0.78}{8.617 \times 10^{-5} \times 1223}\right) = 0.236 \mu m^2/hr$$

After the 4hrs 40mins wet oxidation in Step 13 at 950°C, the LOCOS oxide thickness would be $X_{ox} = 0.762 \mu m$.

d) What is the gate oxide thickness?

Gate oxidation in Step 17 conducts 2 hrs in dry O_2 at 950°C.

$$X_{ox}^2 + AX_{ox} = Bt + X_i^2 + AX_i\ (X_i = 25nm)$$

$$\frac{B}{A} = 3.71 \times 10^6 * \exp\left(-\frac{2}{8.617 \times 10^{-5} \times 1223}\right) = 2.12 \times 10^{-2} \mu m/hr$$

$$B = 7.72 \times 10^2 * \exp\left(-\frac{1.23}{8.617 \times 10^{-5} \times 1223}\right) = 6.59 \times 10^{-3} \mu m^2/hr$$

Then, $A = 0.31 \mu m$.

Plug in the numbers in the oxidation equation above, $X_{ox} = 58.49\ nm$.

e) Estimate the capacitance per unit area of the poly-to-poly capacitor.

Assume polysilicon has the same oxidation rate as <100> Si.

Cap oxidation in Step 20.3 conducts 55/60 hrs in dry O_2 at 950°C.

$$X_{ox}^2 + AX_{ox} = Bt + X_i^2 + AX_i \ (X_i = 25nm)$$

$$\frac{B}{A} = 3.71 \times 10^6 * \exp\left(-\frac{2}{8.617 \times 10^{-5} \times 1223}\right) = 2.12 \times 10^{-2} \mu m/hr$$

$$B = 7.72 \times 10^2 * \exp\left(-\frac{1.23}{8.617 \times 10^{-5} \times 1223}\right) = 6.59 \times 10^{-3} \mu m^2/hr$$

Then, $A = 0.31 \mu m$.

Plug in the numbers in the oxidation equation above, $X_{cap\ ox} = 41\ nm$.

Thus, the capacitance per unit area of the poly-to-poly cap is $\frac{C_{pp\ cap}}{Area} = \frac{\varepsilon_{ox}}{d} = \frac{3.9 \times 8.854 \times 10^{-12}}{41 \times 10^{-9}} = 0.84 mF/m^2$

f) What is the depth of the pwell diffusion at the end of the process?

The initial oxide thickness obtained in step 1 is around 0.12 μm.

	T	B/A	B	A	Xi	tau	t	Xo	(μm)
Dry	1000	0.044783	0.01042	0.232688	0.025	0.618226	0.083333	0.028039	

	T	B/A	B	A	Xi	tau	t	Xo	(μm)
Wet	1000	0.742257	0.315112	0.424533	0.028039	0.040271	0.158333	0.115818	

	T	B/A	B	A	Xi	tau	t	Xo	(μm)
Dry	1000	0.044783	0.01042	0.232688	0.115818	3.873476	0.083333	0.117681	

From Fig. 5.3, 80keV boron implantation energy yields 0.26-μm projected range and 0.06-μm straggle, which means most of the dopants are inside the silicon substrate.

The dopants experience high temperature steps through the entire process, which are summarized below (dominated by the well drive-in of Step 5):

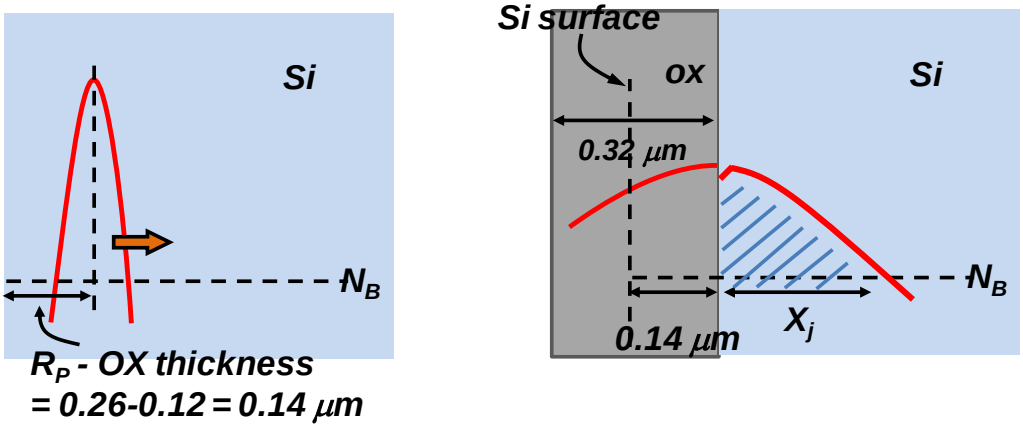
Step	temp	hours	hours	hours	D*t(hr)	D*t(sec)
5	1150	4.000	5.000		8.953E-13	2.90077E-08
6	950	1.000	0.333		6.527E-15	3.13307E-11
13	950	0.083	4.667	0.083	6.527E-15	1.13574E-10
15	950	0.500	0.333		6.527E-15	1.95817E-11
17	950	2.000	0.333		6.527E-15	5.48288E-11
20	950	0.917	0.333		6.527E-15	2.93726E-11
	610	2.500			9.109E-21	8.19803E-17
25	925	1.250			3.143E-15	1.41453E-11
28	450	0.583			1.988E-25	4.17565E-22
	950	0.083	0.333	0.083	6.527E-15	1.1749E-11
35	400	0.333			2.44E-27	2.92846E-24
	1100	5.000			2.992E-13	5.38648E-09
sum						2.92823E-08

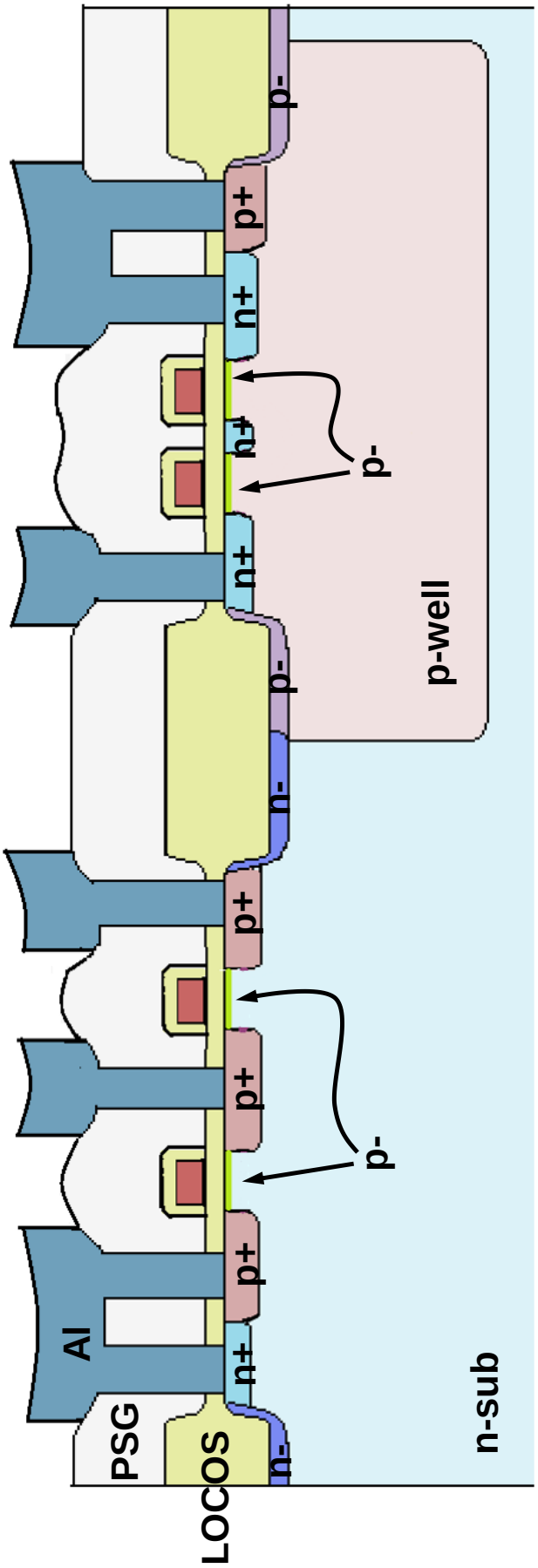
The background concentration of the n-type wafers is around $4 \times 10^{14}/cm^3$ which could be obtained in Fig. 4.8 with a resistivity of 10 ohm-cm.

During the first 4-hr drive-in step in oxygen, a 320-nm thick oxide would grow on the surface that means the interface between oxide and Si would move to the right by around 140 nm, where the peak of the doping concentration is. The dopants to the left of the peak would diffuse into oxide during oxidation and pile up since the diffusion coefficient of boron in oxide is small. So the one-sided diffusion expression is used here with approximately half the implanted dose. The junction depth from the location of peak concentration is

$$X_j = 2 \times \sqrt{Dt * \ln\left(\frac{N_o}{N_B}\right)} = 2\sqrt{Dt * \ln\left(\frac{Q}{\sqrt{\pi Dt} N_B}\right)} =$$

$$2\sqrt{2.93 \times 10^{-8} \ln\left(\frac{1.5\times10^{12}}{\sqrt{\pi \cdot 2.93\times10^{-8} \cdot 4\times10^{14}}}\right)} = 5.43\ \mu m.$$




p-
p+
n+
p-
p-well
n-
p+
p+
p-
p+
n+
Al
PSG
LOCOS
n-
n-sub