EE143 – Fall 2016
Microfabrication Technologies

Lecture 9: Metallization
Reading: Jaeger Chapter 7

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Interconnect
Multilevel Metallization

Interconnect RC Time Delay

- Interconnect circuit parameters are often normalized by length
  - Both resistance and capacitance are proportional to wire length
- Resistance per unit length:
  \[ R_I = \frac{R}{L} = \frac{\rho}{W_m T_m} \]
- Interconnect-substrate capacitance per unit length:
  \[ C_{sub} = \frac{C}{L} = \frac{\varepsilon_{ox} W_m}{T_{ox}} \]
- Interconnect-interconnect capacitance per unit length:
  \[ C_L = \frac{C}{L} = \frac{\varepsilon_{ox} T_m}{S_m} \]
Interconnect Requirements

- Low Ohmic resistance
  - interconnects material has low resistivity
- low contact resistance to semiconductor device
- Long-term reliability

Resistivity of Metals

<table>
<thead>
<tr>
<th>TABLE 7.1</th>
<th>Bulk Resistivity of Metals (μΩ-cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Commonly Used Metals</td>
</tr>
<tr>
<td>Ag: Silver</td>
<td>Aluminum</td>
</tr>
<tr>
<td>Al: Aluminum</td>
<td>2.65</td>
</tr>
<tr>
<td>Au: Gold</td>
<td>Titanium</td>
</tr>
<tr>
<td>Co: Cobalt</td>
<td>Tungsten</td>
</tr>
<tr>
<td>Cu: Copper</td>
<td>Copper</td>
</tr>
<tr>
<td>Mo: Molybdenum</td>
<td>5</td>
</tr>
<tr>
<td>Ni: Nickel</td>
<td>Less Frequently Utilized</td>
</tr>
<tr>
<td>Pd: Paladium</td>
<td>10</td>
</tr>
<tr>
<td>Pt: Platinum</td>
<td>10.6</td>
</tr>
<tr>
<td>Ti: Titanium</td>
<td>50</td>
</tr>
<tr>
<td>W: Tungsten</td>
<td></td>
</tr>
</tbody>
</table>

Ohmic Contact Formation

- Aluminum to p-type silicon forms an Ohmic contact [Remember Al is p-type dopant]
- Aluminum to n-type silicon can form a rectifying contact (Schottky barrier diode)
- Aluminum to n+ silicon yields a tunneling contact

Contact Resistance $R_c$

For a uniform current density flowing across the contact area:

$$R_c = \frac{\rho_c}{\text{Contact Area}}$$

- $\rho_c$ of Metal-Si contacts $\sim 10^{-6}$ to $10^{-7} \ \Omega \cdot \text{cm}^2$
- $\rho_c$ of Metal-Metal contacts $< 10^{-8} \ \Omega \cdot \text{cm}^2$
Contact Resistivity $\rho_c$

- Specific contact resistivity

$$\rho_c = \left( \frac{\partial J}{\partial V} \right)^{-1} = \rho_{c0} \exp \left[ \frac{2 \sqrt{m^* \epsilon_s}}{\hbar} \left( \frac{\phi_B}{\sqrt{N}} \right) \right]$$

$\phi_B$ is the Schottky barrier height

$N$ = surface doping concentration

$\rho_c$ = specific contact resistivity in ohm-cm$^2$

$m$ = electron mass

$\hbar$ = Planck’s constant

$\epsilon_s$ = Si dielectric constant

- Approaches to lowering of contact resistance:
  - Use highly doped Si as contact semiconductor
  - Choose metal with lower Schottky barrier height

Aluminum Spiking and Junction Penetration

- Aluminum spiking:
  - Si absorption into the aluminum results in Al spikes
  - Short-circuit junctions or cause excess leakage

- To prevent Al spiking
  - Barrier metal deposited prior to metallization
  - Sputter deposition of Al with 1% Si
Alloying of Contacts

- Alloy to obtain very low contact resistivity
- Specific contact resistivity
  \[ \rho_c = 1.2 \times 10^{-6} \Omega \cdot cm^2 \]
- Contact resistance
  \[ R_c = \frac{\rho_c}{A} \]
  $A$: contact area

Electromigration

- High current density causes voids to form in interconnections
- “Electron wind” causes movement of metal atoms
Electromigration

- Copper added to aluminum to improve lifetime (Al with 4% Cu, 1% Si)
- Mean time to failure (MTF)
  \[ MTF \propto \frac{1}{J^2 \exp \left( \frac{E_A}{kT} \right)} \]
  - \( J \): current density
  - \( E_A \): activation energy
- Heavier metals (e.g., Cu) have higher activation energy

Metal Deposition Techniques

- Sputtering has been the technique of choice
  - High deposition rate
  - Capability to deposit complex alloy compositions
  - Capability to deposit refractory metals
  - Uniform deposition on large wafers
  - Capability to clean contact before depositing metal
- CVD processes have recently been developed
  - (e.g. for W, TiN, Cu)
  - Better step coverage
  - Selective deposition is possible
  - Plasma enhanced deposition is possible for lower deposition temperature
Metal CVD Processes

- TiN
  - Used as barrier-metal layer
  - Electrical resistivity ~ 10 to 100 \( \mu \Omega \cdot cm \)
- Deposition processes:

  \[
  6 \text{TiCl}_4 + 8 \text{NH}_3 \rightarrow 6 \text{TiN} + 24 \text{HCl} + \text{N}_2
  \]

  \[
  2 \text{TiCl}_4 + 2 \text{NH}_3 + \text{H}_2 \rightarrow 2 \text{TiN} + 8 \text{HCl}
  \]

  \[
  2 \text{TiCl}_4 + \text{N}_2 + 4 \text{H}_2 \rightarrow 2 \text{TiN} + 8 \text{HCl}
  \]

Electroplating

https://en.wikipedia.org/wiki/Electroplating
**Dual Damascene Process**

(a) Via resist
(b) Metal resist
(c) Etch stop (SiN₂)
(d) Barrier layer (TiN)

**Salicides**

- Self-aligned silicide on silicon and polysilicon
- Often termed “Salicide”
Properties of Silicides

<table>
<thead>
<tr>
<th>Silicide</th>
<th>Starting Form</th>
<th>Sintering Temperature (°C)</th>
<th>Lowest Binary Eutectic Temperature (°C)</th>
<th>Specific Resistivity (μohm-cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CoSi$_2$</td>
<td>Metal on polysilicon</td>
<td>900</td>
<td>1195</td>
<td>18–25</td>
</tr>
<tr>
<td></td>
<td>Cosputtered alloy</td>
<td>900</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HfSi$_2$</td>
<td>Metal on polysilicon</td>
<td>900</td>
<td>1300</td>
<td>45–50</td>
</tr>
<tr>
<td>MoSi$_2$</td>
<td>Cosputtered alloy</td>
<td>1000</td>
<td>1410</td>
<td>100</td>
</tr>
<tr>
<td>NiSi$_2$</td>
<td>Metal on polysilicon</td>
<td>900</td>
<td>966</td>
<td>50</td>
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<tr>
<td></td>
<td>Cosputtered alloy</td>
<td>900</td>
<td></td>
<td>50–60</td>
</tr>
<tr>
<td>Pd$_3$Si</td>
<td>Metal on polysilicon</td>
<td>400</td>
<td>720</td>
<td>30–50</td>
</tr>
<tr>
<td>PtSi</td>
<td>Metal on polysilicon</td>
<td>600–800</td>
<td>830</td>
<td>28–35</td>
</tr>
<tr>
<td>TaSi$_2$</td>
<td>Metal on polysilicon</td>
<td>1000</td>
<td>1385</td>
<td>35–45</td>
</tr>
<tr>
<td></td>
<td>Cosputtered alloy</td>
<td>1000</td>
<td></td>
<td>50–55</td>
</tr>
<tr>
<td>TiSi$_2$</td>
<td>Metal on polysilicon</td>
<td>900</td>
<td>1330</td>
<td>13–16</td>
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<tr>
<td></td>
<td>Cosputtered alloy</td>
<td>900</td>
<td></td>
<td>25</td>
</tr>
<tr>
<td>WSi$_2$</td>
<td>Cosputtered alloy</td>
<td>1000</td>
<td>1440</td>
<td>70</td>
</tr>
<tr>
<td>ZrSi$_2$</td>
<td>Metal on polysilicon</td>
<td>900</td>
<td>1355</td>
<td>35–40</td>
</tr>
</tbody>
</table>

Low-K Dielectric

- Reduce parasitic capacitances by replacing silicon dioxide with a low-dielectric constant (low-K) materials:

\[ C_{sub} = \frac{C}{L} = \frac{\varepsilon_{low-K}W_m}{T_{ox}} \]

\[ C_L = \frac{C}{L} = \frac{\varepsilon_{low-K}T_m}{S_m} \]
Approaches for Low-K Dielectric Materials

Materials with lower polarizability

Silica
SSQ
Polymer

Low-k materials

Non-Si

Si-based

Si-F or Si-C bonds have lower polarizability than SiO bond

Organic polymers with virtually nonpolar bonds, C-C or C-H

Higher porosity (Lower Density)

0 20 40 60 80 100
Porosity (%)

1 2 3 4
Dielectric constant

Current integration efforts


Silica-Based Low-K Materials

SIOCH material with an oxygen atom replaced by a CH₃ group reduces the k value by introducing a less polar bond and by creating additional free volume (constitutive porosity).

SiO₂

SiOCH

Silica-based

SSQ-based

Silsesquioxane (SSQ)

Silsesquioxane (SSQ)