UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

Professor Ali Javey
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MICROFABRICATION TECHNOLOGY
EECS143, Spring 2008

T.A.s:

SangHoon Lee: leesh@me.berkeley.edu (head TA)
Peter Matheu: peter_matheu@berkeley.edu
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LECTURES

Tu-Th 3:30-5:00 pm, 3108 ETCHEVERRY

LAB SECTIONS

M 2-5P, 218 CORY
W 9-12P, 218 CORY
Th 11-2P, 218 CORY
F 9-12P, 218 CORY

Each student must attend one of these laboratory sections

OFFICE HOUR

Professor and T.A.s' office hour will be announced on EE143 homepage.

TEXT

Introduction to Microelectronic Fabrication
R. C. Jaeger
Prentice Hall

REFERENCES (On reserve at the Engineering Library)

Semiconductor Device Fundamentals
R. F. Pierret
Addison Wesley

Device Electronics for Integrated Circuits
R. S. Muller and T. I. Kamins
Wiley

COURSE DESCRIPTION

EE143 teaches the fundamentals of integrated-circuit (IC) fabrication and surface-micromachining technology, giving the student a basic understanding of IC and micromachining processes and the effect of processing choices on device performance. Students learn to use process simulation tools and also fabricate and characterize devices in the laboratory. This lecture part will cover the processing techniques and design methodologies of microfabrication. We will discuss the process modules: lithography, thermal oxidation, diffusion, ion implantation, etching, thin-film deposition, epitaxy, metallization. The second part of the course will cover process simulation, layout design rules, MOS, IC, and MEMS process integration. The laboratory part of the course will provide students opportunities to have hands-on experience to fabricate and characterize a NMOS chip with simple MEMS components.

PREREQUISSITES

EE40/E100 and Physics 7B or equivalent

CONTENTS:

A. Course Overview (1 week)
B. Overview of Semiconductor Materials and Devices (2-3 weeks)
C. Thermal Oxidation (1 week)
D. Ion Implantation (1 week)
E. Diffusion (1 week)
F. Lithography (1 week)
G. Thin Film Deposition (1 week)
H. Etching (1 week)
I. Metallization/Planarization (1 week)
J. Layout & Process Integration (1 week)
K. Nanotechnology and Nanofabrication (1 lecture)

HOMEWORK, EXAM & GRADES

Homework will be assigned every Tuesday and will be due the following Tuesday in class. Discussion and collaboration, as opposed to copying, of homework is encouraged. In other words, you are encouraged to discuss the homework with your classmates but you must write your own derivations and do your own calculations, etc. We encourage cooperation rather than competition. Copying someone else's work is considered cheating and will result in severe consequences.

Percentages are as follows:

Homework	10%
Three Exams	30% (10% each)
Lab (quizzes, lab work, reports)	30%
Final Exam	30%

EECS Department Policy on Academic Dishonesty:

http://www.eecs.berkeley.edu/Policies/acad.dis.shtml

EE 130 Home Page:

http://www-inst.eecs.berkeley.edu/~ee143/