INFORMATION ABOUT THE FINAL EXAM

Extra Office Hours: (in addition to regular office hours)

Jack Yaung	10:30-12 noon on Thursday, May 6
Yenhao Chen	10:30-12 noon on Friday, May 7
Wei-Chang Li	2-3:30 p.m. on Friday, May 7
Jaewon Jang	4:30-6 p.m. on Friday, May 7

Date of Exam:

Monday, May 10, 11:30-2:30 p.m. (sharp)

Place:

102 Moffitt

General Information:

The exam will be closed book, but you will be allowed two 8.5″×11″ sheets on which you can write anything you would like (on both sides). Bring a calculator to the exam. You will be provided with exam sheets with enough space to put all your work on these sheets. You should show and include all your work on the exam sheets.

Material to be Covered:

Reading in Jaeger, class lecture notes, handouts, lab reports, and homeworks. The exam is meant to include all material covered so far in the class. You might pay more attention to the following areas:

1. Basic fabrication process modules, including oxidation, film deposition, lithography, etching, ion implantation, and diffusion. You should understand these to the point of being able to draw cross sections from a given process flow, or vice versa.
2. Process integration, including transistor process flows (e.g., NMOS), MEMS process flows, dark or clear field masks, mask ordering and alignment sequences, drawing cross-sections from given process flows, and vice versa.
3. Lithography, including resolution, mask-to-wafer variations (e.g., due to temperature changes), photoresist types, and contact vs. proximity vs. projection printing.
4. Oxidation, including oxidation modeling, oxidation graphs and their use, phenomena that influence the rate of oxidation, and dopant redistribution during oxidation.
5. Film deposition, including evaporation, sputtering, chemical vapor deposition, epitaxy, atomic layer deposition, and electroplating. Be able to determine whether or not a given deposition is conformal.
6. Details of etching, including anisotropy and selectivity, the influence of topography, the mechanisms behind wet and dry etching, ion milling, plasma etching, reactive ion etching, and chemical mechanical polishing. Be able to draw final cross-sections after exposing a given cross-section to etching for a specific amount of time.

7. Ion implantation, including statistical modeling, masking, and junction depth.
8. Dopant diffusion, including pre-deposition, drive-in, junction depth, Irvin's curves, sheet resistance, and the effect of successive high temperature steps.
9. Methods for determining junction depth given a fabrication process flow.
10. Advanced MOS device needs, including advanced isolation strategies and methods to avoid punchthrough.
11. Methods for determining threshold voltages, including factors that influence it, the impact of implant dose and depth, and its dependence upon body bias voltage.
12. Device Characterization, including the procedure and reasoning behind the measurements and extractions discussed in lecture and performed in lab.
13. Latchup, including identification of important parasitic devices that induce it and methods for suppressing it.
14. Ability to understand quickly a complete (and realistic) process traveler for a microfabricated device, e.g., a transistor or a MEMS device, and predict its cross-sections, governing parameters, and device performance characteristics.