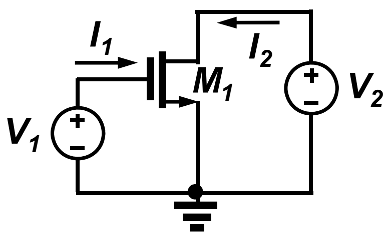
PROBLEM SET #1

Issued: Thursday, Jan. 28, 2010

Due: Thursday, Feb. 4, 2010, 7:00 p.m. in the EE 143 homework box in 240 Cory

I. MOSFET Characteristics

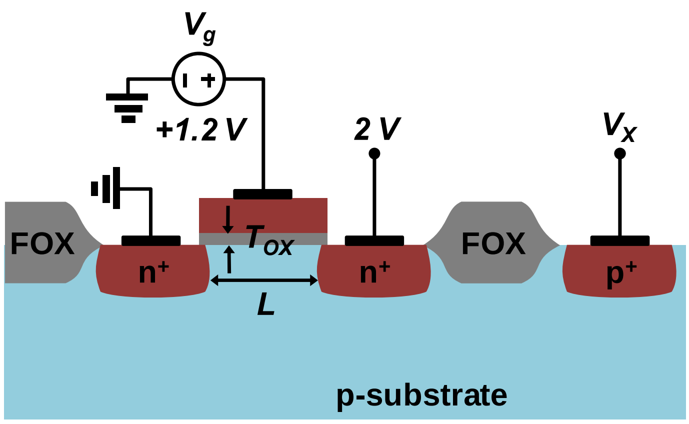
1. Consider the following circuit. Assume transistor M_1 is in saturation and that its bias voltages, V_1 and V_2, process parameter K ($=\mu_n C_{OX}$), and threshold voltage V_{TH} can be changed independently. Indicate in the table how an *increase* in each of these parameters changes the gate current I_1, the drain current I_2, the small-signal transconductance g_m, and the small-signal output resistance r_d of M_1. Use symbols: ↑ for increase, ↓ for decrease, -- for no change.



	I_1	I_2	g_m	r_d
V_1↑				
V_2↑				
K↑				
V_{TH}↑				

2. Consider the cross-section shown below for an NMOS device under dc biasing where the supply voltage $V_{DD} = 2V$, and the gate bias $V_G = 1.2V$.

Assume $L = 0.5\ \mu m, W = 50\ \mu m, T_{OX} = 9\ nm, 2\Phi_F = 0.8\ V, V_{TH0} = 0.7V,$ $substrate\ doping = 9 \times 10^{14}\ cm^{-3}, relative\ permittivity\ of\ Si = 11.8,$ $and\ of\ SiO_2 = 3.9, channel\ mobility = 350\ cm^2/V/S.$



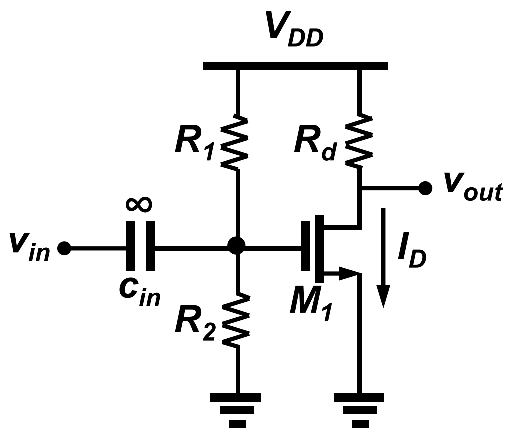
a. Calculate the threshold voltage if $V_X = V_{DD} = 2V$.

b. (Continued) Compared to V_{TH0}, does the threshold voltage increase or decrease? Is this desirable? Why or why not?

c. Plot drain current versus V_X if V_X varies from -∞ to 0.

II. MOSFET Amplifier

3. Consider the MOSFET amplifier given below, where $I_{DS} = \frac{K}{2}(V_{GS} - V_T)^2, V_{DD} = 5V, R_d = 2k\Omega, K = 1\,mA/V^2$, and $V_{TH} = 1V$.



a. Derive an expression for the transistor dc bias point (i.e., dc bias voltage) at the gate terminal as a function of V_{DD}, R_1 and R_2.

b. Determine the required ratio of R_1/R_2 such that the MOSFET transconductance $g_m = 1mA/V$.

c. What is the dc bias voltage at the output V_{out}?

d. Draw the small-signal model for the amplifier. Write an expression for its gain v_{out}/v_{in} and calculate its numerical value. Clearly label the components and input/output.

III. Fabrication Yield/Cost

4. The cost of processing a wafer in a particular process is \$1,000. Assume that 35% of the fabricated dice are good. For this problem, use Fig. 1.1(c) in the textbook to determine the number of dice.

a. Determine the cost per good die for a 150 mm wafer.

b. Repeat for a 200 mm wafer.