PROBLEM SET #10

Issued: Tuesday, Apr. 20, 2010

Due: Tuesday, Apr. 27, 2010, 7:00 p.m. in the EE 143 homework box in 240 Cory

1. Referring to the layout and process flow in HW#8, answer the following questions.
   a) What is the threshold voltage V_{tn} for the NMOS devices of this process for zero source-to bulk voltage, V_{SB}=0? Assume that the fixed charge in the gate oxide is negligible. (Note that this may or may not be a good assumption. Don't be surprised if you get a strange value for V_{tn}.)
   b) What is the threshold voltage V_{tp} for the PMOS devices of this process for zero source-to-bulk voltage, V_{SB}=0? Assume that the fixed charge in the gate oxide is negligible. (Note that this may or may not be a good assumption. Don't be surprised if you get a strange value for V_{tp}.)
   c) Calculate $k_n'=\mu_n C_{ox}$ and $k_p'=\mu_p C_{ox}$ for this process.
   d) Assuming the pwell is tied to ground, what is the minimum value of voltage on a metal line over the field region in the pwell that would invert the pwell surface?
   e) Assuming the nwell is tied to V_{DD}=5V, what is the maximum value of voltage on a metal line over the field region in the nwell that would invert the nwell surface?
   f) What is the value of capacitance per unit area for the poly-to-poly capacitors?