

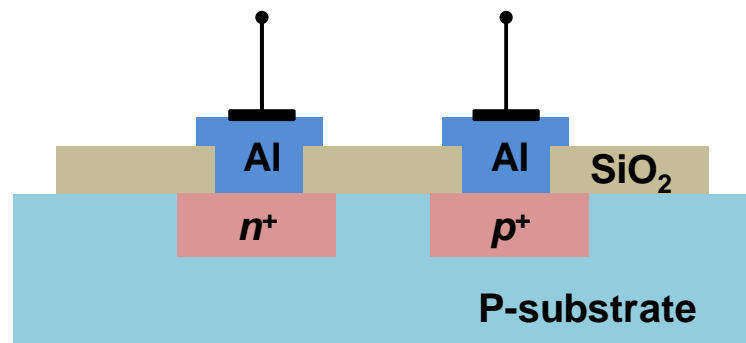
PROBLEM SET #2

Issued: Thursday, Feb 4, 2010

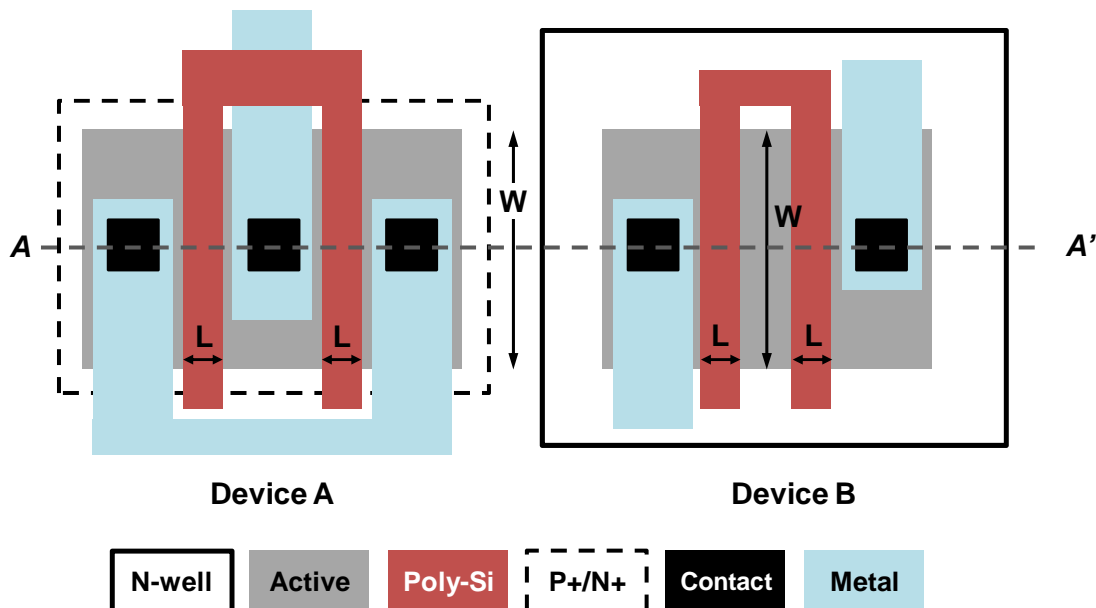
Due: Thursday, Feb. 11, 2010, 7:00 p.m. in the EE 143 homework box in 240 Cory

I. Process Flow/Layout to Cross-Section

1. Consider the cross-section of a device shown below:
 - a. What kind of device is this?
 - b. Generate a possible process flowchart for fabrication of this structure. Use a form like the cross-sections in Figure 1.6 in Jaeger's textbook.



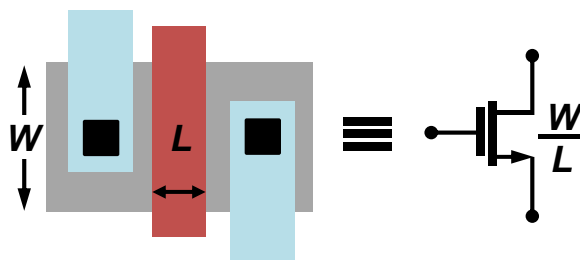
2. Consider the following layout of two MOSFET devices and the corresponding process flow:



The process flow

- | | |
|--|---|
| 1) Silicon oxidation: target = 300nm | 20) Dry etch polysilicon |
| 2) Lithography: Mask I (N-well) | 21) Remove PR |
| 3) Etch SiO_2 | 22) Lithography: Mask IV (n+ implant)(dark field) |
| 4) Remove PR | 23) D/S ion implantation: P (n-type) |
| 5) N-well diffusion: P (n-type) | 24) Remove PR |
| 6) Etch SiO_2 | 25) Lithography: Mask V (p+ implant)(clear field) |
| 7) Silicon oxidation: target = 100nm | 26) D/S ion implantation: B (p-type) |
| 8) LPCVD Si_3N_4 : target = 500nm | 27) Remove PR |
| 9) Lithography: Mask II (Active) | 28) Anneal at 1050°C to activate dopants and drive-in diffusion |
| 10) Etch Si_3N_4 | 29) LPCVD PSG: target = 1 μm and reflow at 950°C |
| 11) Etch SiO_2 | 30) Lithography: Mask VI (contact) |
| 12) Field isolation implant: B+ (p-type) | 31) Etch SiO_2 down to S/D regions |
| 13) Remove PR | 32) Remove PR |
| 14) Grow 1 μm of SiO_2 thermally (LOCOS oxidation) | 33) Deposit Al: sputtering target = 1 μm |
| 15) Etch Si_3N_4 | 34) Lithography: Mask VII (metal) |
| 16) Etch SiO_2 | 35) Dry etch Al |
| 17) Dry oxidation for gate oxide: target = 100nm | |
| 18) LPCVD situ phosphorous-doped gate polysilicon: target = 350nm | |
| 19) Lithography: Mask III (Poly) | |

- Plot the cross-sections along AA' plane through step 6), 14), 21), 26) and 35).
- A MOSFET device can be represented by a circuit symbol view, e.g., a NMOS device layout can be depicted as:



Draw the circuit schematics implemented by each device layout in A and B. Then, for each of A and B, equate the circuit to an equivalent single device and redraw the layout so that it realizes the corresponding single device.