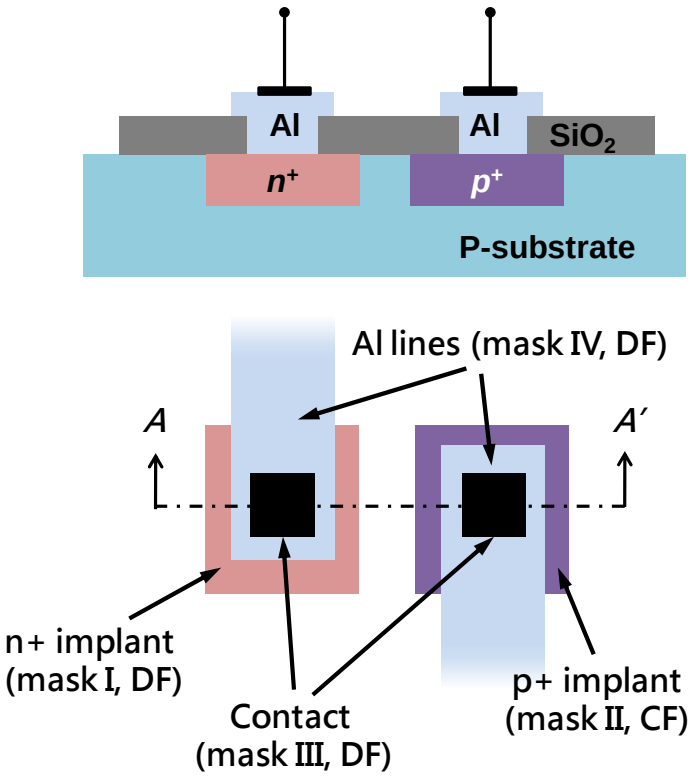
PROBLEM SET #4

Issued: Thursday, Feb. 18, 2010

Due: Thursday, Feb. 25, 2010, 7:00 p.m. in the EE 143 homework box in 240 Cory

1. In HW#2, you created a process flow for fabricating a *pn* diode of which the cross-section and the four-layer layout are shown below:



DF: dark field CF: clear field

Process flow

1) Lithography of n+ implant (mask I, **dark field**).
2) Ion implantation: P (n-type).
3) Remove photoresist.
4) Lithography of p+ implant (mask II, **clear field**).
5) Ion implantation: B (p-type).
6) Remove photoresist.

7) Silicon oxidation: target = 300nm
8) Lithography of contact (mask III, **dark field**).
9) Etch SiO_2.
10) Remove photoresist.
11) Sputter Al: target = 500nm.
12) Lithography of Al lines (mask III, **dark field**).
13) Etch Al.
14) Remove photoresist.

*each lithography step consists of spin, expose and develop photoresist.

a. What type of photoresist (positive or negative) must be used on each of the four lithography steps?
b. In order to pattern Al metal lines, the "lift-off" process may be used instead of using the etching process described in step 11) to 14). Replace step 11) to 14) described above with the two-layer photoresist lift-off process shown as below:

   i. Spin on 1.1 μm g-line photoresist.
   ii. Expose without any mask.
   iii. Spin on 1.1 μm g-line photoresist.
   iv. Contact lithography (mask IV, **dark field**): expose and develop.
   v. Evaporate Al: target = 500 μm.
   vi. Remove photoresist in acetone.

   Draw the cross-sections along AA' plane through step **iv**, **v** and **vi**. (Ignore the patterns made prior to the metal definition, i.e., start with a blank wafer for the lift-off process)

2. Problem 3.2, 3.8, 3.10, 3.12 in the textbook (Jaeger).