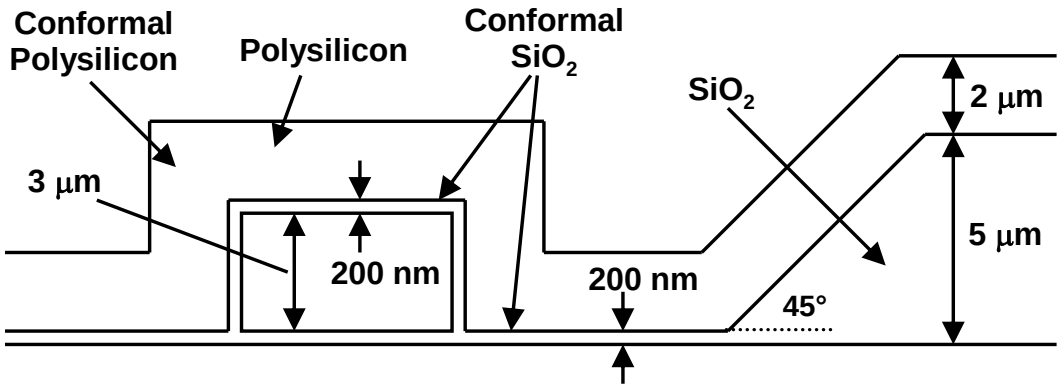
PROBLEM SET #6

Issued: Thursday, Mar. 4, 2010

Due: ~~*Thursday, Mar. 11*~~*, 2010*, 7:00 p.m. in the EE 143 homework box in 240 Cory
Tuesday, Mar. 16

Note: Problem 4 and 5 are added at *Mar. 9*.

1. The cross-section below is to be etched via reactive ion etching (RIE). For this problem, assume that the RIE etch is 100% anisotropic and that it etches polysilicon at the rate of 1 μm/min and has a silicon-to-oxide selectivity of 5:1. Draw cross-sections of the structure after etching for (a) 2 min.; (b) 5 min.; and (c) 6 min.



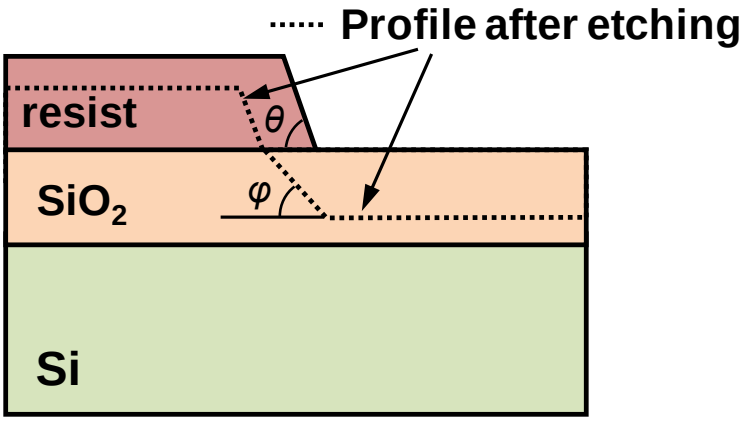
2. Suppose you want to etch the oxide layer shown in the cross-section below using reactive ion etching (RIE). Assume that the resist has an initial slope of angle θ, and the etch rates in the RIE system are defined as follows:

   Vertical etch rate of oxide: V_{OV} = 100nm/min
   Lateral etch rate of oxide: V_{OL} = 10nm/min
   Vertical etch rate of resist: V_{RV} = 100nm/min
   Lateral etch rate of resist: V_{RL} = 50nm/min

   a) Express φ in terms of θ, V_{OV}, V_{OL}, V_{RV} and V_{RL}.

   b) Assume that all the etch rates have a variation of ±10%. If $\theta = 80°$, what are the maximum and minimum values of φ?

c) If the etch rates of resist both are reduced to 10% of the original values, what is the value of φ? Does the slope of oxide become steeper? (Again, $\theta = 80°$)



3. You are doing the step of polysilicon gate lithography and etching in the lab. The polysilicon is 350 nm with a variation of ±10% across the wafer and the etch rate of polysilicon in Si etchant also has a ±10% variation.

a) How much overetch in percentage of etch time is required to ensure all polysilicon on the wafer is removed?

b) The mask has four NMOS devices with varying gate lengths, 4 μm, 6 μm, 8 μm and 10 μm. Assume that there is no patterning error during the lithography, i.e., the photoresist patterns have exactly the same sizes as the drawings on the mask. Fill in the table below to summarize the worst-case shortest gate lengths on the wafer obtained after the overetch calculated in a) for each of the four devices; and to provide estimates for the DC current variations ($\frac{I - I_{nominal}}{I_{nominal}} \times 100\%$) due to the overetch for each case. (Assume that Si etchant does not etch the underlying thin oxide.)

Gate length	4 μm	6 μm	8 μm	10 μm
Shortest length after overetch				
DC current variation				

4. Problem 5.2 in the textbook (Jaeger).
5. Problem 5.4 in the textbook (Jaeger).