PROBLEM SET #9

Issued: Tuesday, Apr. 13, 2010

Due: Tuesday, Apr. 20, 2010, 7:00 p.m. in the EE 143 homework box in 240 Cory

1. Referring to the layout and process flow in HW#8, answer the following questions.
   a) Why did we etch the oxide before well drive-in in step 5.2?
   b) Why did we do a backside etch in step 31?
   c) Identify all control wafers in the process and explain what they are used for.
   d) What is the total thickness of oxide over the field regions?
   e) What is the depth x_{jn} of the NMOS n+ S/D junctions at the end of the process?
   f) What is the depth x_{jp} of the PMOS p+ S/D junctions at the end of the process?
   g) What is the gate-overlap capacitance (i) for NMOS devices? (ii) for PMOS devices?