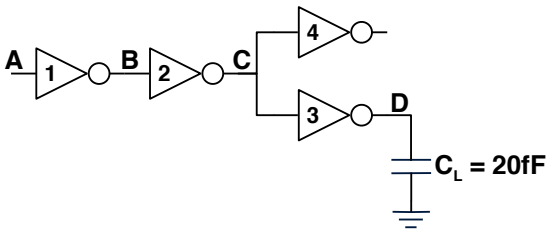
EE 16B Designing Information Devices and Systems II
Fall 2015 Section 5B

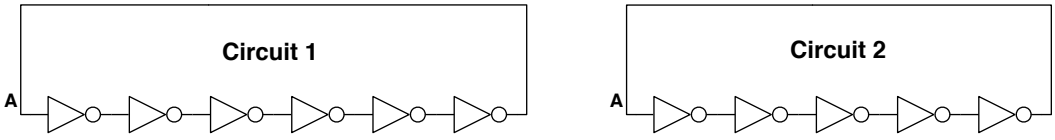
1. Non-Uniform Delays



Find the delay from point A to point D in the circuit shown above for both rising and falling transitions at point A. Assume the following R and C values:

Inverter	$R_{ON,N}$	$R_{ON,P}$	$C_{gate,N}$	$C_{gate,P}$
1	8.5kΩ	10kΩ	0.2fF	0.4fF
2	2.5kΩ	3kΩ	0.6fF	1.2fF
3,4	1kΩ	1.2kΩ	2.5fF	5fF

2. Ring Oscillators



(a) Describe the behavior of each circuit drawn above. Assume node A is initially 0.

(b) Circuit 2 is called a *ring oscillator* or RO. If each inverter in this circuit has $R_{ON,N} = R_{ON,P} = 5\text{k}\Omega$ and $C_{gate,N} = C_{gate,P} = 0.5\text{fF}$, at what frequency will node A oscillate?

3. Ring Oscillators, Really

In reality, it would be difficult to design transistors with the parameters given above because pMOS devices tend to be 1.5-3x weaker than nMOS devices of the same size. (This is because electrons, the charge carriers for nMOS devices, have a higher *mobility* than holes, the charge carriers for pMOS devices.) Let's investigate options for a more realistic ring oscillator.

(a) First, we'll try leaving the nMOS and pMOS the same size. Using the same nMOS characteristics as Question 2, use $R_{ON,P} = 10\text{k}\Omega$ and $C_{gate,P} = 0.5\text{fF}$ to find the new oscillation frequency of the RO.

(b) Next, we'll increase the size of the pMOS to match the nMOS drive strength. Using the same nMOS characteristics as Question 2, use $R_{ON,P} = 5\text{k}\Omega$ and $C_{gate,P} = 1\text{fF}$ to find the new oscillation frequency of the RO.

(c) If we wanted to use the RO design from part (b) to generate a 1GHz clock, approximately how many inverter stages would be required?