Solutions: Provided by John Noonan.

1. Non-Uniform Delays

Find the delay from point A to point D in the circuit shown above for both rising and falling transitions at point A. Assume the following $R$ and $C$ values:

<table>
<thead>
<tr>
<th>Inverter</th>
<th>$R_{ON,N}$</th>
<th>$R_{ON,P}$</th>
<th>$C_{gate,N}$</th>
<th>$C_{gate,P}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8.5kΩ</td>
<td>10kΩ</td>
<td>0.2fF</td>
<td>0.4fF</td>
</tr>
<tr>
<td>2</td>
<td>2.5kΩ</td>
<td>3kΩ</td>
<td>0.6fF</td>
<td>1.2fF</td>
</tr>
<tr>
<td>3,4</td>
<td>1kΩ</td>
<td>1.2kΩ</td>
<td>2.5fF</td>
<td>5fF</td>
</tr>
</tbody>
</table>

Solutions:
Rising at A (A high voltage at A):
$t_{A\rightarrow B} = 8.5k\Omega \times 1.8fF \times \ln(2) = 10.61\text{ps}$
$\ t_{B\rightarrow C} = 3k\Omega \times 15fF \times \ln(2) = 31.2\text{ps}$
$\ t_{C\rightarrow D} = 1k\Omega \times 20fF \times \ln(2) = 13.86\text{ps}$
Thus, $t_{A\rightarrow D} = 55.67\text{ps}$

Falling at A (A low voltage at A):
$t_{A\rightarrow B} = 10k\Omega \times 1.8fF \times \ln(2) = 12.48\text{ps}$
$\ t_{B\rightarrow C} = 2.5k\Omega \times 15fF \times \ln(2) = 26.0\text{ps}$
$\ t_{C\rightarrow D} = 1.2k\Omega \times 20fF \times \ln(2) = 16.64\text{ps}$
Thus, $t_{A\rightarrow D} = 55.12\text{ps}$

2. Ring Oscillators
(a) Describe the behavior of each circuit drawn above. Assume node A is initially 0.

**Solutions:**

Circuit 1: Because there are an EVEN number of inverters, each node would stay at a fixed voltage – not a ring oscillator.

Circuit 2: Because there are an ODD number of inverters, circuit 2 creates a ring oscillator. We need an ODD number of inverters to create a ring oscillator.

(b) Circuit 2 is called a ring oscillator or RO. If each inverter in this circuit has \(R_{ON,N} = R_{ON,P} = 5k\Omega\) and \(C_{gate,N} = C_{gate,P} = 0.5fF\), at what frequency will node A oscillate?

**Solutions:** Equation: \(\tau = R \times C \times \ln(2)\)

\[R_{ON,N} = R_{ON,P} = 5k\Omega\] and \(C_{gate,N} = C_{gate,P} = 0.5fF\).

The frequency will oscillate at \(f = \frac{1}{2\tau}\) where \(\tau\) is the time delay at each node and \(n\) is the number of nodes (inverters). \(R_{ON,N} = R_{ON,P}\) the resistance at the output each node will be the same. The capacitance at the input of each node will also be the same \((C_{gate,N} + C_{gate,P})\).

Thus, \(\tau = 5k\Omega \times (0.5 + 0.5) fF \times \ln(2) = 3.47ps\), so \(f = \frac{1}{2 \times 3.47ps} = 28.9GHz\).

3. Ring Oscillators, Really

In reality, it would be difficult to design transistors with the parameters given above because pMOS devices tend to be 1.5-3x weaker than nMOS devices of the same size. (This is because electrons, the charge carriers for nMOS devices, have a higher mobility than holes, the charge carriers for pMOS devices.) Let’s investigate options for a more realistic ring oscillator.

(a) First, we’ll try leaving the nMOS and pMOS the same size. Using the same nMOS characteristics as Question 2, use \(R_{ON,P} = 10k\Omega\) and \(C_{gate,P} = 0.5fF\) to find the new oscillation frequency of the RO.

**Solutions:** \(R_{ON,N}\) is the same as in 2b, \(R_{ON,P} = 10k\Omega\), \(C_{gate,N}\) is the same as in 2b, and \(C_{gate,P} = 0.5fF\).

The frequency will oscillate at \(f = \frac{1}{n(\tau_1 + \tau_2)}\) where \(\tau_1\) is the time delay at a PMOS node, \(\tau_2\) is the time delay at a NMOS node, and \(n\) is the number of nodes (inverters). The capacitance at the input of each node will be the same \((C_{gate,N} + C_{gate,P})\).

Thus, \(\tau_1 = 10k\Omega \times (0.5 + 0.5) fF \times \ln(2) = 6.93ps\); \(\tau_2 = 5k\Omega \times (0.5 + 0.5) fF \times \ln(2) = 3.47ps\), so \(f = \frac{1}{5(6.93ps+3.47ps)} = 19.2GHz\).

(b) Next, we’ll increase the size of the pMOS to match the nMOS drive strength. Using the same nMOS characteristics as Question 2, use \(R_{ON,P} = 5k\Omega\) and \(C_{gate,P} = 1fF\) to find the new oscillation frequency of the RO.

**Solutions:** \(R_{ON,N}\) is the same as in 2b, \(R_{ON,P} = 5k\Omega\), \(C_{gate,N}\) is the same as in 2b, and \(C_{gate,P} = 1fF\).

The frequency will oscillate at \(f = \frac{1}{n(\tau_1 + \tau_2)}\) where \(\tau_1\) is the time delay at a PMOS node, \(\tau_2\) is the time delay at a NMOS node, and \(n\) is the number of nodes (inverters). The capacitance at the input of each node will be the same \((C_{gate,N} + C_{gate,P})\).

Thus, \(\tau_1 = 5k\Omega \times (0.5 + 1) fF \times \ln(2) = 5.20ps\); \(\tau_2 = 5k\Omega \times (0.5 + 1) fF \times \ln(2) = 5.20ps\), so \(f = \frac{1}{5(5.20ps+5.20ps)} = 19.2GHz\).

(c) If we wanted to use the RO design from part (b) to generate a 1GHz clock, approximately how many inverter stages would be required?

**Solutions:** (c) Since 5 inverters produced a 19.2 GHz clock from part (b), in order to produce a 1 GHz clock, we would need about 5 * 19 inverters = 95 inverters.