This homework is due February 29, 2016, at Noon.

1. Homework process and study group

Who else did you work with on this homework? List names and student ID’s. (In case of hw party, you can also just describe the group.) How did you work on this homework?

2. Lecture Attendance

Did you attend live lecture this week? (the week you were working on this homework) What was your favorite part? Was anything unclear? Answer for each of the subparts below. If you only watched on YouTube, write that for partial credit.

(a) Monday lecture
(b) Wednesday lecture
(c) Friday lecture

3. Redo problem 3 on the midterm

(a)
(b)
(c)

4. Redo problem 4 on the midterm

(a)
(b)

5. Redo problem 5 on the midterm

6. Redo problem 6 on the midterm

7. Redo problem 7 on the midterm

(a)
(b)
(c)

8. Redo problem 8 on the midterm

9. Redo problem 9 on the midterm

(a)
10. Redo problem 10 on the midterm

(a) 
(b) 
(c) 
(d) 
(e) 

11. Redo problem 11 on the midterm

(a) 
(b) 
(c) 

12. Op-Amp Review and Prelab

In this review problem, you will apply the golden rules to derive something you need in lab.

Below is a picture of the equivalent model of an op-amp we are using for this question, where we are assuming $R_{in} \rightarrow \infty$ (open circuit) and $R_{out} \rightarrow 0$ (short circuit). Assume that no current flows into the "+" and "-" terminals of the op-amp, and $v_{out} = Av_{in} = A(V^+ - V^-)$. As in 16A, we assume $A \rightarrow \infty$ and so the golden rules apply when the op-amp is used in negative feedback.

Now let’s work on the circuit you will build in lab:
(a) Write down all the branch and node equations using the golden rules of Op-Amps.

(b) Notice that there exists a symmetry between the two op-amps at the first stage of this circuit. What are the directions of the currents going through the two $R_2$s? How do the currents of $R_2$s influence the current through $R_1$?

(c) What is the current through $R_1$?

(d) What are the output voltages of the two op-amps at the first stage?

(e) Compute the voltage at the + terminal of the second-stage op-amp.

(f) What is $V_{out}$?

(g) What is the voltage in the middle of the resistor $R_1$?

(h) Based on the above analysis, we could introduce a "fake ground" in the middle of the resistor $R_1$ and come up with the following circuit:

Now, each of the first two op-amps is being used in a form that resembles building blocks that you have seen before. What are the gains of those blocks? What is $V_{out}/(V_p - V_n)$ for this revised circuit?

13. Transistors and Boolean Logic
A Boolean formula can be implemented in digital circuitry using nMOS and pMOS transistors. In circuits, the truth value 1 (true) is represented by a high voltage, called POWER ($V_{DD}$). The truth value 0 (false) is represented by a low voltage, called GROUND (GND). In this problem, we will only use the truth values in order to simplify notations. That is, if you see $A = 1$ for a point $A$, then it means the voltage of $A$ is equal to $V_{DD}$. Similarly, if $A = 0$, then the voltage of $A$ is equal to GND.

An inverter can be implemented with 1 nMOS and 1 pMOS, as shown in the figure below. When the input $A$ is 0, then the nMOS is OFF and the pMOS is ON. Thus, the output $Y$ is pulled up to 1 because it is connected to $V_{DD}$. Conversely, when $A$ is 1, then the nMOS is ON and the pMOS is OFF, and $Y$ is pulled down to 0. Therefore, the circuit implements the Boolean formula, $Y = \overline{A}$.

In general, a Boolean-formula circuit has an nMOS pull-down network to connect the output to 0 (GND) and a pMOS pull-up network to connect the output to 1 ($V_{DD}$). The pull-up and pull-down networks in the inverter example each consist of a single transistor.

In this problem, we will ask you to design pull-up networks when pull-down networks are given.

(a) The pull-down network of the Boolean formula (a 2-input NAND gate), $Y = \overline{(A \land B)}$, is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.

(b) The pull-down network of the Boolean formula (a 2-input NOR gate), $Y = \overline{(A \lor B)}$, is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.
(c) The pull-down network of the Boolean formula, \( Y = \neg((A \land B) \lor C) \), is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.

(d) The pull-down network of the Boolean formula, \( Y = \neg((A \lor B) \land C) \), is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.
(e) You have designed four pull-up networks. What can you conclude about the rules for designing pull-up networks when pull-down networks are given?

14. Your Own Problem

Write your own problem related to this week’s material and solve it. You may still work in groups to brainstorm problems, but each student must submit a unique problem. What is the problem? How to formulate it? How to solve it? What is the solution?

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