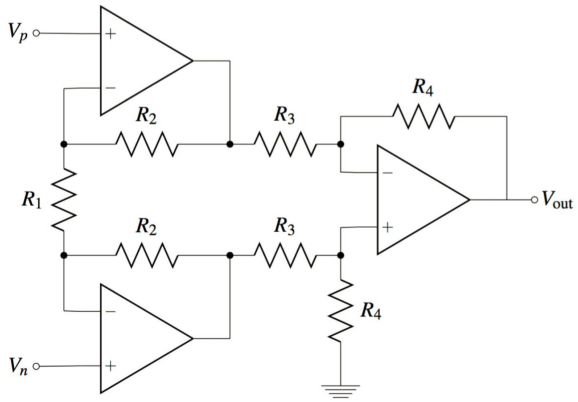
EECS 16B Designing Information Devices and Systems II
Spring 2017 Murat Arcak and Michel Maharbiz

Homework 0

This homework is due January 25, 2017, at 17:00.

1. Op-amp review

Let us look at the circuit below:



(a) Write down all the branch and node equations using the golden rules of Op-Amps.

(b) Notice that there exists a symmetry between the two op-amps at the first stage of this circuit. What are the directions of the currents going through the two R_2s? How do the currents of R_2s influence the current through R_1?

(c) What is the current through R_1?

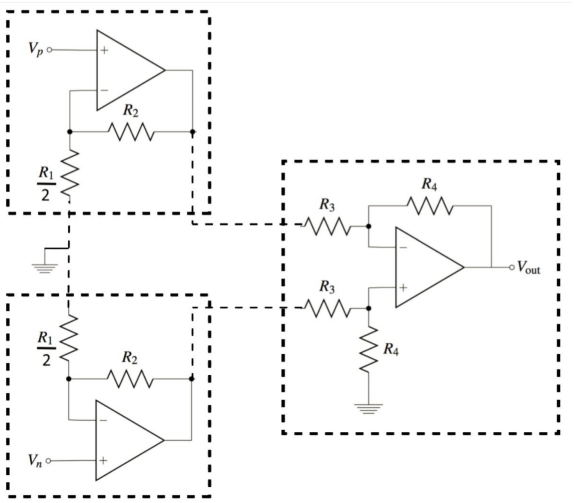
(d) What are the output voltages of the two op-amps at the first stage?

(e) Compute the voltage at the + terminal of the second-stage op-amp.

(f) What is V_{out}?

(g) If we broke R_1 into two series resistors, each with a value of $\frac{R_1}{2}$ What is the voltage at the node in between each of these resistors?

(h) Based on the above analysis, we could introduce a "fake ground" in the middle of the resistor R_1 and come up with the following circuit:



Now, each of the first two op-amps is being used in a form that resembles building blocks that you have seen before. What are the gains of those blocks?

What is $V_{out}/(V_p - V_n)$ for this revised circuit?

2. KVL

Now consider the circuit shown below:

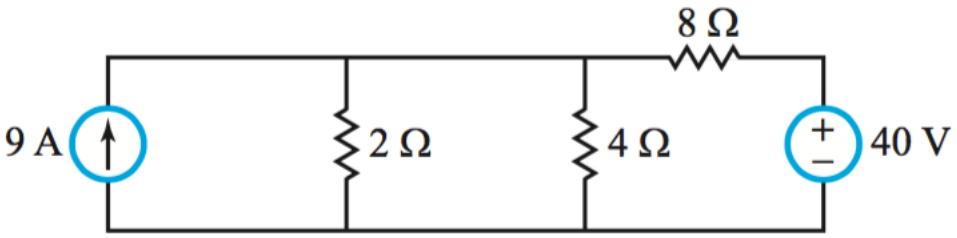


Figure 1: From Ulaby, Maharbiz, Furse. *Circuits*. Third Edition.

Determine the amount of power supplied by the voltage source.

3. KCL

Now consider the circuit shown below:

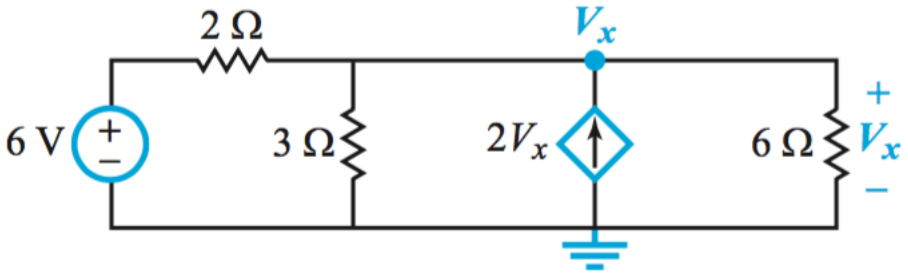


Figure 2: From Ulaby, Maharbiz, Furse. *Circuits*. Third Edition

Determine the voltage V_x.

4. Circuits and gaussian elimination

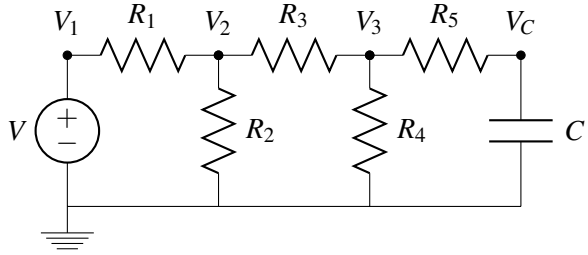


Figure 3: Example Circuit

(a) Find a system of linear equations that could be solved to find the node voltages.

(b) Given that the component values are $R_1 = 500\Omega$, $R_2 = 3000\Omega$, $R_3 = 1000\Omega$, $R_4 = 2000\Omega$, and $R_5 = 4000\Omega$, solve the circuit equations using Gaussian elimination.

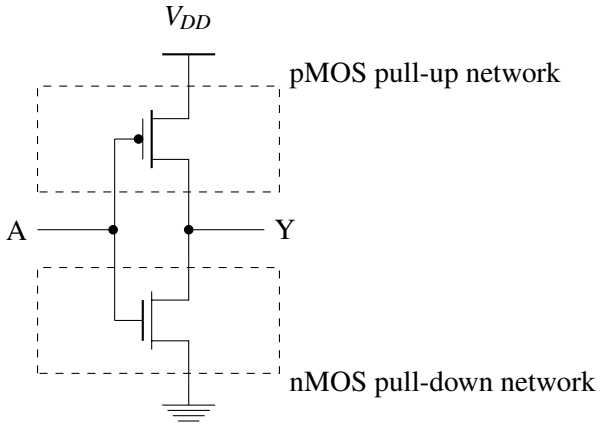
(c) What's the voltage V_C across the capacitor?

(d) How would you check your work? Do so.

5. Transistors and boolean logic

A Boolean formula can be implemented in digital circuitry using nMOS and pMOS transistors. In circuits, the truth value 1 (*true*) is represented by a high voltage, called POWER (V_{DD}). The truth value 0 (*false*) is represented by a low voltage, called GROUND (GND). In this problem, we will only use the truth values in order to simplify notations. That is, if you see $A = 1$ for a point A, then it means the voltage of A is equal to V_{DD}. Similarly, if $A = 0$, then the voltage of A is equal to GND.

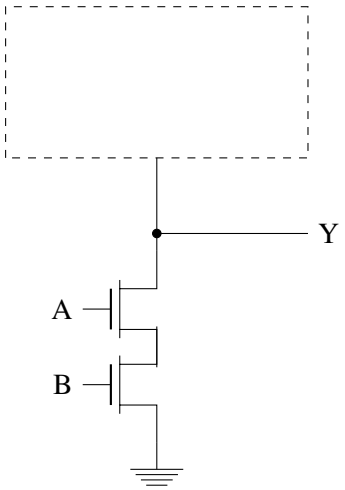
An inverter can be implemented with 1 nMOS and 1 pMOS, as shown in the figure below. When the input A is 0, then the nMOS is OFF and the pMOS is ON. Thus, the output Y is pulled up to 1 because it is connected to V_{DD}. Conversely, when A is 1, then the nMOS is ON and the pMOS is OFF, and Y is pulled down to 0. Therefore, the circuit implements the Boolean formula, $Y = \neg A$.



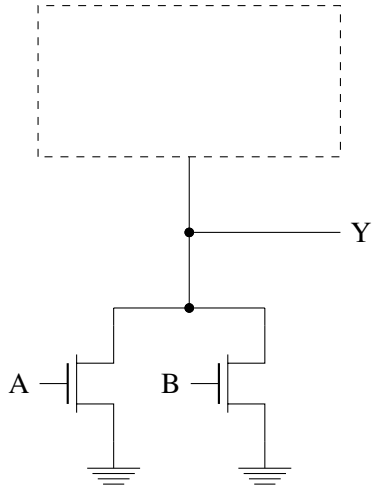
In general, a Boolean-formula circuit has an nMOS *pull-down network* to connect the output to 0 (GND) and a pMOS *pull-up network* to connect the output to 1 (V_{DD}). The pull-up and pull-down networks in the inverter example each consist of a single transistor.

In this problem, we will ask you to design pull-up networks when pull-down networks are given.

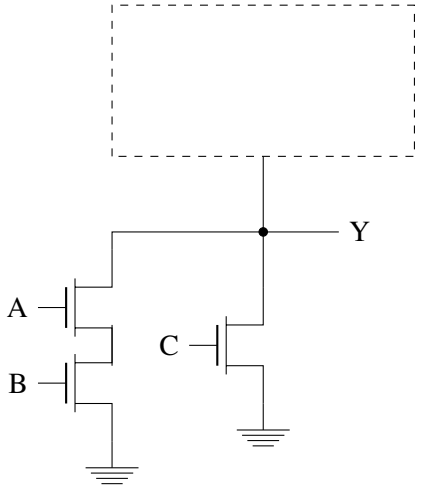
(a) The pull-down network of the Boolean formula (a 2-input NAND gate), $Y = \neg(A \wedge B)$, is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.



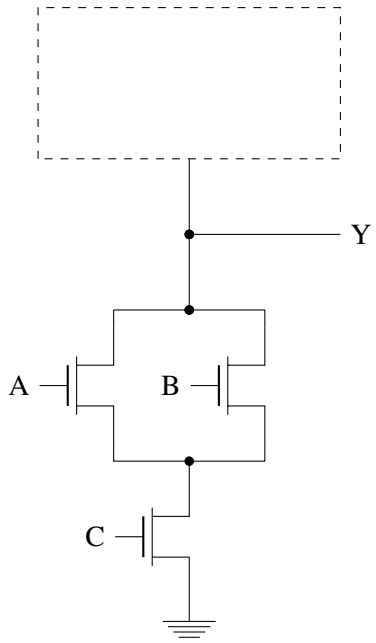
(b) The pull-down network of the Boolean formula (a 2-input NOR gate), $Y = \neg(A \vee B)$, is given below. Design the pull-up network (the dashed box) with 2 pMOS transistors.



(c) The pull-down network of the Boolean formula, $Y = \neg\big((A \wedge B) \vee C\big)$, is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.



(d) The pull-down network of the Boolean formula, $Y = \neg\big((A \vee B) \wedge C\big)$, is given below. Design the pull-up network (the dashed box) with 3 pMOS transistors.



(e) You have designed four pull-up networks. What can you conclude about the rules for designing pull-up networks when pull-down networks are given?

Contributors:

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