16B 19SP WOA

Next 9 lectures

- What limits speed & power of computers (μP)
- 1st order ordinary diff. eqn.
- time response, transient
- switching power in transistor circuits

Bohr → transistors

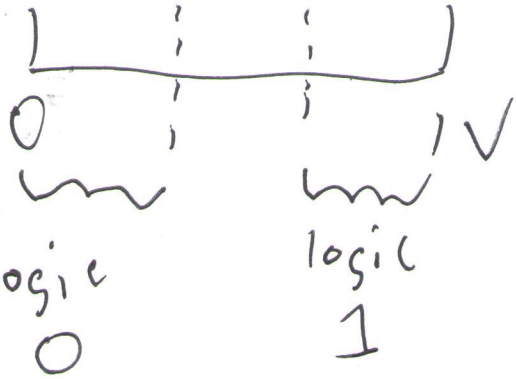
frequency response, Bode plots, applications

state space representation of O.D.E.

Digital Circuits

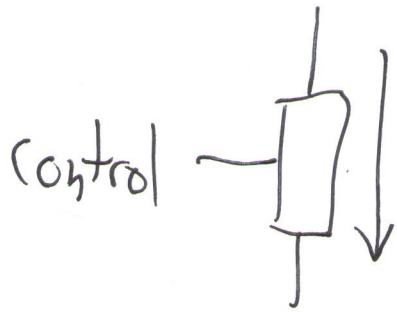
discrete/quantized interpretation of continuous signals

Ex:

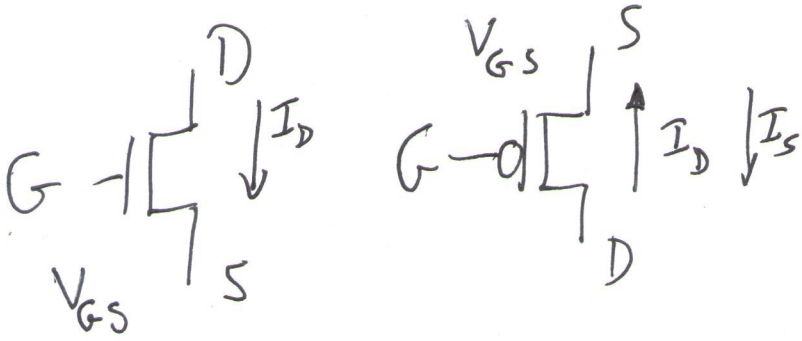


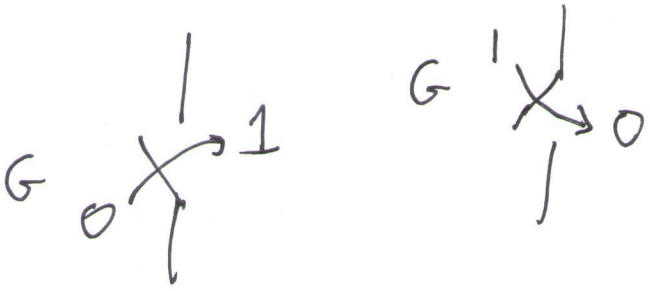
today CMOS - Complementary Metal Oxide Semi

NMOS PMOS



Gate controls current from source to drain





logic gate: inverter

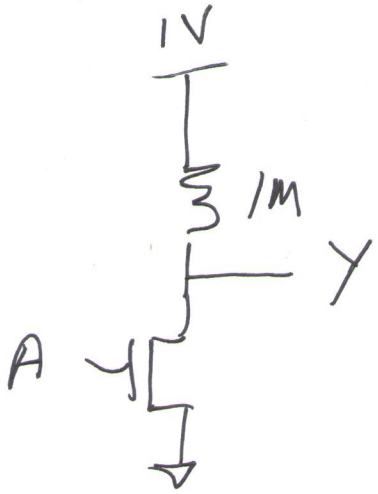
$Y = \text{not } A$

$= \overline{A}$

truth table

A	Y
0	1
1	0

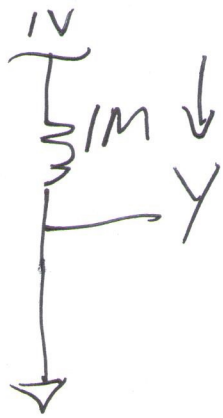
implementation



A = 0

Y = 1

A = 1



Y = 0

$I = \frac{V}{R} = \frac{1V - 0V}{10^6 \Omega} = \frac{1V}{10^6 \Omega}$

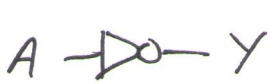
$= 1 \mu A$

$P = \frac{V^2}{R} = I^2 R = IV$

$= 1 \mu W$ when $Y = 0$

10^9 gates

$(10^9 \text{ gates})(10^{-6} \frac{W}{\text{gate}}) =$ hair dryer

simplest logic gate: inverter 

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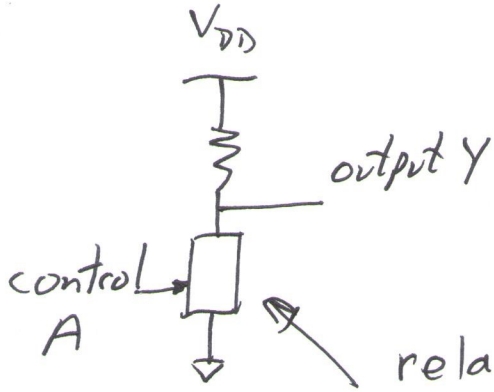
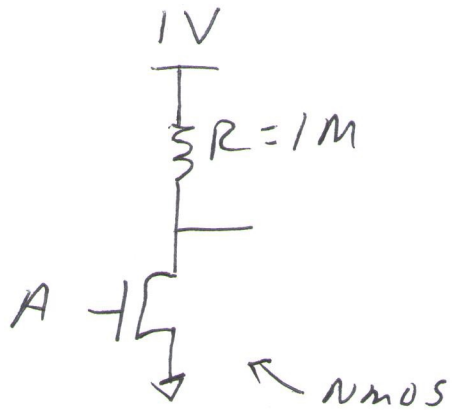
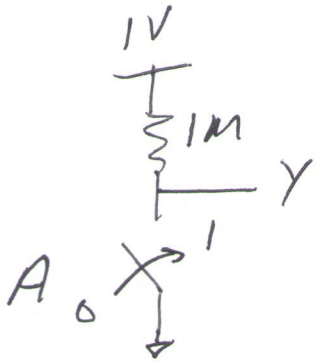
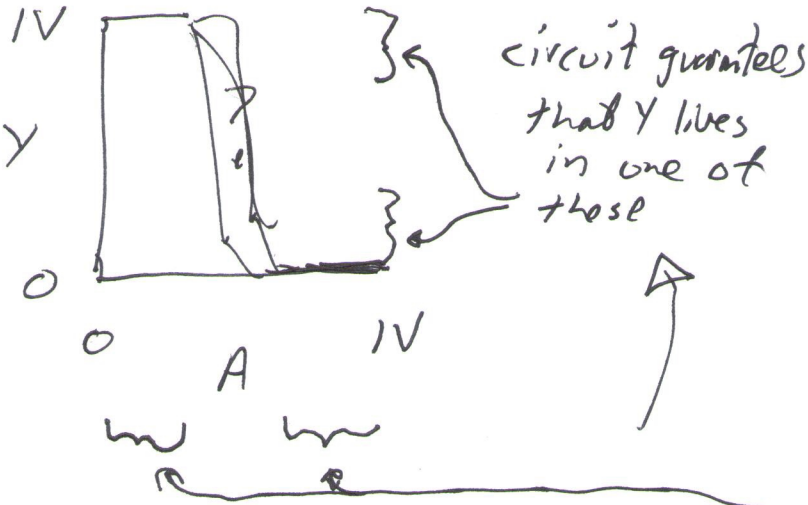
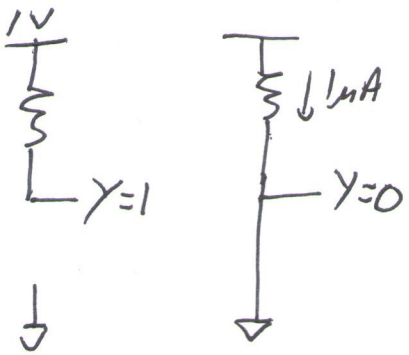








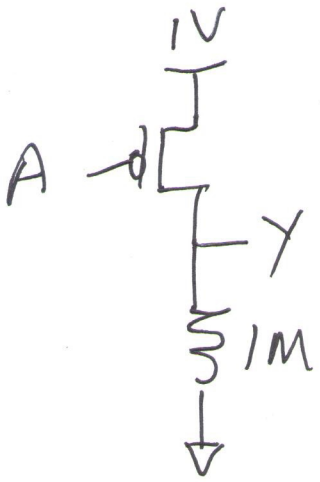
A = 0 A = 1



As long as A lives in one of these

noise immunity

PMOS inverter



A=0

Y = 1

I = 1μA

P = 1μW

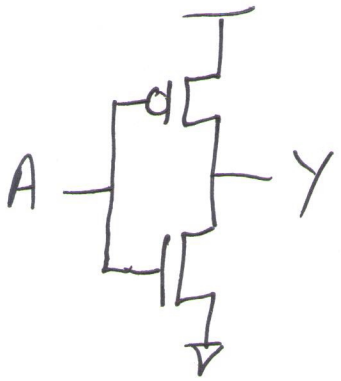
A=1

Y=0

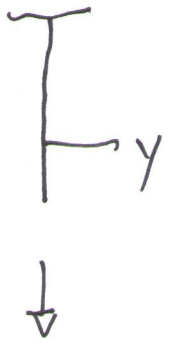
I=0

P=0

A → Y



A=0



Y=1

I=0

P=0

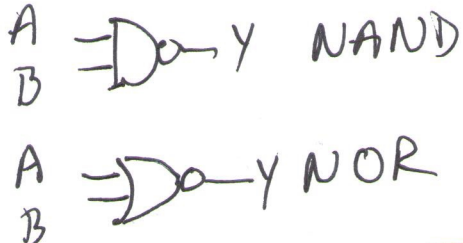
A=1

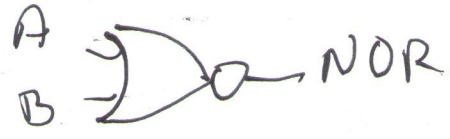
Y=0

I=0

P=0

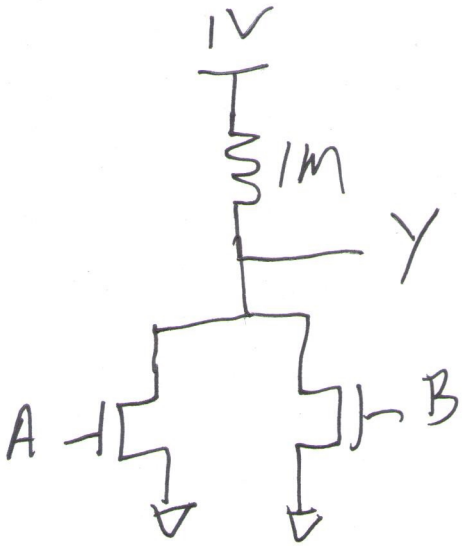
fancier gates

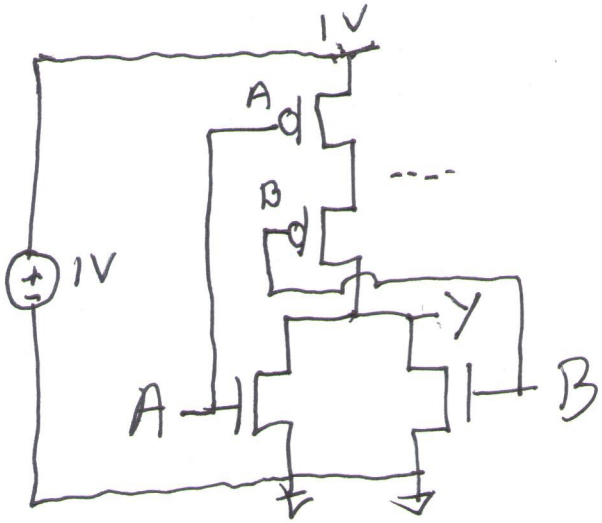


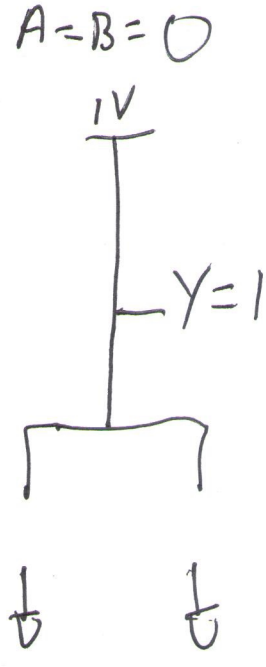


A	B	A+B	$\overline{A+B}$ = Y	
0	0	0	1	
0	1	1	0	at least 1 PMOS "open"
1	0	1	0	
1	1	1	0	

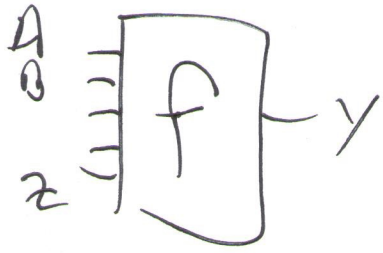
NMOS "ON"

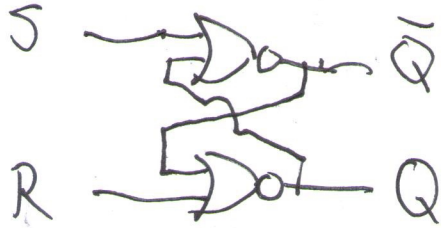






universal - make any digital function





SR latch

stores 1 bit

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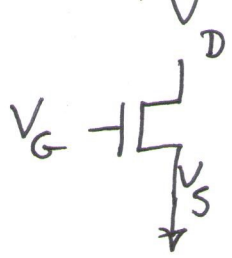
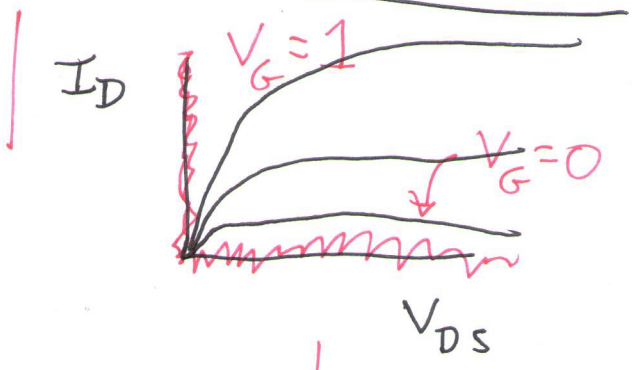
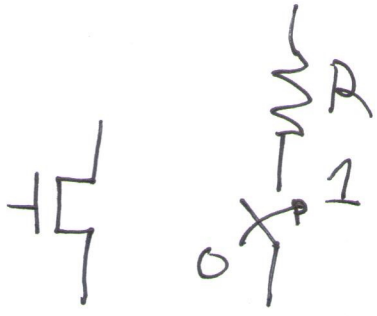
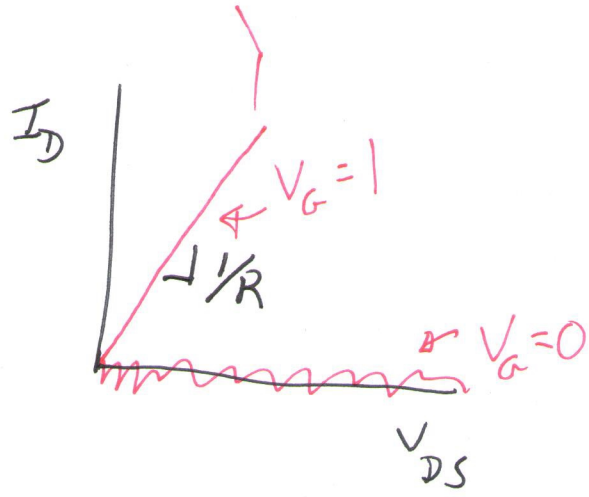
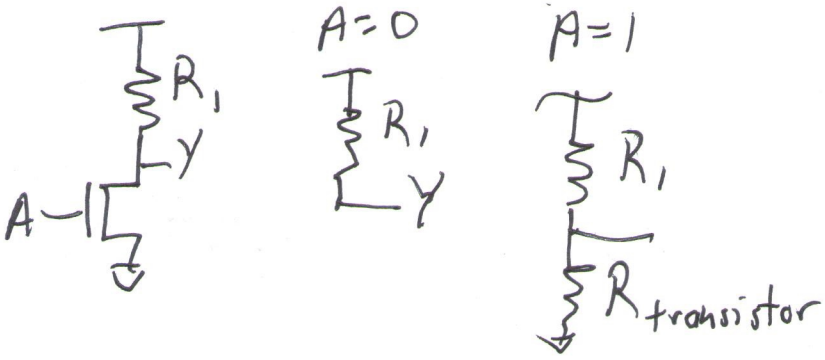
transistor = switch

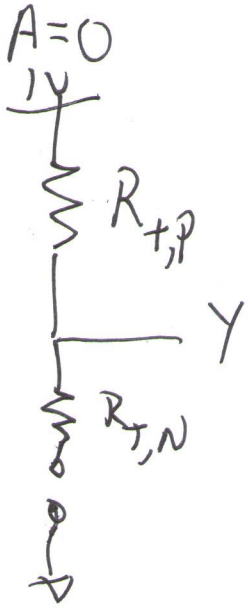




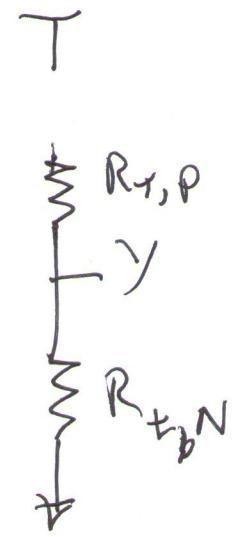




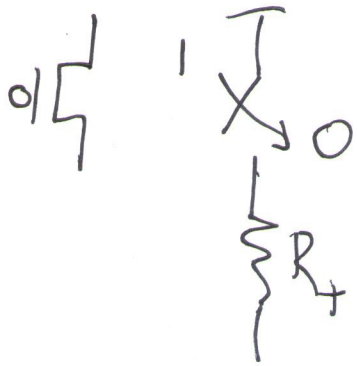




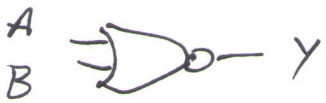
Y=1



Y=0



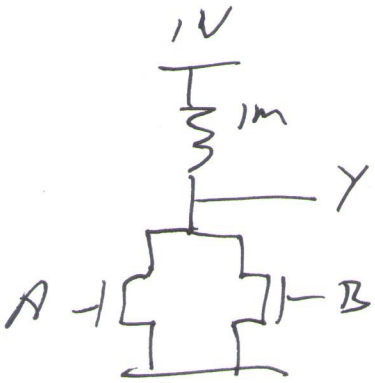
fancier gates



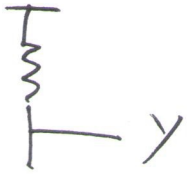
NOR gate

$Y = \overline{A+B}$

A	B	A+B	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

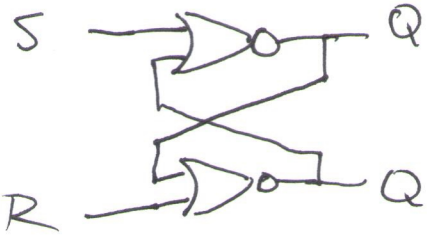


A = B = 0



A = 1 or B = 1
or both

NOR is a universal gate: any binary function can be implemented w/ 2-input NORs



CS61C

latch stores 1 bit