Next 9 lectures

- What limits speed & power of computers (CPU)
- 1st order ordinary diff. eqn.
- Time response, transient
- Switching power in transistor circuits

Bohr → transistors

- Frequency response, Bode plots, applications
- State space representation of ODE

Digital circuits

- Discrete/quantized interpretation of continuous signals

Ex: 0 | 1
     0 | 1
     Logic | Logic
     0 | 1
today CMOS - Complementary Metal Oxide Semi-

NMOS  PMOS

Gate controls current from source to drain

\[ G \to \frac{1}{G} \downarrow I_D \quad \frac{V_{GS}}{V_S} \quad \frac{V_{GS}}{S} \quad \frac{I_D}{I_S} \]

\[ G \to 1 \quad G \to 0 \]
logic gate: inverter

truth table

<table>
<thead>
<tr>
<th>A</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
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<td>0</td>
</tr>
</tbody>
</table>

A $\rightarrow$ Y  \hspace{1cm} Y = \text{not} \ A  \hspace{1cm} \bar{A}

implementation

$V$

$\frac{1}{3} \hspace{1cm} Y$

$A$

Y

A = 0  \hspace{1cm} A = 1

$\frac{1}{10^6} \hspace{1cm} Y$

$\frac{1}{10^6} \hspace{1cm} Y$

$Y = 1$  \hspace{1cm} Y = 0

$I = \frac{V}{R} = \frac{1V - 0V}{10^6 \Omega} = \frac{1V}{10^6 \Omega}$

$= 1 \mu A$

$P = \frac{V^2}{R} = I^2 R = IV$

$= 1 \mu W \text{ when } Y = 0$

$10^9 \text{ gates}$

$(10^9 \text{ gates}) (10^{-6} \text{ W}) = \text{hair dryer}$
simplest logic gate: inverter \( A \rightarrow \overline{A} \)

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\( Y = \text{not} \ A = \overline{A} \)

implementation

[Diagram of relay and transistor implementation]

\( V_{DD} \)

output

control

relay tube transistor (micro relay!)

[Diagram of circuit operation]

\( V = 5 \text{V} \), \( R = 1 \text{M} \)

A \rightarrow

\( Y = 3 \)

As long as \( A \) lives in one of these noise immunity
PMOS inverter

\[ A = 0 \quad A = 1 \quad A \rightarrow \overline{Y} \]

\[ Y = 1 \quad Y = 0 \]

\[ I = \mu A \quad I = 0 \]

\[ P = \mu W \quad P = 0 \]
A = 0

$T \quad T$

Y

Y = 1

I = 0

P = 0

A = 1

$T \quad T$

Y

Y = 0

I = 0

P = 0
fancier gates

\[ \begin{align*}
A & = \overline{D} \cdot Y \quad \text{NAND} \\
B & = \overline{D} \cdot Y \quad \text{NOR} \\
A & = \overline{D} \cdot Y \quad \text{NOR} \\
B & \\
\end{align*} \]

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>A + B</th>
<th>\overline{A + B} = Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
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<td>1</td>
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\[
\text{NMOS } \{00, 01\} \quad \text{at least 1 PMOS } \text{"open"}
\]

\[
A = B = 0
\]

\[
A = B = 0
\]

\[
Y = 0
\]

\[
Y = 1
\]
universal - make any digital function

\[ f(y) \]

SR latch
stores 1 bit

transistor = switch

\[ V_{DS} \]

\[ V_G = \frac{1}{R} \]

\[ A = 0 \]
\[ A = 1 \]
A = 0
\[ \frac{1}{Y} \]
\[ R_{T1P} \]
\[ R_{T1N} \]
\[ \rho \]
\[ Y = 1 \]

A = 1
\[ \frac{1}{Y} \]
\[ R_{T1P} \]
\[ \rho \]
\[ R_{T2N} \]
\[ Y = 0 \]
fancier gates

\[
\begin{align*}
A & \quad B \quad \Downarrow \quad Y \\
1 & \quad 1 \quad \text{m} \\
A & \quad \bar{A} \quad \bar{B} \\
A = B = 0 & \quad A = 1 \quad \text{or} \quad B = 1 \\
& \quad \text{or both}
\end{align*}
\]

NOR gate

\[
y = \overline{A + B}
\]

\[
\begin{array}{ccc|c|c}
A & B & A + B & \overline{A + B} \\
0 & 0 & 0 & 1 \\
0 & 1 & 1 & 0 \\
1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 \\
\end{array}
\]

NOR is a universal gate: any binary function can be implemented with 2-input NORs.

CS61C latch stores 1 bit.