

# EECS192 Lecture 1

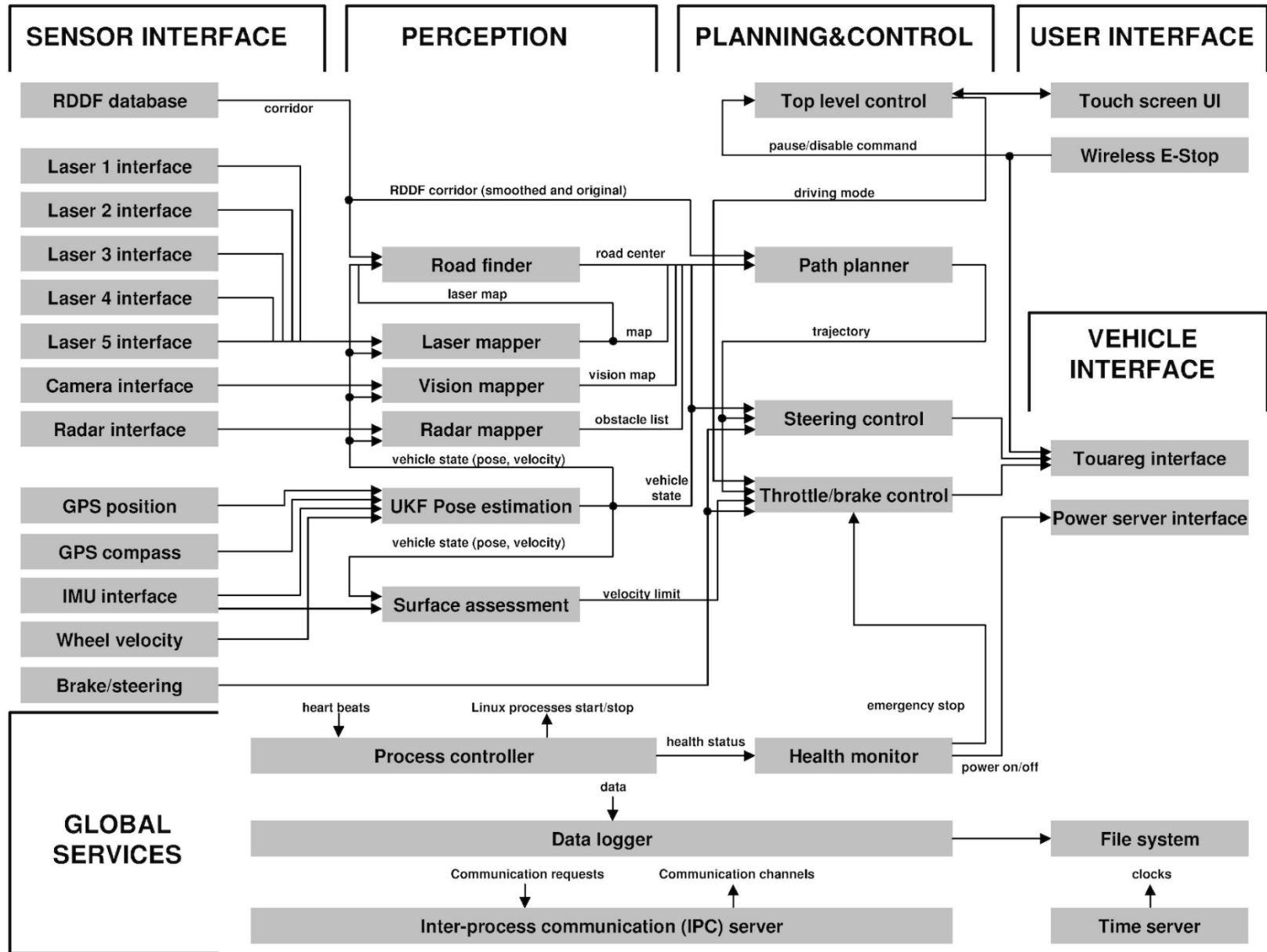
## Jan. 20, 2016

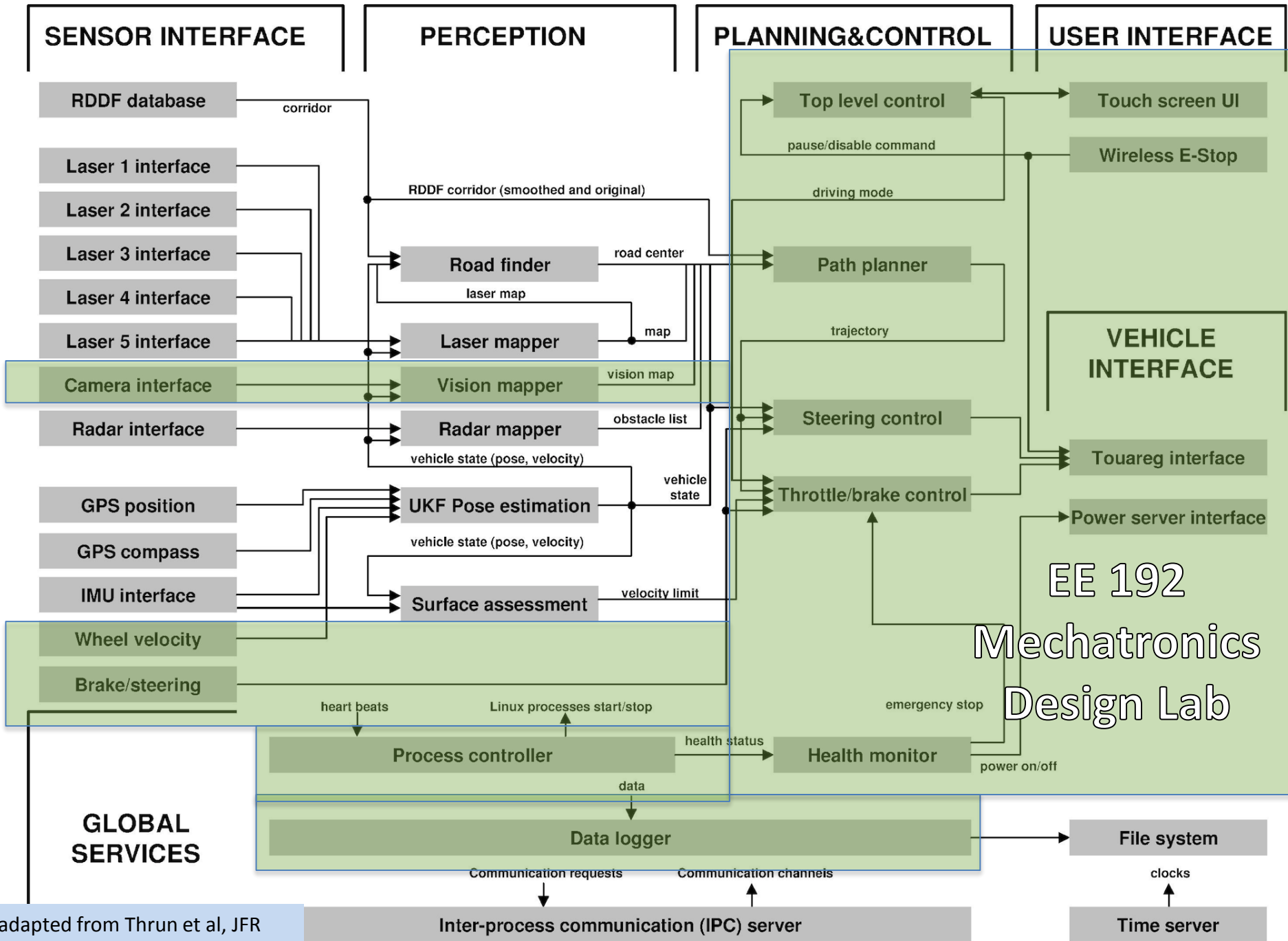
- Project Description
- Autonomous system example
- Course Organization
- ARM Cortex M0 overview

# Hardware

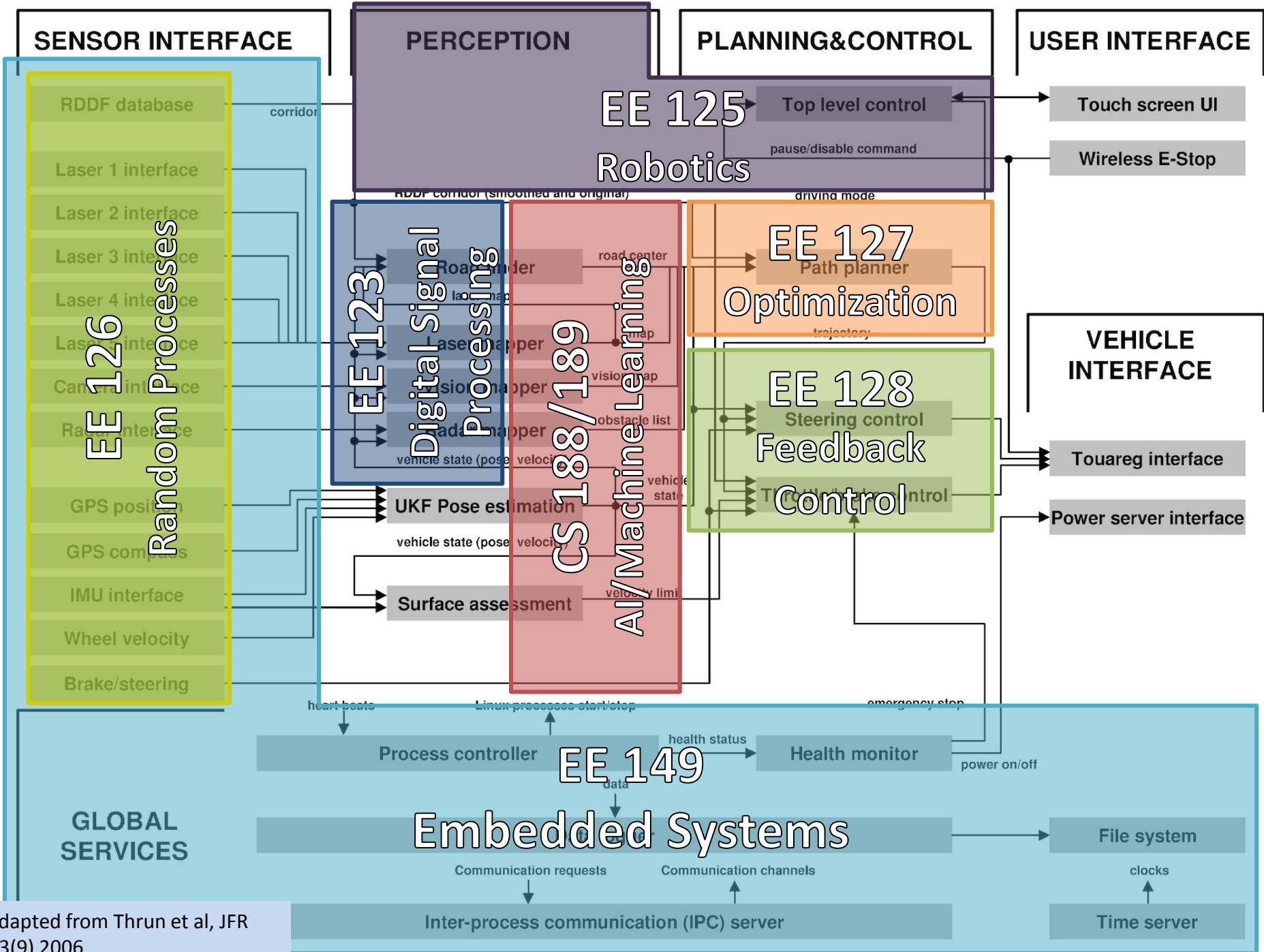


# Thrun et al Stanley 2005





adapted from Thrun et al, JFR 23(9) 2006



**SENSOR INTERFACE**

**PERCEPTION**

**PLANNING & CONTROL**

**USER INTERFACE**

- EE 126**  
Random Processes
- RDDF database
  - Laser 1 interface
  - Laser 2 interface
  - Laser 3 interface
  - Laser 4 interface
  - Laser 5 interface
  - Camera interface
  - Radar interface
  - GPS position
  - GPS compass
  - IMU interface
  - Wheel velocity
  - Brake/steering

**EE 123**  
Digital Signal Processing

**CS 188/189**  
AI/Machine Learning

**EE 127**  
Optimization  
Path planner

**EE 128**  
Feedback Control  
Steering control  
Throttle control

**EE 125**  
Robotics  
Top level control  
pause/disable command

- Touch screen UI
- Wireless E-Stop

**VEHICLE INTERFACE**

- Touareg interface
- Power server interface

**GLOBAL SERVICES**

**EE 149**  
Embedded Systems

- Process controller
- Health monitor
- Inter-process communication (IPC) server
- File system
- Time server

adapted from Thrun et al, JFR 23(9) 2006

# ARM® Cortex™-M0+ Core

Debug interfaces

Interrupt controller

MTB

## System

Internal watchdog

DMA

BME

## Memories and Memory Interfaces

Program flash

RAM

## Clocks

Phase-locked loop

Frequency-locked loop

Low/high frequency oscillator

Internal reference clocks

128K Flash  
16K RAM  
32 bit ARM 7 core  
48 MHz  
A/D, D/A  
2x SPI  
Touch sense input  
Timers

## Security and Integrity

Internal watchdog

## Analog

16-bit ADC x1

Analog comparator x1

6-bit DAC

12-bit DAC

## Timers

Timers 1x6ch+2x2ch

Low power timer x1

Periodic interrupt timers

RTC

## Communication Interfaces

I<sup>2</sup>C x2

Low power UART x1

SPI x2

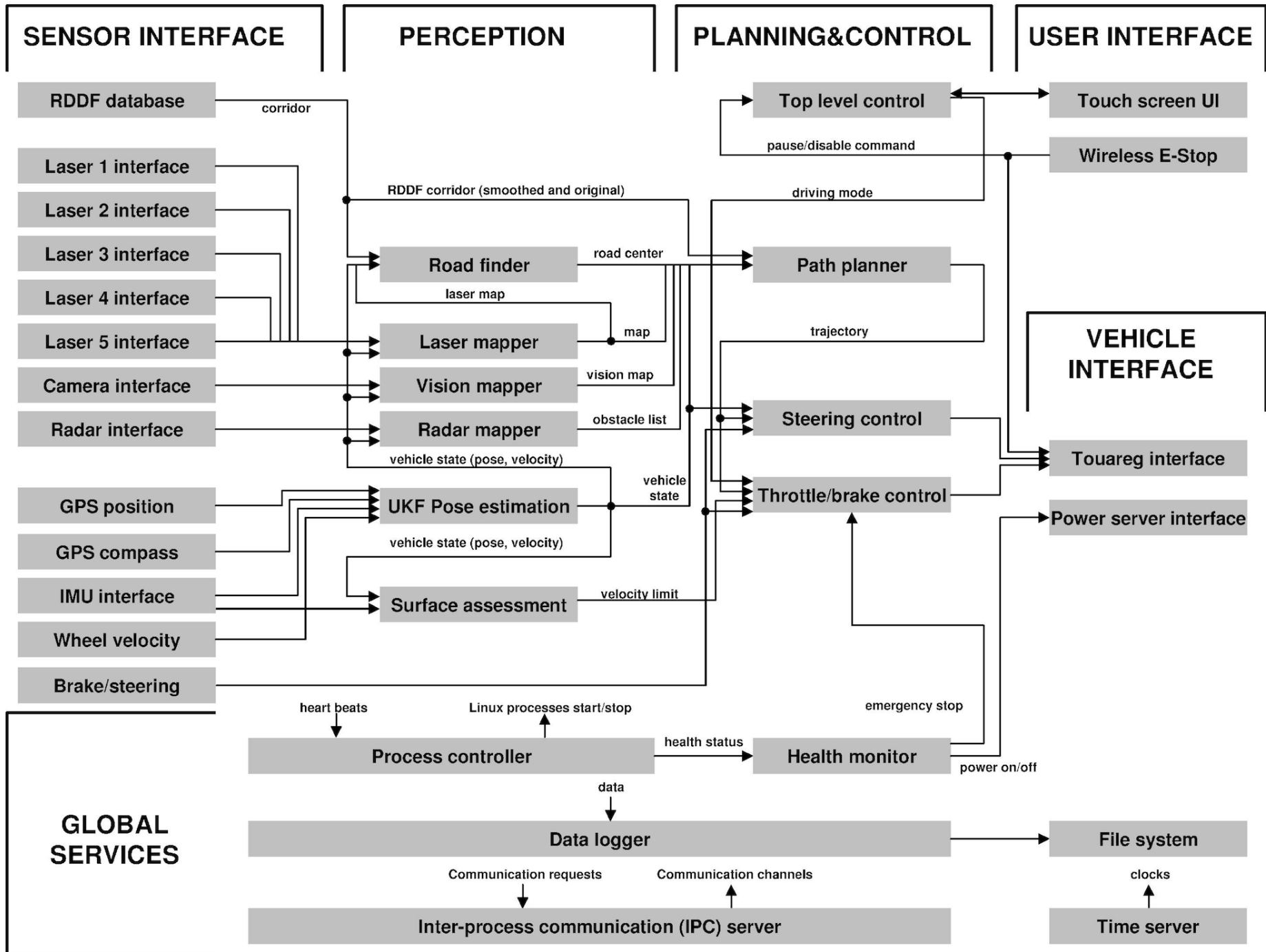
UART x2

USB LS/FS x1

## Human-Machine Interface (HMI)

GPIOs with interrupt

TSI



## Challenge: Embedded real-time programming

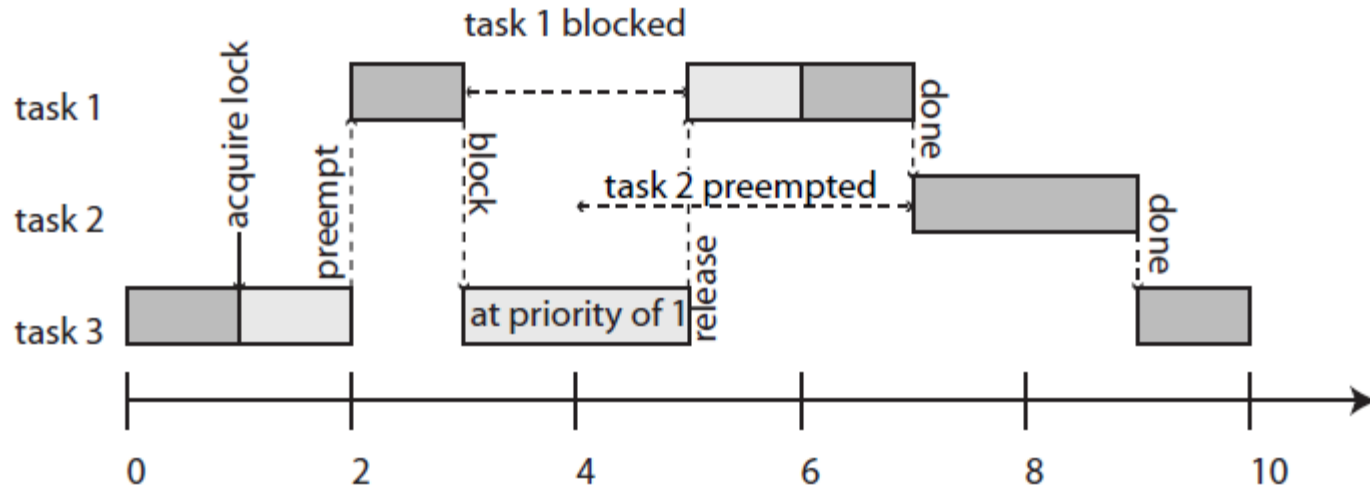
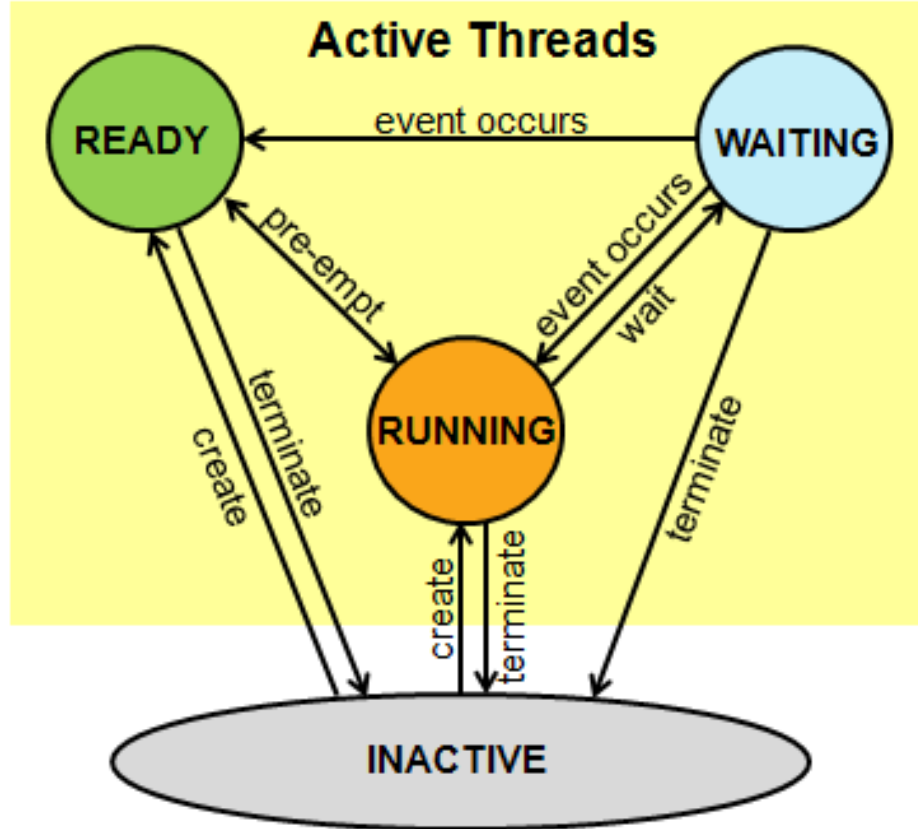


Figure 12.10: Illustration of the priority inheritance protocol. Task 1 has highest priority, task 3 lowest. Task 3 acquires a lock on a shared object, entering a critical section. It gets preempted by task 1, which then tries to acquire the lock and blocks. Task 3 inherits the priority of task 1, preventing preemption by task 2.

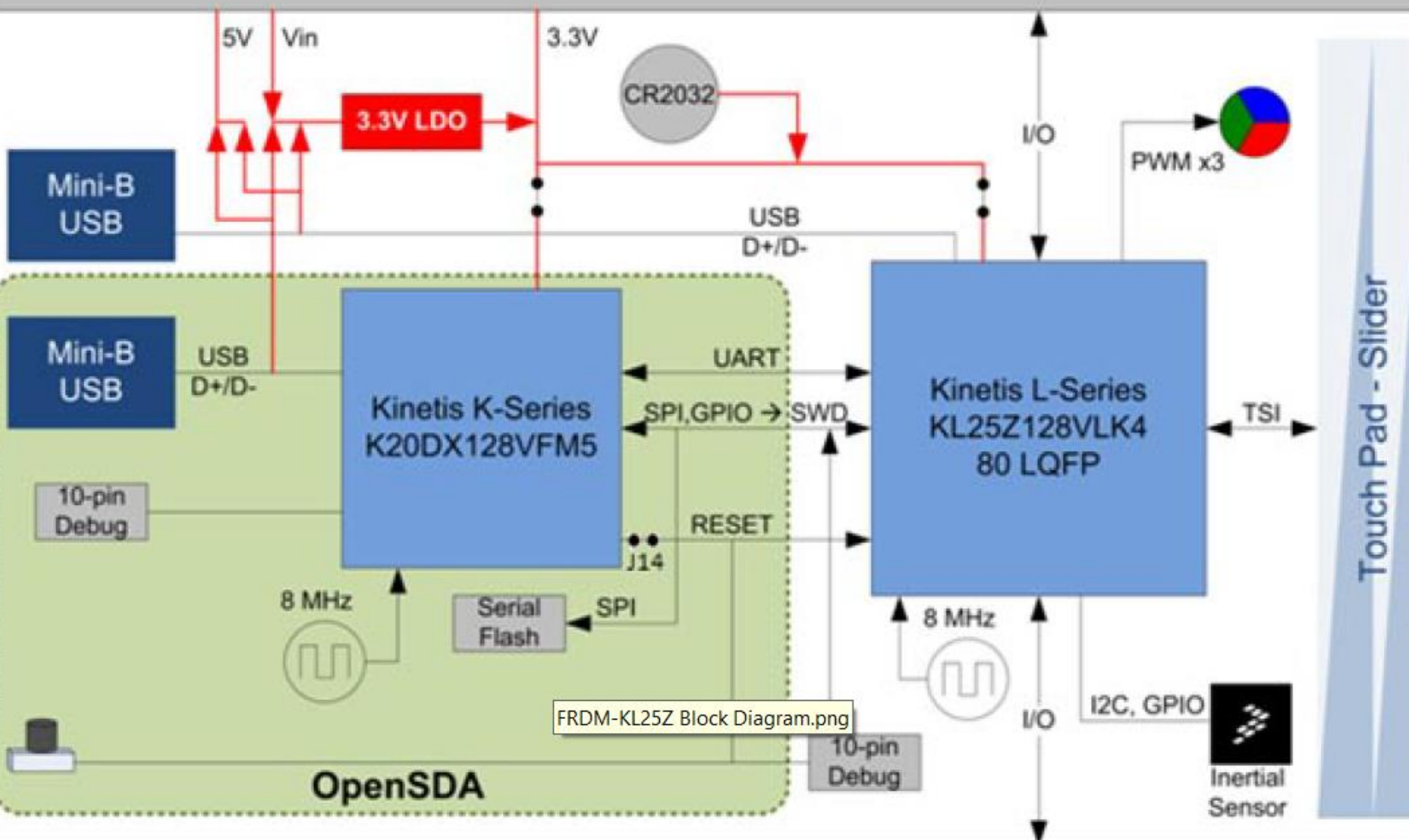




<https://developer.mbed.org/handbook/RTOS>



# I/O Header



FRDM-KL25Z Block Diagram.png

OpenSDA

# I/O Header