# FPA Printed Circuit Board Layout Guidelines

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## Introduction

Factorized Power with VI Chips enables system density to keep pace with technology by providing layout flexibility and high power density. More importantly, VI Chips allow a power conversion system to be "factorized" or separated into its constituent functions. A small, dense, and efficient VTM® Current Mulitplier is deployed at the point-of-load, minimizing the high current within a board and performing the voltage transformation and isolation functions of a power system. The regulation function is performed by the PRM® Regulator which can be located away from the VTM in a less space-constrained area of the motherboard, or on another board altogether. Since there are many advantages to the layout flexibility afforded by Factorized Power and VI Chips, some basic guidelines should be utilized when designing a system with these power components.

## The Importance of Board Layout

Board layout is crucial to the success of any application, both from the perspective of the power supply and the actual load. A good layout optimizes the overall system performance. A poor layout may result in power supply instability, low efficiency, noise, or data corruption throughout the system. Improper design of high current connections may result in unexpected board heating resistive losses. It may also result in parasitic spikes which occur during transient loading.

Routing power control signals is frequently one of the most overlooked aspects of system design—much care is taken with respect to proper layout of sensitive digital and analog signals for most system components while the critical signals interfacing with the power system are typically routed based on convenience, not proper design guidelines. Finally, Electromagnetic Interference (EMI) can degrade the performance of an otherwise well designed system. While there is no proven methodology to eliminating EMI from a power system, there are several guidelines for reducing EMI which will be covered.

## Low DC Impedance Layout at the Point of Load

Ideal layout of copper planes at the point of load is dependent upon the type of loading being applied. There are essentially two types of high-current, low-voltage load configurations: a) single device high current load (Fig. 1) and b) multiple devices powered by a single low-voltage rail (Fig. 2).

*Figure 1*
*Single device high current load*

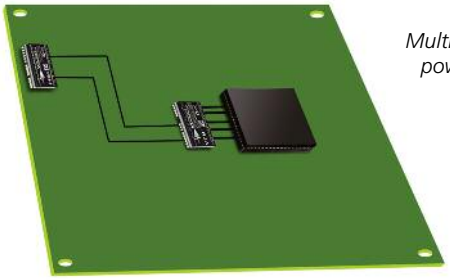
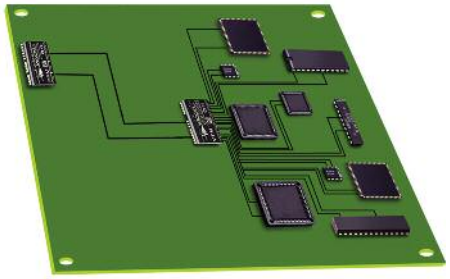


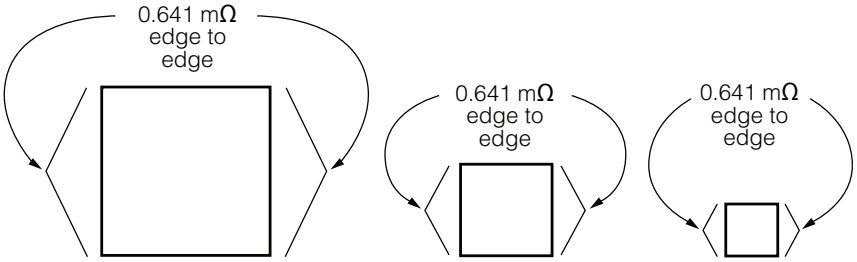
*Figure 2*
*Multiple devices powered from single low voltage rail*



For typical low-voltage, high-current applications DC impedance and AC impedance (inductance) must be minimized.

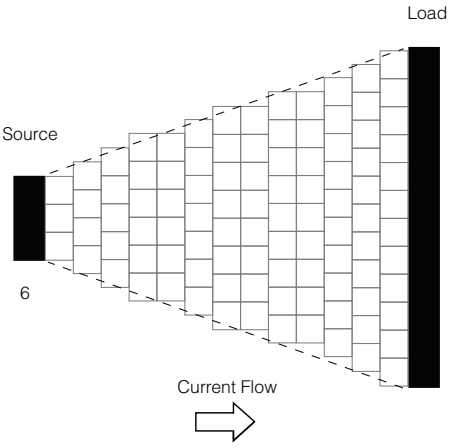
Minimizing DC impedance in a board layout requires an analysis using squares to determine the geometry and the impedance of the interconnect.

*Figure 3*
*A square will have the same edge to edge impedance regardless of size*




A square of 1 oz. copper will have a resistance of 0.641 mΩ between parallel edges, regardless of square dimension (Fig. 3). It is important to note that the current must originate and flow evenly from edge to edge of the square. If the geometry of the source or load is such that current would not flow evenly from edge to edge of the square, the square geometry must be reduced in size (Fig. 4).

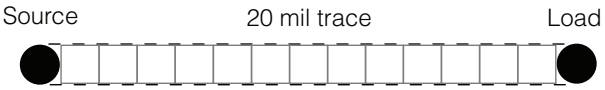
*Figure 4*
*Current flow through a plane broken into squares*



There are five steps to determining the DC board loss for a single high current microprocessor load:

**1)** *Determine the current path between source and load. If the source and load are connected by a trace, the current path is the trace path (Fig. 5).*

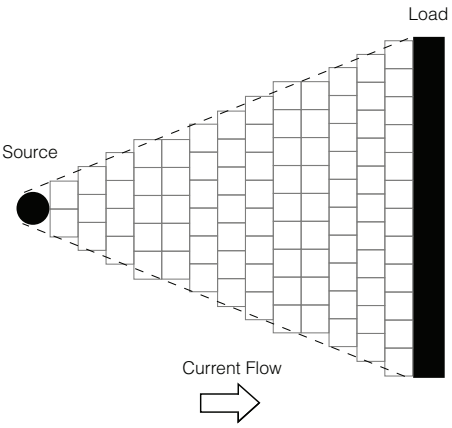
*Figure 5*
*A trace path is easily broken down into squares*




*If the source and load are connected by a plane, the current will take the shortest path (Fig. 6).*

*As illustrated in Fig. 6, the current path may end up with a fan-shaped characteristic if the source and sink geometries have different sizes. Also keep in mind that the positive and negative current paths may be routed differently.*

*Figure 6*
*Current flow through a plane*




**2)** *Break the current path up into a number of squares of integral size. As illustrated in Fig. 5, if the trace width is 20 mils, the current path can be broken up into a series of 20 mil squares for the length of the trace. If the current path is through a plane as shown in Fig. 6, the shape should be re-constituted using an array of squares that are small enough to reasonably represent its original shape.*

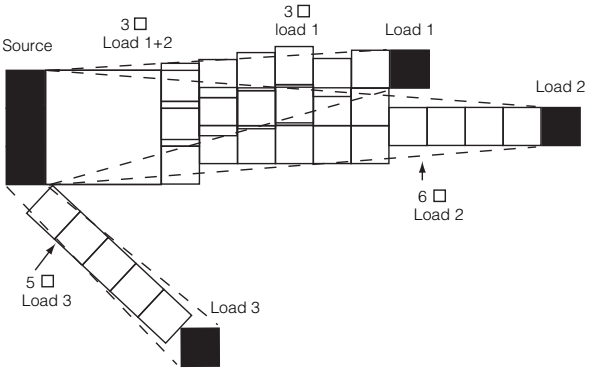
**3)** *Calculate the total number of squares. Per the connection shown in Fig. 5, this would be the sum of the squares in the current path. For Fig. 6, parallel squares would be summed as the reciprocal of the number of squares in parallel. For example, 2 squares in parallel would count as 1/2 a square, 4 squares in parallel would count as 1/4 a square, etc.*

**4)** *Calculate the resistance of the current path. Using the rule that a square of 1 oz. copper is 0.641 mΩ, multiply this by the calculated number of squares for the total resistance. If there is more than 1 oz. total copper, this number decreases proportionally. Likewise if there is less than 1 oz. total copper, this number should increase proportionally.*

5) *Multiply this number by the maximum current squared to calculate the distribution loss in watts for this current path.*

**Steps 1-5** should be repeated for each current carrying segment between source and load. If there are multiple points of load (for example one VI Chip® is powering 5 or 6 devices in different locations), steps 1-5 should be performed separately for common current paths (using total current) and unique current paths (using the current flowing to the particular device). This is illustrated in Fig.7.

*Figure 7*
*Current flow to multiple load points; 3 squares carrying current to Load 1 and 2, 3 additional squares carry current exclusively to Load 1, 6 additional squares carry current exclusively to Load 2, and 5 squares carry current to Load 3*




## Low AC Impedance Layout at the Point of Load

The AC impedance of the path from the output of the VTM® to the point of load is critical in applications where a good transient response is required. The leading edge of the transient response is determined by Equation 1.

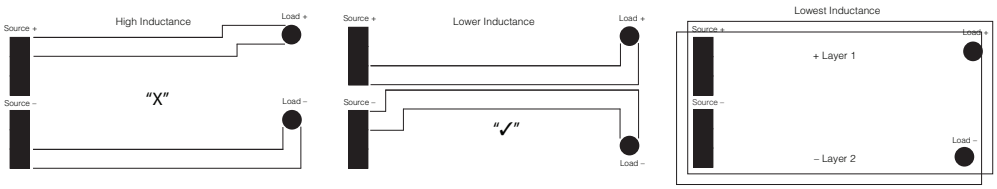
*Equation 1*

$$V_{TRANS} = L \bullet \frac{dIL}{dt}$$

In this equation IL represents the load current and L represents the inductance between the source and the load.

To limit this inductance, source and return currents should flow as close to each other as possible to maximize cancellation of the respective magnetic fields. Inductance is primarily a function of loop area – the greater the area between the source and return currents, the less cancellation of flux, and the greater the overall inductance (Fig. 8).

*Figure 8*
*Minimizing loop area lowers AC impedance*



The VTM® package design limits parasitic inductance (Fig. 9) by alternating pads of source (+Vout) and return (-Vout). However, even here there is imperfect cancellation of currents, resulting in a parasitic inductance term. This term can be minimized by terminating Vout+ and Vout- planes on the PCB as close as possible (Fig.10) and interleaving Vout+ and Vout- planes between the VTM and the load.

*Figure 9*
*VTM package*
*(bottom view)*

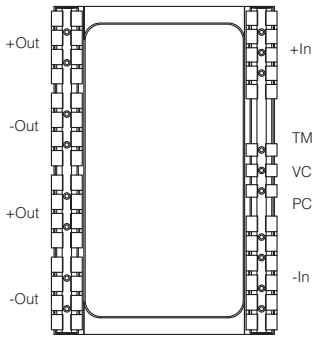
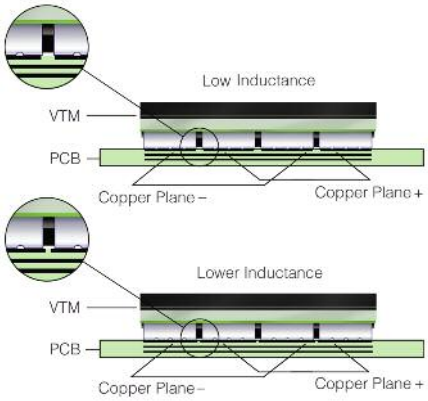



*Figure 10*
*Low induction*
*VTM interconnect*




With this type of layout, it is possible to achieve interconnect inductance as low as 400 pH for the VTM full size package.

Other recommendations for low AC impedance are:

1) Use vias between and behind J-leads to conduct current to the inner interleaved layers. Vias can also be placed in front of the J-leads to further decrease DC impedance but the pads should be tapered and as small as possible to limit AC impedance.

2) Interleave copper planes as much as possible. If it is not possible to dedicate planes to Vout+ and Vout-, the traces or sub-planes should be routed on top of each other as opposed to side by side.

3) Use high frequency bypass capacitors at the point of load to decouple the parasitic inductance from the load. These capacitors should be placed in line with the current flow, and should be of a low ESL / ESR type.

4) The VTM should be placed as close to the point of load as possible.

## PRM® – VTM® Layout

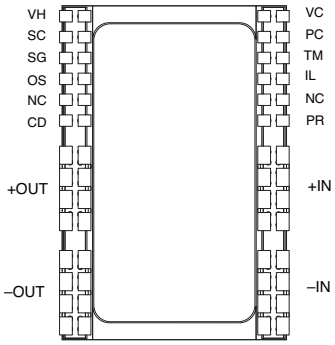
We now review the layout of signal and power interconnections for a PRM and VTM system.

## PRM Control Signals: OS, SC, CD

The PRM pins are shown in Fig. 11. It has a number of control pins, which control the output voltage set point and compensation as a function of load when used in the Adaptive Loop mode.

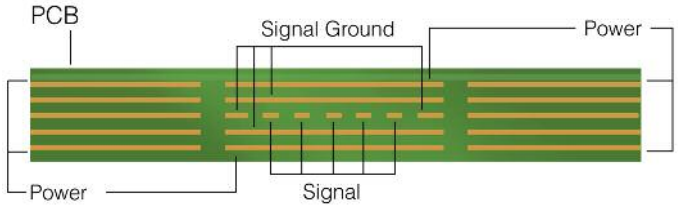
These control pins are high impedance and are susceptible to noise pick up. The primary pins of concern are: PR, OS, SC, CD, VC and to a lesser extent PC. All with the exception of PC have a direct connection to the regulation control loop.

*Figure 11*
*PRM package*
*(bottom view)*




Resistors used to set the device output (OS, CD) should be located as close to their respective PRM® ports as possible to minimize noise pick up. Increase noise immunity by shielding these signals from the power signals. This shield plane should be made part of the PCB as shown in Fig. 12. If these components cannot be placed adjacent to the PRM, a local bypass capacitor of ~200 pF should be used to attenuate any high frequency components. This device forms the regulation stage, so it is the most sensitive to layout issues when compared to the VTM®.

*Figure 12*
*Shielding signals from*
*power traces improves*
*noise immunity*




## PRM Control Signal: PR

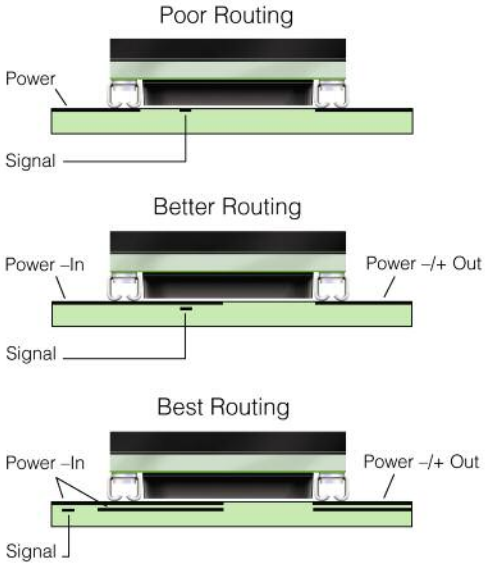
The PR signal is used to parallel multiple arrays of PRMs or PRM / VTM pairs. There are special considerations that need to be implemented in the layout of a VI Chip® array that are discussed at length in the Application Note "Paralleling PRMs and VTMs".

## PRM®, VTM®, and BCM® Control Signal: PC

PRMs, VTMs, and BCMs all have a PC (primary control) port which is used to enable and disable the device. This port is important in that it is designed to interface with external application specific devices (such as the load, or a microcontroller, or some other device which sequences power supplies). A typical application may route the PC signal a considerable distance across the printed circuit board, so care must be taken. The PC signal, especially compared with the control signals OS, CD, SC, and PR is quite noise immune. However, capacitive coupling from neighboring high voltage switching traces could result in noise on the PC pin.

This noise, if it is great enough could cause the device (PRM®, VTM®, or BCM®) to disable. To eliminate this, the PC pin should not be routed under or beside traces which have a high switching (dV/dt) signal on them. Keep in mind that other modular power devices may have high voltage switching inside (as an example, the PC trace should not be routed under the primary side of a high voltage BCM, as shown in Fig. 13). If routing near high switching traces or devices is absolutely necessary, Faraday shielding using the –IN return for the VTM and BCM, and the SG for the PRM should be employed, also shown in Fig. 13.

*Figure 13*
*Shielding PC from high voltage switching node*




## PRM / VTM Interconnect Signal: VC

The VTM has one control node, VC, which is used with the PRM to achieve voltage compensation as a function of load when the pair is used in the Adaptive Loop mode. This signal should be routed close to the PRM –OUT trace, which serves as the return for this signal. Shield the signal by routing it between two layers connected to SG. Ferrite beads (33 Ohm @ 100 MHz) can be installed in the VC line and -IN line to provide some very high frequency attenuation.

## PRM / VTM Power Interconnect

One of the major advantages of Factorized Power is the ability to locate the VTM at the point of load while at the same time minimizing the power interconnect from the PRM. This is accomplished by having the PRM provide a relatively high output voltage of ~48 Vdc to the VTM. In such a way, a 150 W / 100 A load can be supported by only providing ~3 A to the point of load VTM.

For loads using a VTM, the interconnect impedance between PRM-VTM seen at the point-of-load follows Equation 2.

*Equation 2*

$$Z_{LOAD} = Z_{PRM-VTM} \bullet K^2$$

Here K is the transformation ratio of the VTM® defined as the output voltage divided by the input voltage. Equation 2 is valid for impedance values from DC to ~1 MHz. Beyond this, the internal impedance of the VTM plays a role.

Equation 2 indicates a geometric relationship between K factor and reflected impedance. For a K = 1, the load impedance is equal to the interconnect impedance. For a K = 1/32, however, the load impedance is seen as 1/1000th of the interconnect impedance. Thus if a K = 1/32 VTM were used, 1 Ω of PRM®-VTM interconnect impedance would look like 1 mΩ of source impedance at the point of load.

Since the source impedance is reduced at the point of load by the VTM, the power interconnections between PRM and VTM can be made smaller (with higher impedance) with little effect on load characteristics. However, traces should always be sized to dissipate as little power as possible. Parasitic inductance should also be minimized where possible.

One final note concerns output and input ripple voltage. Since the PRM and VTM are both power conversion devices operating at a specific switching frequency, they both provide a characteristic ripple voltage on the input and output bus. Since PRM and VTM switch at similar but different frequencies, there is the possibility of low frequency "beats" to show up on the factorized bus. To attenuate beat frequencies and the potential of issues both in the control loop and application, it is recommended that a small amount of inductance be placed between the PRM and VTM. A 0.4 uH inductor placed in series with the + OUT of the PRM and the + IN of the VTM sufficiently attenuates high frequency currents in most applications.

## Layout for EMI Minimization

Here are some brief layout guidelines to minimize the effects of conducted and radiated noise. Actual filter and shield design is covered in a separate application note. Here the layout of components to minimize conducted and radiated EMI will be discussed.

Both PRM and VTM components are 1-2 MHz switching converters. Since Zero-Voltage-Switching (ZVS) and Zero-Current-Switching (ZCS) techniques are used, the level of conducted and radiated noise is significantly lower than conventional hard switching supplies.

Differential mode noise is AC voltage that appears between Vin+ and Vin- (or Vout+ and Vout-) of the converter. For the PRM and VTM both common and differential-mode noise has a strong component at 1-2 MHz and smaller high frequency components beyond 10 MHz. Typically downstream POL converters (such as niPOLs) will show with strong fundamentals between 100 and 500 kHz.

Common and differential-mode filtering components should be sized and located to attenuate the 1-2 MHz fundamental. Shunt and serial attenuation components (capacitors and inductors) should be located close to the VI Chip®.

Very important to controlling conducted noise is radiated noise. Radiated noise is AC voltages that are induced by Electromagnetic fields. Electromagnetic fields are generated by AC currents traveling through a conductor (such as a copper trace, plane, or wire). The ability of a conductor to radiate is based on its its length, the current which it is carrying, and the frequency of the AC current. Radiated noise is also caused by magnetic fields from transformer or inductor components coupling with a nearby conductor.

Radiated and conducted noise are linked since one may easily cause the other. Filtering components components should be placed close enough to the VI Chips such that they attenuate conducted noise, however not so close as to allow radiated noise to bypass or couple into them. Surrounding metal may act as a shield to protect noise sensitive components, but also as a conduit that would re-direct noise to another part of the circuit.

The following are some simple layout guidelines for reducing EMI effects.

1) *Limit high frequency differential current travel within the PCB. Filtering and high frequency bypass capacitors should be located as close to the module as possible. The 1-2 MHz ripple component should be well filtered, particularly if it is traveling more than 1-2 inches (i.e. the PRM® and VTM® are separated by more than 2 inches).*

2) *Common-mode bypass should be local to the VTM and should be bypassed to a grounded shield plane located directly under the VTM. This will return capacitively coupled common-mode switch currents local to the VTM and limit the extent to which they couple into other planes.*

3) *A combination of series and shunt attenuation practices should be used. Shunt attenuation should provide a low impedance return path for noise currents. Series attenuation should increase the impedance of the path from the module (noise source) back to the power source.*

4) *Noise sensitive components should not be located directly above the PRM or VTM. Both VI Chip® components have a closed magnetic field present directly above and below the package. 1-2 MHz noise may be coupled into components that intercept this field.*

5) *Self-resonance frequencies of bypass components should be well known. It is possible that a bypass capacitor may self-resonate at a frequency close to the switching frequency of the PRM or VTM. Generally ceramic or film capacitors have a very high Q. Series resistive damping may need to be considered in some applications.*

## Conclusion

Good layout practices are crucial for designing a small, dense system that performs optimally for a given application. However, with the deployment of power components among sensitive load components, care must be taken in designing a system, both to optimize the layout of the load components and the power system.

A few basic guidelines in laying out a PRM® and VTM® will provide the basis for a quiet, efficient, and dense system.

Vicor Applications Engineers are experts in applying VI Chip® components to a large range of applications. Vicor Applications Engineering is available as needed to conduct reviews of layouts using VI Chip components and provide recommendations and feedback at any stage in the design cycle.