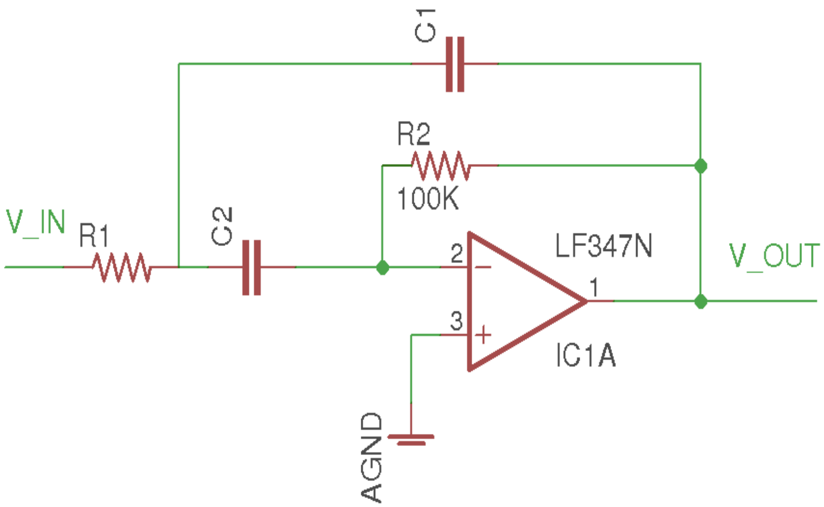
EECS192 Lecture 2
Jan. 24, 2017

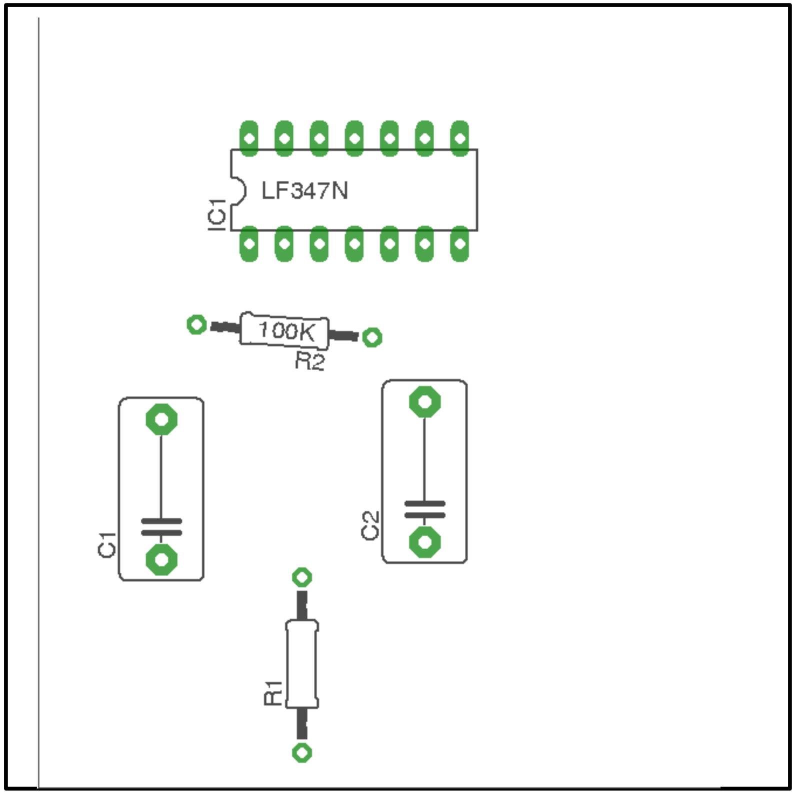
- Project proposal
- Documentation
- Block Diagram/Software Model
- LED/Port Information
- Motor Model

Notes:
Check off- Hello World+LED
``look don’t touch’’
Github repo

Documentation



Eagle parts layout- no copper



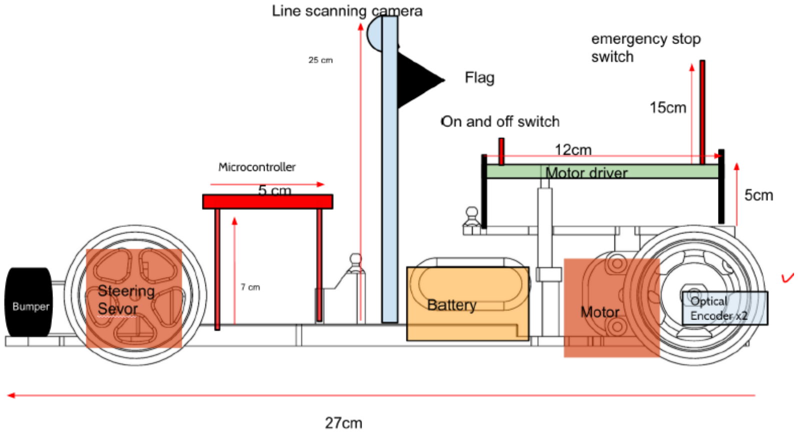
Black: tNames, tValues, tPlace
White or off: tOrigins, Unrouted

Eagle: File → export → image (300 dpi png)

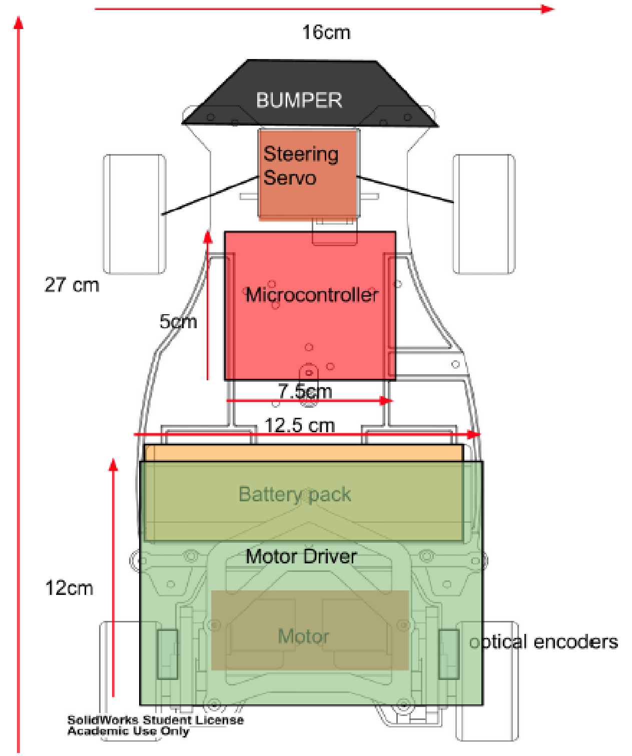
Documentation

2. Detailed Mechanical Drawing of Vehicle

a. Side view of vehicle

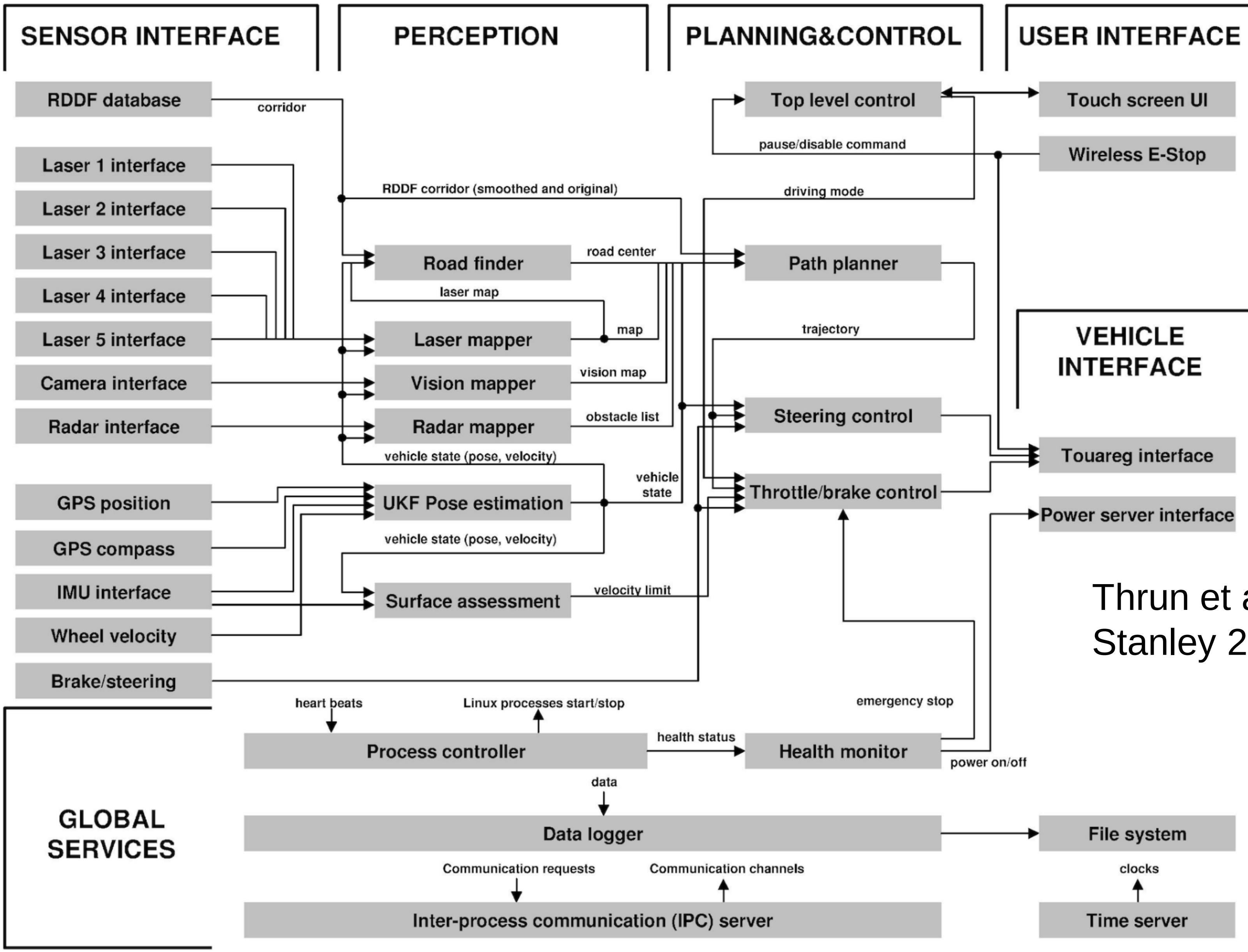


b. Top view of vechicle



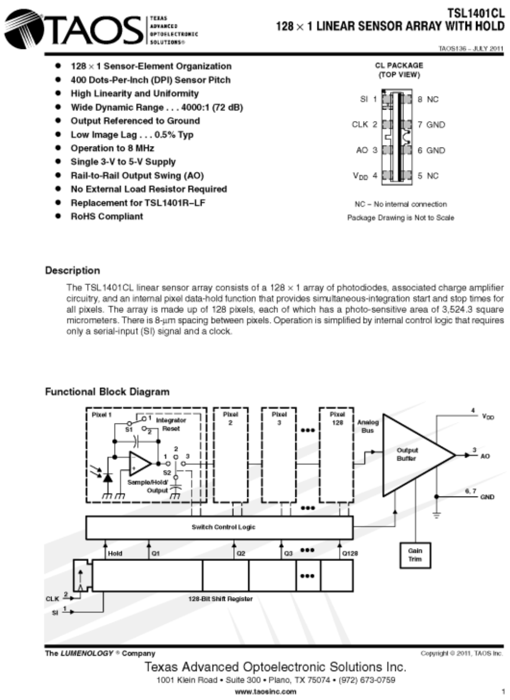
c. Include a labelled photo which indicates good lo

Block Diagram/Software Model



Thrun et al
Stanley 2005

Input/Output



TAOS TEXAS ADVANCED OPTOELECTRONIC SOLUTIONS

TSL1401CL
128 × 1 LINEAR SENSOR ARRAY WITH HOLD

TAOS136 – JULY 2011

- 128 × 1 Sensor-Element Organization
- 400 Dots-Per-Inch (DPI) Sensor Pitch
- High Linearity and Uniformity
- Wide Dynamic Range . . . 4000:1 (72 dB)
- Output Referenced to Ground
- Low Image Lag . . . 0.5% Typ
- Operation to 8 MHz
- Single 3-V to 5-V Supply
- Rail-to-Rail Output Swing (AO)
- No External Load Resistor Required
- Replacement for TSL1401R–LF
- RoHS Compliant

NC – No internal connection
Package Drawing is Not to Scale

Description

The TSL1401CL linear sensor array consists of a 128 × 1 array of photodiodes, associated charge amplifier circuitry, and an internal pixel data-hold function that provides simultaneous-integration start and stop times for all pixels. The array is made up of 128 pixels, each of which has a photo-sensitive area of 3,524.3 square micrometers. There is 8-μm spacing between pixels. Operation is simplified by internal control logic that requires only a serial-input (SI) signal and a clock.

Functional Block Diagram

The LUMENOLOGY ® Company

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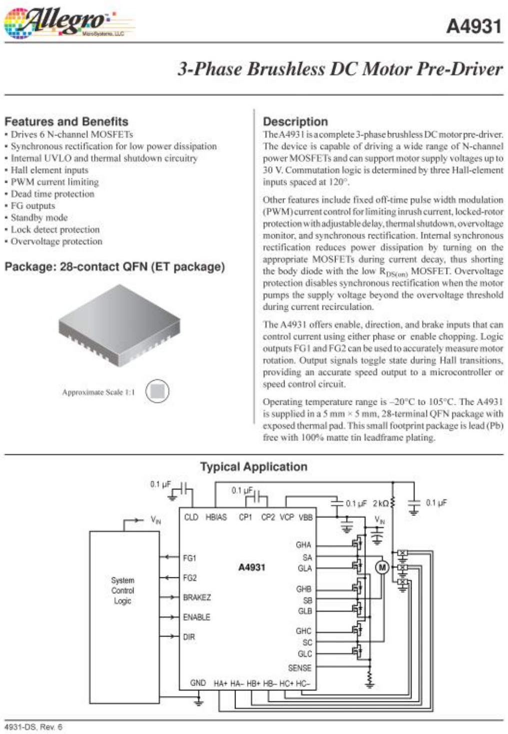


Allegro MicroSystems, LLC

A4931

3-Phase Brushless DC Motor Pre-Driver

Features and Benefits

- Drives 6 N-channel MOSFETs
- Synchronous rectification for low power dissipation
- Internal UVLO and thermal shutdown circuitry
- Hall element inputs
- PWM current limiting
- Dead time protection
- FG outputs
- Standby mode
- Lock detect protection
- Overvoltage protection

Package: 28-contact QFN (ET package)

Approximate Scale 1:1

Description

The A4931 is a complete 3-phase brushless DC motor pre-driver. The device is capable of driving a wide range of N-channel power MOSFETs and can support motor supply voltages up to 30 V. Commutation logic is determined by three Hall-element inputs spaced at 120°.

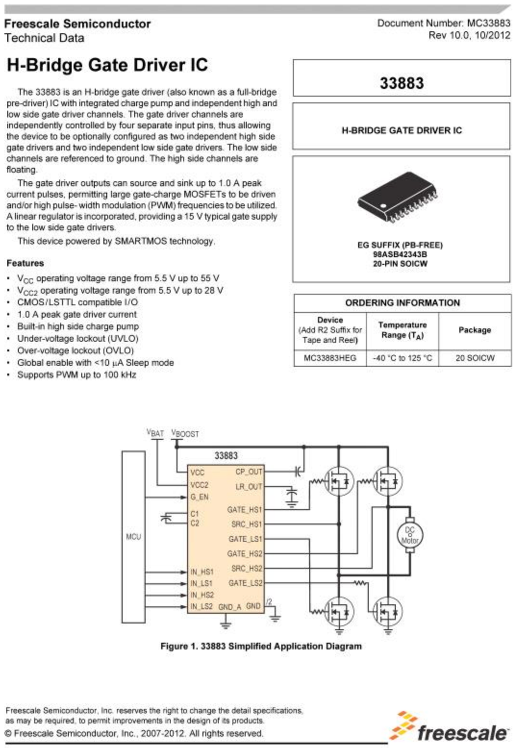
Other features include fixed off-time pulse width modulation (PWM) current control for limiting inrush current, locked-rotor protection with adjustable delay, thermal shutdown, overvoltage monitor, and synchronous rectification. Internal synchronous rectification reduces power dissipation by turning on the appropriate MOSFETs during current decay, thus shorting the body diode with the low $R_{DS(on)}$ MOSFET. Overvoltage protection disables synchronous rectification when the motor pumps the supply voltage beyond the overvoltage threshold during current recirculation.

The A4931 offers enable, direction, and brake inputs that can control current using either phase or enable chopping. Logic outputs FG1 and FG2 can be used to accurately measure motor rotation. Output signals toggle state during Hall transitions, providing an accurate speed output to a microcontroller or speed control circuit.

Operating temperature range is –20°C to 105°C. The A4931 is supplied in a 5 mm × 5 mm, 28-terminal QFN package with exposed thermal pad. This small footprint package is lead (Pb) free with 100% matte tin leadframe plating.

Typical Application

4931-DS, Rev. 6



Freescale Semiconductor
Technical Data

Document Number: MC33883
Rev 10.0, 10/2012

H-Bridge Gate Driver IC

33883

H-BRIDGE GATE DRIVER IC

The 33883 is an H-bridge gate driver (also known as a full-bridge pre-driver) IC with integrated charge pump and independent high and low side gate driver channels. The gate driver channels are independently controlled by four separate input pins, thus allowing the device to be optionally configured as two independent high side gate drivers and two independent low side gate drivers. The low side channels are referenced to ground. The high side channels are floating.

The gate driver outputs can source and sink up to 1.0 A peak current pulses, permitting large gate-charge MOSFETs to be driven and/or high pulse- width modulation (PWM) frequencies to be utilized. A linear regulator is incorporated, providing a 15 V typical gate supply to the low side gate drivers.

This device powered by SMARTMOS technology.

Features

- V_{CC} operating voltage range from 5.5 V up to 55 V
- V_{CC2} operating voltage range from 5.5 V up to 28 V
- CMOS/LSTTL compatible I/O
- 1.0 A peak gate driver current
- Built-in high side charge pump
- Under-voltage lockout (UVLO)
- Over-voltage lockout (OVLO)
- Global enable with <10 μA Sleep mode
- Supports PWM up to 100 kHz

EG SUFFIX (PB-FREE)
98ASB42343B
20-PIN SOICW

ORDERING INFORMATION		
Device (Add R2 Suffix for Tape and Reel)	Temperature Range (T_A)	Package
MC33883HEG	-40 °C to 125 °C	20 SOICW

Figure 1. 33883 Simplified Application Diagram

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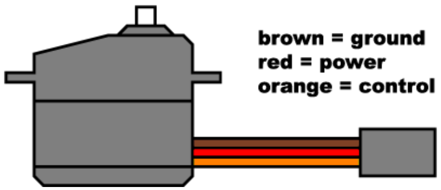
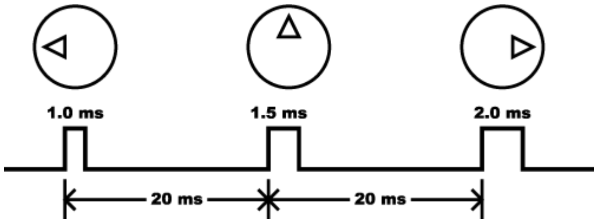
freescale





https://www.sparkfun.com/tutorials/283

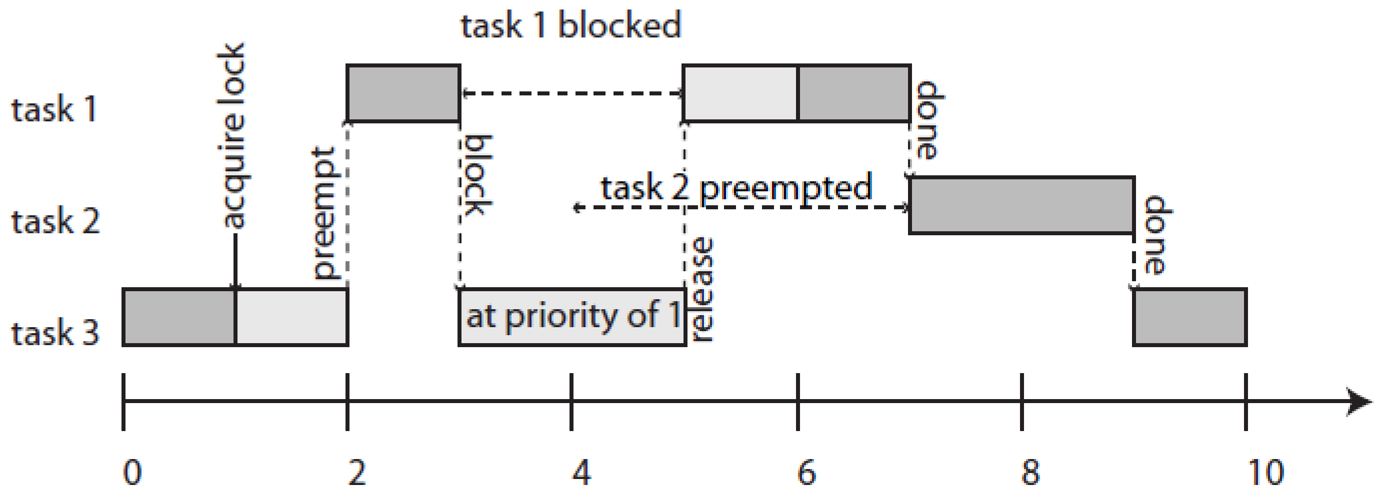
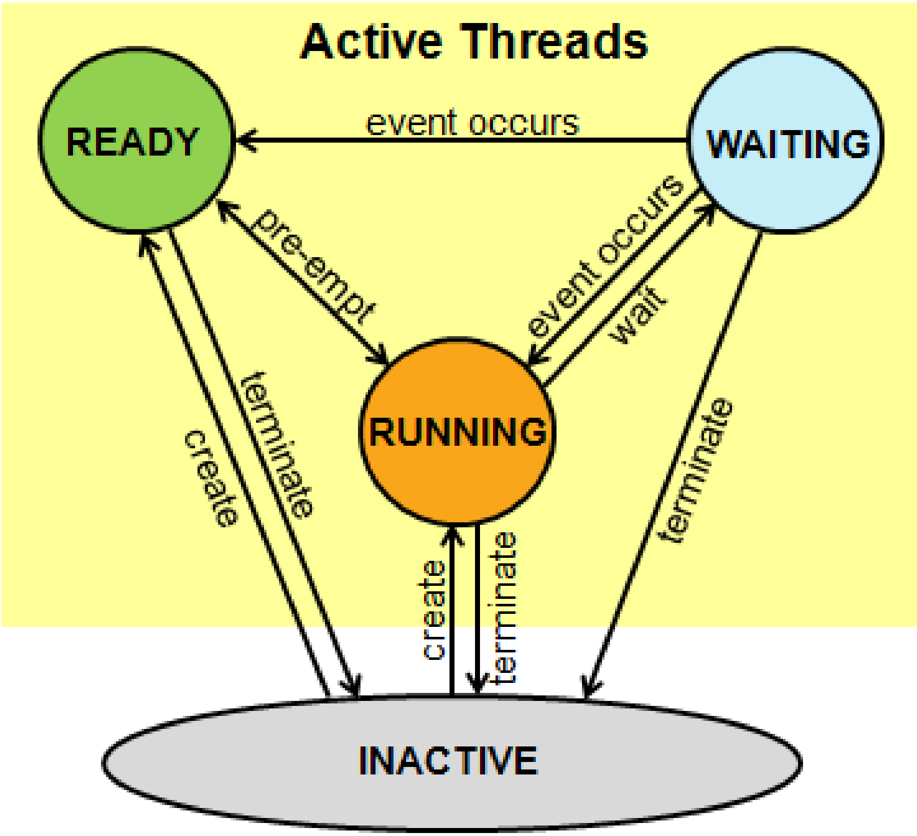
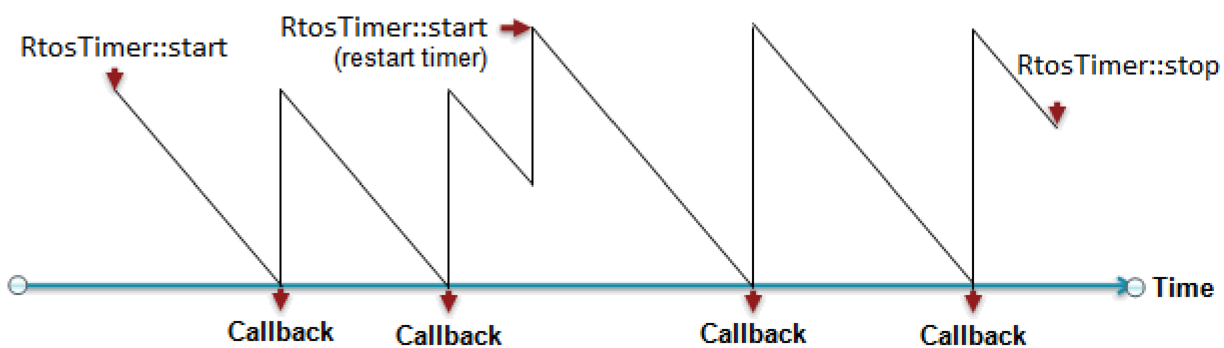


Figure 12.10: Illustration of the priority inheritance protocol. Task 1 has highest priority, task 3 lowest. Task 3 acquires a lock on a shared object, entering a critical section. It gets preempted by task 1, which then tries to acquire the lock and blocks. Task 3 inherits the priority of task 1, preventing preemption by task 2.



https://developer.mbed.org/handbook/RTOS

os_time: very useful for measuring execution time



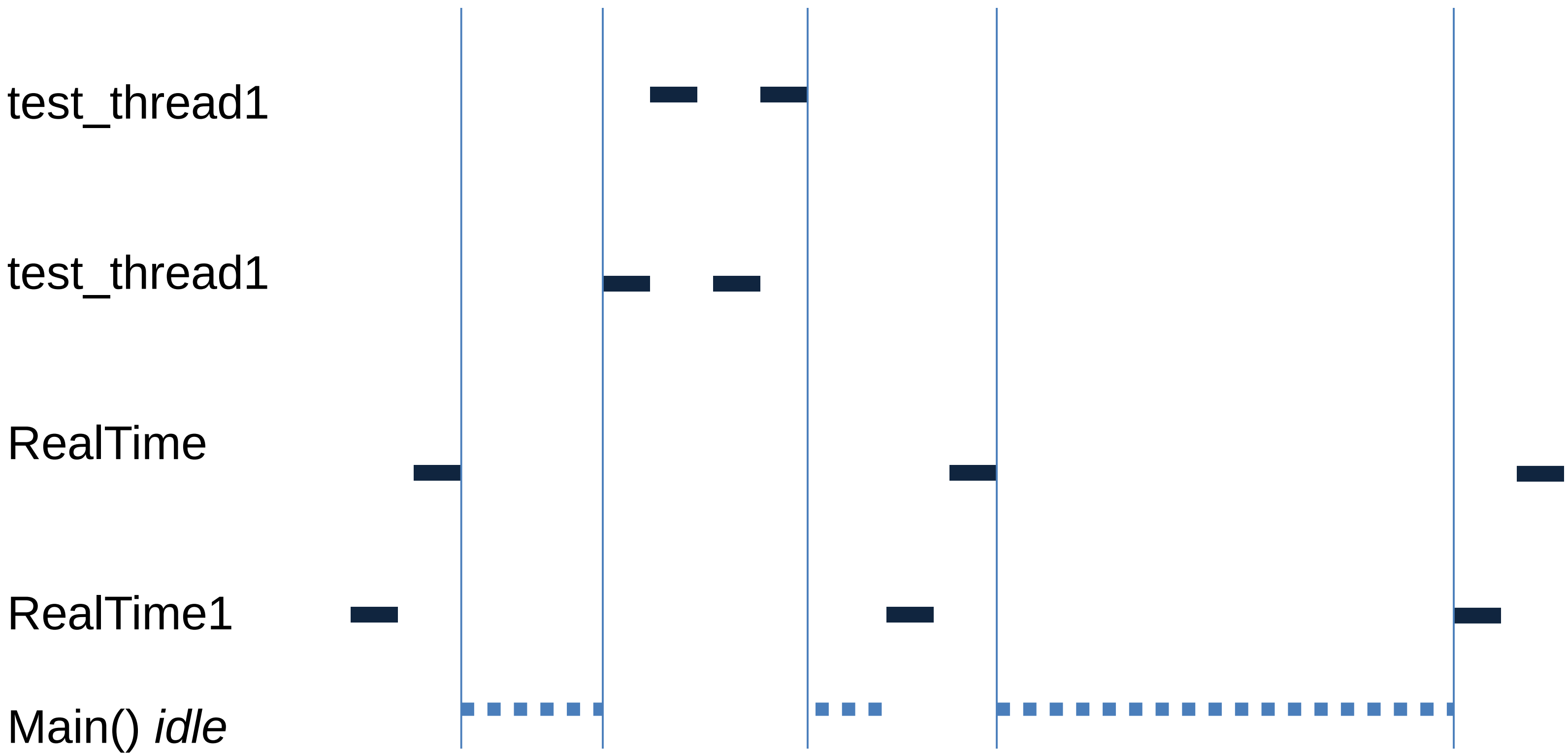
```
returnCode = SysTick_Config ((uint32_t)(SystemCoreClock /
10000)); //100us granularity
// start a thread to handle printing without blocking
      Thread printThread(print_thread);

// Start some threads running character printing
      Thread testThread(test_thread);
      Thread testThread1(test_thread1);

// start real time clock at 200 us NOTE only need 1 main
RT ``super loop''
/*** CAUTION - this gets BLOD at 200 us ***/

      RtosTimer realTimeTimer(RealTime);
      realTimeTimer.start(2); // .2 millisecond timing
      // second rtos with no calculations
      RtosTimer realTimeTimer1(RealTime1);
      realTimeTimer1.start(2); // 0.2 millisecond timing
```

RTOS timer and threads example



LED Port Information

1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB_DP}	USB_DP input voltage	–0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	–0.3	3.63	V
V_{REGIN}	USB regulator input	–0.3	6.0	V

Table 7. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad (except $\overline{RESET}$) • $2.7 V \leq V_{DD} \leq 3.6 V$, $I_{OH} = -5 mA$ • $1.71 V \leq V_{DD} \leq 2.7 V$, $I_{OH} = -1.5 mA$	 $V_{DD} - 0.5$ $V_{DD} - 0.5$	 — —	 V V	1, 2
V_{OH}	Output high voltage — High drive pad (except $\overline{RESET}$) • $2.7 V \leq V_{DD} \leq 3.6 V$, $I_{OH} = -18 mA$ • $1.71 V \leq V_{DD} \leq 2.7 V$, $I_{OH} = -6 mA$	 $V_{DD} - 0.5$ $V_{DD} - 0.5$	 — —	 V V	1, 2
I_{OHT}	Output high current total for all ports	—	100	mA	—
V_{OL}	Output low voltage — Normal drive pad • $2.7 V \leq V_{DD} \leq 3.6 V$, $I_{OL} = 5 mA$ • $1.71 V \leq V_{DD} \leq 2.7 V$, $I_{OL} = 1.5 mA$	 — —	 0.5 0.5	 V V	1
V_{OL}	Output low voltage — High drive pad • $2.7 V \leq V_{DD} \leq 3.6 V$, $I_{OL} = 18 mA$ • $1.71 V \leq V_{DD} \leq 2.7 V$, $I_{OL} = 6 mA$	 — —	 0.5 0.5	 V V	1
I_{OLT}	Output low current total for all ports	—	100	mA	—
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	μA	3
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	μA	3
I_{IN}	Input leakage current (total all pins) for full temperature range	—	65	μA	3
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	—
R_{PU}	Internal pullup resistors	20	50	kΩ	4
R_{PD}	Internal pulldown resistors	20	50	kΩ	5

Motor Model

On board….