EECS192 Lecture 12
Apr. 16, 2019

Notes:
1. Mon. 4/29: (Mon 5-6? pm) round 2 (NATCAR rules)
   1. 13 makes first turn
   2. 15 ½ track in < 5 minutes
   3. 16 whole track in < 5 minutes
   4. 18 whole track in less than 120 sec (1.1 m/s)
   5. 20 CW+CCW in < 70 sec (less deductions)
2. Thanks for CalDay (Teams 1,2,3,5,6)
3. Quiz 5 on 4/22 on steering control

Topics
• Round 1 results
• Round 2 notes
• Hardware Robustness
• Progress report notes
• Steering discussion
• C.O.P. Watchdog/Software Robustness
• Supervisor Systems
• Digital Filtering
Spring 2019 Round 1 Results

Whole track <60 seconds (9+ pts):
N=8 (28.565, 32.65, 34.26, 34.457, 38.68, 40.656, 46.156, 46.812)

Whole track > 60 seconds: N=1 (67.193)

9 teams
Track length - ~ 65 meters. Top speed 2.3 m/sec
Spring 2018 Round 1 Results

Whole track <60 seconds (9+ pts): N=2 (50.25 sec, 53.19 sec)
Whole track (9 pts): N=2 (60.89, 73.03)
¾ track (8.5 pts): N=1
½ track (8 pts): team
¼ track (7.5): N=2
2 turns, or turn+steps (7 pts):
1 turn (6.5 pts): 4, 6, 7
Moves (6 pts): N=2

9 teams
Track length - ~ 65 meters. Top speed 1.3 m/sec
Cones +2 second

Finish line: The start/finish line will be marked with two 4-inch-long segments of 1-inch-wide white tape that are parallel to the track with 1-inch spacing, as shown in the figure below.

The car must automatically stop within 6 feet of the finish line after finishing the race.

A penalty of 4 seconds will be added to the lap time for any car that does not automatically stop within the required region.
Round 2 notes

-0.5 points  Twitchy steering
-0.5 points  Goes wide on curves
-0.5 points  Oscillatory step response
-1 point     Loose hardware including car scraping on track
-1 point     Hits cone(s)
-0.5 points  Overshoot Natcar Finish Line (6 ft after finish line)
             + 4 second penalty in lap time
Lessons Learned

Lessons Learned:
• Extreme lighting variation ➔
  Need AGC,
  steering hold,
  Autocalibration
• Camera mechanics- dragging
• Track vs terrain features
• Self-shadow

What worked well:
• Velocity control?
• Stability decent
• Car electromechanics
• No DoA cars
• No random resets or runaway cars
• No tank cars
• Crossings ok
Automatic Gain Control

In all the discussion that follows, we will be using one-shot imaging.
Hardware Robustness

• Mechanical oscillations
• Lock washers
• Strain relief on connections
  – (stranded vs solid core wire)
PWM for Steering Servo

Gotchas:
- 4.8 or 6V, (Not 7.2V!)
- max current 2A
- May be sensitive to noise on supply line
- Performance depends on voltage
- Period < 5 ms???
- Driving past mechanical stop
1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Digital supply voltage</td>
<td>$-0.3$</td>
<td>$3.8$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Digital supply current</td>
<td>$-$</td>
<td>$1.0$</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{IO}$</td>
<td>IO pin input voltage</td>
<td>$-0.3$</td>
<td>$V_{DD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{D}$</td>
<td>Instantaneous maximum current single pin limit (applies to all port pins)</td>
<td>$-25$</td>
<td>$25$</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{DDA}$</td>
<td>Analog supply voltage</td>
<td>$V_{DD} - 0.3$</td>
<td>$V_{DD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{USB_DP}$</td>
<td>USB_DP input voltage</td>
<td>$-0.3$</td>
<td>$3.63$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{USB_DM}$</td>
<td>USB_DM input voltage</td>
<td>$-0.3$</td>
<td>$3.63$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{REGIN}$</td>
<td>USB regulator input</td>
<td>$-0.3$</td>
<td>$6.0$</td>
<td>V</td>
</tr>
</tbody>
</table>

LATCHUP!

- 3.3V
- 3.3V
- 1K
Latchup phenomena

Protection circuit
Progress report notes

• Motor snubber caps
• E-stop
• G_EN on mc338833 (sleep mode- need pull down?)
Steering discussion - given $v = 3 \text{ m/s}$

$$\delta = k_p y_a + k_d \frac{dy_a}{dt} + k_i \text{ integral}(y_a)$$

$k_p = \boxed{400} \text{ deg/m}$,

$k_i = \boxed{0} \text{ deg/ m-s}$,

$k_d = \boxed{60} \text{ deg/m/s}$

$k_p = \boxed{100} \text{ deg/m}$,

$k_i = \boxed{300} \text{ deg/ m-s}$,

$k_d = \boxed{30} \text{ deg/m/s}$
Steering discussion - given $v = 3 \text{ m/s}$

$$\delta = k_p \gamma_a + k_d \frac{d\gamma_a}{dt} = (400)(0.04) + k_d 0 = 16 \text{ degrees}$$

$k_p = \_400\_ \text{ deg/m}$, \hspace{1cm} $k_i = \_0\_ \text{ deg/m-s}$, \hspace{1cm} $k_d = \_60\_ \text{ deg/m/s}$
Steering discussion

\[ \delta = k_p y_a + k_d \frac{dy_a}{dt} + k_i \text{integral}(y_a) \]

- \( k_p = 100 \) deg/m
- \( k_i = 300 \) deg/m-s
- \( k_d = 30 \) deg/m/s

Steady state error

\( \pi r \approx 3m \rightarrow 1 \text{ sec} \)
C.O.P. Watchdog timer

- Despite extensive software and hardware testing, faults will still occur in real devices. Even momentary noise spikes on a power supply can lock up a processor occasionally. Such events will occur on the power grid several times a year. Watchdog timers provide a last line of defense to prevent system failure with minimal hardware cost.

- https://developer.mbed.org/cookbook/WatchDog-Timer
ARM Cortex A8 Overview

Beaglebone Blue
TI Sitara™ AM335x Processors
ARM Cortex A8
4GB Flash
512 MB RAM
32 bit ARM 7 core
1 GHz
A/D
3x SPI
Timers
WiFi
USB
microSD card
Watch Dog Timer

Figure 20-94. 32-Bit Watchdog Timer Functional Block Diagram

Watchdog timer

Prescaler
(1:128 ratio)

Counter
(32-bit)

Registers

Interrupt
generation

L4 interface

RESET

IRQ
20.4.3.5 Overflow/Reset Generation

When the watchdog timer counter register (WDT_WCCR) overflows, an active-low reset pulse is generated to the PRCM module. This RESET pulse causes the PRCM module to generate global WARM reset of the device, which causes the nRESETIN_OUT pin to be driven out of the device. This pulse is one prescaled timer clock cycle wide and occurs at the same time as the timer counter overflow.

After reset generation, the counter is automatically loaded with the value stored in the watchdog load register (WDT_WLDR) and the prescaler is reset (the prescaler ratio remains unchanged). When the reset pulse output is generated, the timer counter begins incrementing again.

Figure 20-95 shows a general functional view of the watchdog timers.

Figure 20-95. Watchdog Timers General Functional View
To start and stop a watchdog timer, access must be made through the start/stop register (WDT_WSPR) using a specific sequence. To disable the timer, follow this sequence:
1. Write XXXX AAAAh in WDT_WSPR.
2. Poll for posted write to complete using WDT_WWPS.W_PEND_WSPR.
3. Write XXXX 5555h in WDT_WSPR.
4. Poll for posted write to complete using WDT_WWPS.W_PEND_WSPR.

To enable the timer, follow this sequence:
1. Write XXXX BBBBh in WDT_WSPR.
2. Poll for posted write to complete using WDT_WWPS.W_PEND_WSPR.
3. Write XXXX 4444h in WDT_WSPR.
4. Poll for posted write to complete using WDT_WWPS.W_PEND_WSPR. All other write sequences on the WDT_WSPR register have no effect on the start/stop feature of the module.
Software Robustness

• Checksums for bit rot
• Watch dog timer/computer operating properly COP
• Lost track detection
• Autocalibration at startup
  – (sanity check for steering angle vs line error)
  – AGC
• State Observer/estimator
• Discrete State observer
FSM Recognizer (generalized WDT)

State 1
- Left turn, velocity
- Right turn
- Time out

State 2
- Time out
Digital Filtering

• Moving average
  \[ y_{1[n]} = \frac{y[n-2]+y[n-1]+y[n]}{3} \]

• Median filter (outlier rejection)

• Notch filter (mechanical vibration)
  \[ y[n] = \frac{x[n-2]+2x[n-1]+x[n]}{4} \]

• Model based filtering (or Kalman filter)

(on board)
Round 1 Results

- **2015**: 48.14, 46.56, 67.93, DNF, 53.72, 85.51, 40.37, 40.24, 41.61, DNF, 62.88, 45.59

- **2016**: 33.61, 42.32, 42.48, 42.83, 55.14, 62.59, 66.72, 67.69, 140.01, DNF,

Round 1 time