EE 240B discussion 5

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Folding cascode stage sizing?

- **NOTE**: tail NMOS sinks currents of both input and output stage.
- What should the input/output stage current ratio be?
Folded Cascode Analysis

• What is the DC gain, dominant pole, and second order pole of this amplifier?
Folded Cascode Analysis

• Two ways of computing the DC gain: stage-by-stage inspection analysis, or input black-boxing.
• The poles are effectively separated; easy to compute. Remember to short dominant pole before computing second/third order poles!
As you size up the entire amplifier:

– How does the dominant pole change?
– How does the second/third order pole change?
• Since second/third order poles are isolated, they don’t change that much when entire amplifier is sized up.
  – Still moves a little because of imperfect separation.
• Strategy: from unit-amplifier gain and second/third order pole location, find lowest dominant pole to meet settling time, then size entire amplifier up.
Computing settling time

• It’s 2018; don’t use inverse laplace transforms / hand-wavy approximations.

• `scipy.signal.step()` computes step response given (numerator, denominator) of transfer function.

• Can use `scipy.interpolate.InterpolatedUnivariateSpline` and `scipy.optimize.brentq()` to find exact intersection time.
  
  – Reduce numerical errors.
Example optimal settling

• Intersects error bars at exactly two points, which allows for maximum ringing.
Unit Amplifier design

- Consider the load PMOS first.
- Assume $V_{in}^*$ given, $r_{on} = r_{op}/3$, and ignore pole associated with NMOS.
  - Some of these assumptions are clearly wrong, but we just want to figure out the tradeoffs, so this is OK.
- How many degrees of freedom does the load PMOS have?
PMOS Load tradeoffs \((V_{bot}^*)\)

- Load uniquely determined by \(V_{bot}^*, V_{DS,bot}, \text{ and } N_{casc}\).
- Left shows various metrics \(v.s. V_{bot}^* \) and \(V_{DS,bot}\).
- Always want largest \(V_{bot}^*\) and largest \(V_{DS,bot}\) (for this technology at least).
  - Thus we can eliminate \(V_{DS,bot}\) if we’re doing blind sweeping.
  - Output swing spec will eventually limit these values.
PMOS Load tradeoffs ($N_{casc}$)

- Left shows various metrics v.s. $N_{casc}$ and $V_{DS,bot}$
- Large $N_{casc}$ improves gain at the cost of lowering second order pole.
  - An optimal exists given settling time.
- Note that usually the PMOS internal pole is $3^{rd}$ order, so we want to have some margin.
- This procedure can similarly be repeated to the NMOS/input stages.
BAG’s LTICircuit

- As circuits get more complicated, it’s harder and harder to match calculation with simulation.
  - Did you do your math right? Did you simplify too much? Does body effect matter?
  - For this technology, ignoring body effect results in 11% DC gain error.

- **bag.data.lti.LTICircuit** is a Python AC circuit solver that makes AC analysis/small-signal transient easy.
  - Works with MOSDBDiscrete transistor bias information dictionary.
  - Guarantees accurate AC transfer function computation.
  - **NOTE**: ignores all nonlinear effects! Should only trust transient output with small input.

- Sample script **lti_circuit_sample.py** uploaded to hw2_soln branch.