Preliminaries

• This will be the first in a series of design methodologies we will develop
  • To keep the discussion manageable, will generally assume that only a couple of specifications are critical
  • And that all other specs will “automatically” be met
  • In practice, can inspect specs and technology capabilities to figure out which constraints are really active, and utilize the appropriate methodology

• Will largely ignore biasing details for now
  • But will patch this later
CS Amplifier Design Methodology

- Input specifications:
  - Minimum small signal gain $A_v$
  - Minimum 3dB bandwidth $\omega_{bw}$
  - Fixed capacitive load $C_L$
  - Supply voltage $V_{dd}$

- Goal: minimize power

- What are our design variables?
Power and $g_m$

First Pass Methodology
Side Discussion: Digital vs. Analog Power

\[ P_{\text{digital}} = \alpha_0 \cdot \frac{V_{DD}}{2} f_{\text{clk}} \quad P_{\text{analog}} = \frac{1}{2} C \cdot V_{DD} \cdot V^* \cdot A \cdot \omega_{\text{bw}} \]

• What needs to be true for analog to be lower power than digital?

\[ g_m \text{ vs. } GBW \text{ revisited (1)} \]
$g_m$ vs. GBW revisited (2)

$g_m$ vs. GBW revisited (3)
Direct Implication

\[ I_D = \frac{1}{2} \left( \frac{A_T \omega_{bw} V^* C_L}{1 - A_T \omega_{bw} / (\omega_T / \gamma)} \right) \]

- For a given \( V^* \), there is a maximum GBW you can achieve
  - No matter how much power you spend, cannot exceed this limit (with this topology)

Methodology Take 2
Methodology Take 2

What about $r_o$?
Bias Point

Extension #1: Differential Amplifier
Extension #2: Multi-Stage Amplifier

Extension #3: “Inverter” Amplifier