Comparator

• Specs and issues:
  • Clock rate $f_s$
  • Offset
  • Resolution
  • Hysteresis
  • Input cap

  • Power dissipation
  • CM rejection
  • Kickback noise
  • ...

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Comparator Gain-Bandwidth

Example:

- 10Gb/s link
- Minimum ΔV: 1mV
- Vdd = 1V

→ \( A_v > \frac{1V}{1mV} = 1000 \) in < 100ps!

Operational Amplifier?

![Graph showing the relationship between frequency and gain]

\[
f_{-3dB} = \frac{f_u}{A_v} = \frac{2}{3} \frac{1}{T_{bit}}
\]

\[
f_u = \frac{2A_v}{3T_{bit}} = \frac{2 \times 1000}{3 \times 100\text{ps}} = 6.67\text{THz}
\]
Open-Loop Amplifier Cascade

Cascaded Amplifier

- Simplified bandwidth analysis:
  - Open-circuit time constants
  - (Not most accurate, but leads to nearly the right answer for design optimization)
Bandwidth/Gain Optimization
Power Consumption

Regenerative Latch
CML Comparator (Latch)

CML Comparator Analysis (1)
CML Comparator Analysis (2)

CML Comparator Design