inst.eecs.berkeley.edu/~ee241b

EE241B : Advanced Digital Circuits

Lecture 1 – Introduction

Borivoje Nikolić

Tuesdays and Thursdays 9:30-11am

293 Cory

Class Goals and Expected Outcomes

Practical Information

- **Instructor:**
  - **Borivoje Nikolić**

    509 Cory Hall , 3-9297, bora@eecs

    Office hours: Tu 11am-12pm or by appointment
- **GSI:**
  - **Daniel Grubb dpgrubb@berkeley**

Class Discussion
http://piazza.com/berkeley/spring2020/ee241b
Sign up for Piazza!
Class Web page
inst.eecs.berkeley.edu/~ee241b

Class Topics

- This course aims to convey a knowledge of advanced concepts of digital circuit and system design in state-of-the-art technologies.
  - Emphasis is on the circuit and chip design and optimization for both energy efficiency and high performance for use in applications such as microprocessors, signal and multimedia processors, communications, memory and periphery. Special attention will be devoted to the most important challenges facing digital circuit designers today and in the coming decade, being the impact of slowdown in scaling, nanoscale effects, variability, power-limited design and timing.
- We will use qualitative analysis when practical
- Many case studies

EECS251A vs. EE241B

- EECS 251A:
  - Emphasis on digital logic design
  - (Very) basic transistor and circuit models
  - Basic circuit design styles
  - First experiences with design – creating a solution given a set of specifications
  - A complete pass through the design process
- EE 241B (likely 251B from next year):
  - Understanding of technology possibilities and limitations
  - Transistor models of varying accuracy
  - Design under constraints: power-constrained, flexible, robust,…
  - Learning more advanced techniques
  - Study the challenges facing design in the coming years
  - Creating new solutions to challenging design problems, design exploration

Special Focus in Spring 2020

- Current technology issues
- Process variations
- Robust design
- Memory
- Energy efficiency
- Power management
- SoC components
- (Circuits for machine learning)

Class Topics

- Module 1: Fundamentals – Current technologies (1.5 wks)
- Module 2: Models – From devices to gates, logic and standard cells (3 wks)
- Module 3: Design for performance (1.5 wks)
- Module 4: Memory, SRAM, variability, scaling options (2.5 wks)
- Module 5: Energy-efficient design (3 wks)
- Module 6: Clock and power distribution (1 week)
- Project presentations, final exam (1 week)

Class Organization

- 4 (+/-) assignments (20%)
- 4 quizzes (10%)
- 1 term-long design project (40%)
  - Phase 1: Topic selection (Feb 20, after ISSCC)
  - Phase 2: Study (report by March 19, before Spring break)
  - Phase 3: Design (report in RRR week)
  - Presentations, May 4, afternoon
- Final exam (30%) (Thursday, April 30, in-class)

Class Material

- Recommended text: J. Rabaey, "Low Power Design Essentials," Springer 2009.
  - Available at www.springerlink.com
- Other reference books:
  - "VLSI Design Methodology Development" by, T. Dillinger, Pearson 2019.
  - "Design of High-Performance Microprocessor Circuits," edited by A. Chandrakasan, W. Bowhill, F. Fox (available on-line at Wiley-IEEE), Wiley 2011.
  - "CMOS VLSI Design," 4th ed, by N.Weste, D. Harris
  - "Digital Integrated Circuits - A Design Perspective", 2nd ed. by J. M. Rabaey, A. Chandrakasan, B. Nikolić, Prentice-Hall, 2003.

Class Material

- List of background material available on website
- Selected papers will be made available on website
  - Linked from IEEE Xplore and other resources
  - Need to be on campus to access, or use library proxy, library VPN (check http://library.berkeley.edu)
- Class notes on website
  - No printed handouts in class!

Reading Assignments

- Three types of readings:
  - Assigned reading, that should be read before the class
  - Recommended reading that covers the key points covered in lecture in greater detail
  - Occasionally, background material will be listed as well

Reading Sources

- IEEE Journal of Solid-State Circuits (JSSC)
- IEEE International Solid-State Circuits Conference (ISSCC)
- Symposium on VLSI Circuits (VLSI)
- Other conferences and journals

Project Topics

- Focus this semester: Memories, Circuits for ML
- Design components that are very efficient in running matrix multiplications and convolutions.
  - Logic, in-memory computing
  - Build a complete system based on RISC-V Rocket
  - Negative results are ok
- Project teams: 2+ members, proportional to the size of the project
- More details in Week 2

Tools

- 7nm predictive model (ASAP7), with (mostly) complete design kit
- HSPICE
  - You need an instructional (or research) account
- Cadence, Synopsys, available on instructional servers
- Other predictive sub-100nm models
  - Such as SAED32

Webcast

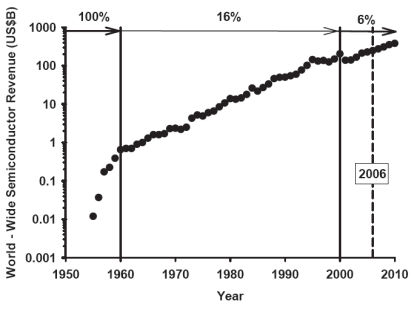
- No recording! Focus on interactive lectures.
- Course notes available in advance.
- Be engaged in the discussions. You are part of the learning process.

Trends and Challenges in Digital Integrated Circuit Design

Reading (Lectures 1 & 2)

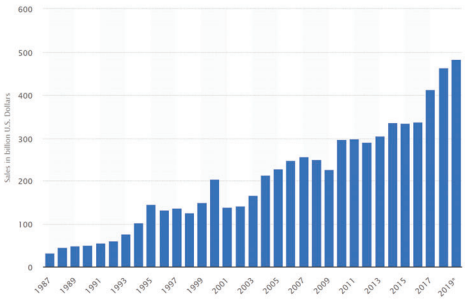
- Assigned
  - Rabaey, LPDE, Ch 1 (Introduction)
  - G.E. Moore, *No exponential is forever: but "Forever" can be delayed!* Proc. ISSCC'03, Feb 2003.
  - T.-C. Chen, *Where CMOS is going: trendy hype vs. real technology.* Proc. ISSCC'06, Feb 2006.
- Recommended
  - Chandrakasan, Bowhill, Fox, Chapter 1 – Impact of physical technology on architecture (J.H. Edmondson),
  - Chandrakasan, Bowhill, Fox, Chapter 2 – CMOS scaling and issues in sub-0.25µm systems (Y. Taur)
  - S. Borkar, "Design challenges of technology scaling," IEEE Micro, vol.19, no.4, p.23-29, July-Aug. 1999.
- Background: Rabaey et al, DIC Chapter 3.
- The contributions to this lecture by a number of people (J. Rabaey, S. Borkar, etc) are greatly appreciated.

Semiconductor Industry Revenues



M. Chang, "Foundry Future: Challenges in the 21st Century," ISSCC'2007

Current State of Semiconductor Industry



Current GWP ~ 78,000 billion

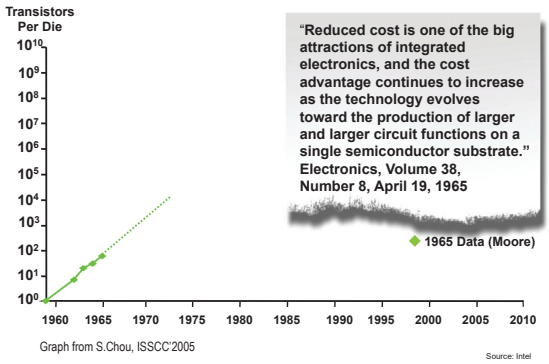
Source: Statista

Moore's Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 12 months.
- He made a prediction that semiconductor technology will double its effectiveness every ~~12~~ ~~18~~ 24 months

"*The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term, this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000.*"
Gordon Moore, Cramming more Components onto Integrated Circuits, (1965).

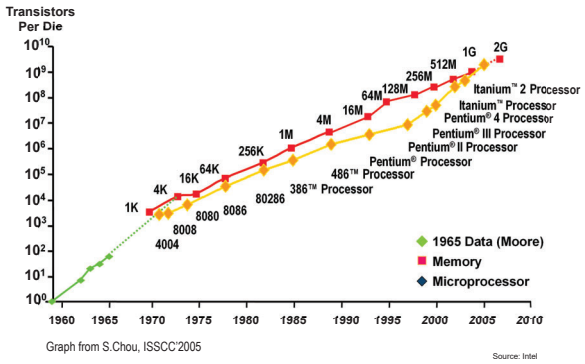
Moore's Law - 1965



Graph from S.Chou, ISSCC'2005

Source: Intel

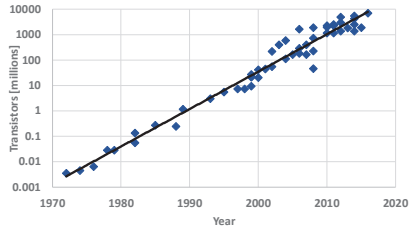
Moore's Law - 2005



Graph from S.Chou, ISSCC'2005

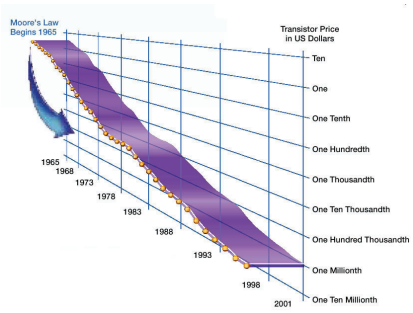
Source: Intel

Moore's Law - 2018

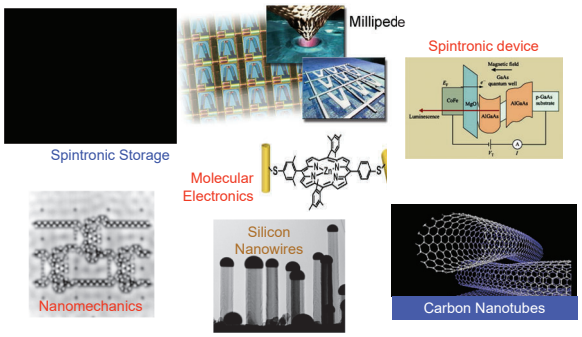


- Slowdown is apparent, but scaling continues

Moore's Law and Cost

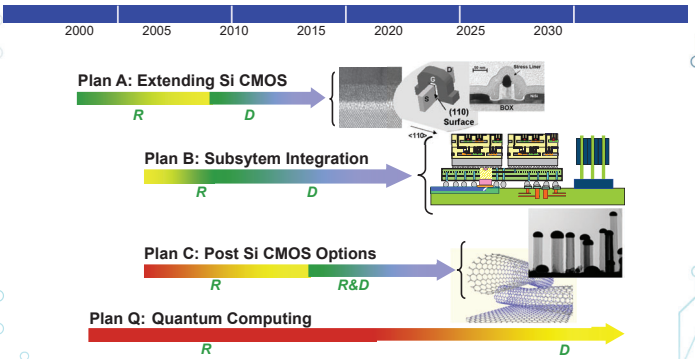


Progress in Nano-Technology



T.C. Chen, Where Si-CMOS is going: Trendy Hype vs. Real Technology, ISSCC'06

Technology Strategy / Roadmap



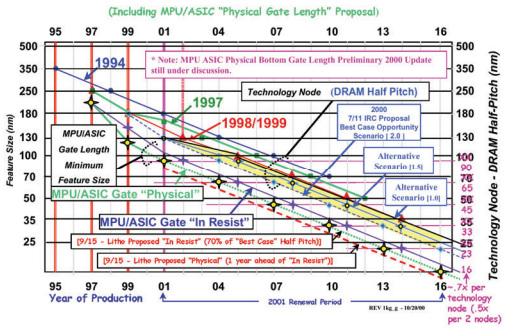
T.C. Chen, Where Si-CMOS is going: Trendy Hype vs. Real Technology, ISSCC'06

Technology Evolution

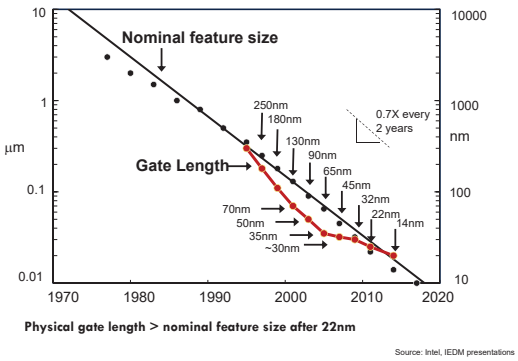
International Technology Roadmap for Semiconductors - 2003 data

Year	2004	2007	2010	2013	2016
Dram ½ pitch [nm]	90	65	45	32	22
MPU transistors/chip	550M	1100M	2200M	4400M	8800M
Wiring levels	10-14	11-15	12-16	12-16	14-18
High-perf. physical gate [nm]	37	25	18	13	9
High-perf. V_{DD} [V]	1.2	1.1	1.0	0.9	0.8
Local clock [GHz]	4.2	9.3	15	23	40
High-perf. power [W]	160	190	220	250	288
Cost-perf. power [W]	84	104	120	138	158
Low-power V_{DD} [V]	0.9	0.8	0.7	0.6	0.5
'Low-power' power [W]	2.2	2.5	2.8	3.0	3.0

Roadmap Acceleration in the Past



Printed vs. Physical Gate

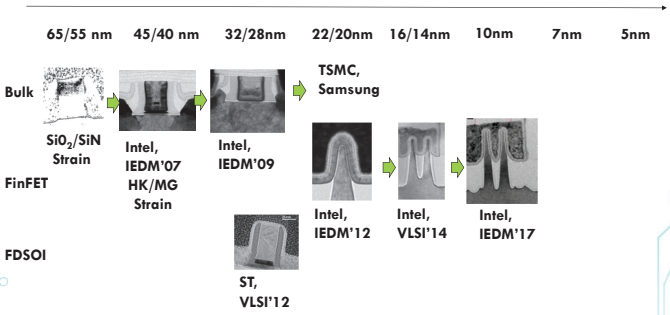


Physical gate length > nominal feature size after 22nm

Source: Intel, IEDM presentations

Transistors are Changing

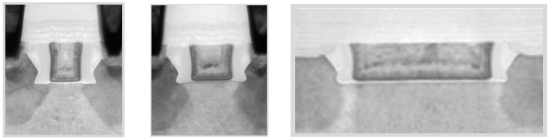
- From bulk to finFET and FDSOI



Varying Flavors in Each Node

- 32nm (and 28nm): Various flavors - Intel

Logic Transistor	Low Power Transistor	HV I/O Transistor
(HP or SP)	(LP)	(1.8 V or 3.3 V)



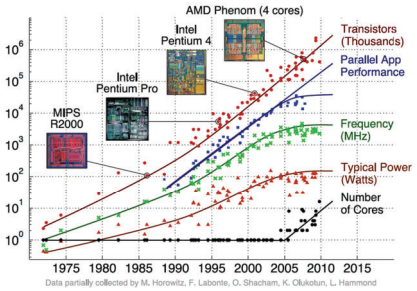
Lg = 30/34nm | Lg = 46nm | Lg > 140nm

C.-H. Jan, IEDM'09, P. VanDerVoorn, VLSI Tech'10

Major Roadblocks

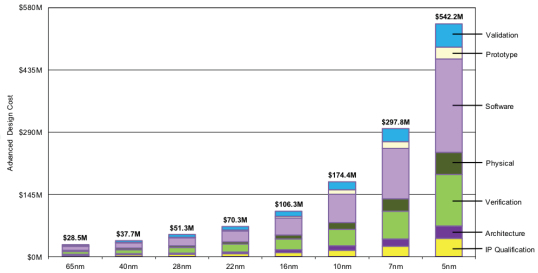
1. Managing complexity
   How to design a 10 billion (100 billion) transistor chip?
   And what to use all these transistors for?
2. Cost of integrated circuits is increasing
   It takes >>$10M to design a chip
   Mask costs are many $M in 16nm technology
3. Power as a limiting factor
   End of frequency scaling
   Dealing with power, leakages
4. Robustness issues
   Variations, SRAM, memory, soft errors, signal integrity
5. The interconnect problem

Power and Performance Trends



- What do we do next?

Cost Of Developing New Products



- These are non-recurring (NRE) costs, need to be amortized over the lifetime of a product
- We will attempt to dismantle this…

Next Lecture

- Impact of technology scaling (and its end)
- Characteristics of current technologies