

EE241B : Advanced Digital Circuits

Lecture 11 – Flip-Flops

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February 25, 2020, NY Times: Should robots have a face?

As automation comes to retail industries, companies are giving machines more humanlike features in order to make them liked, not feared.



Announcements

- Response to project abstracts sent
 - Please let me know if you didn't receive it
 - Team web pages
 - Be careful not to leak proprietary info (interface tools via Hammer)
- Assignment 2 posted

Outline

- Module 3
 - Design of latches and flip-flops

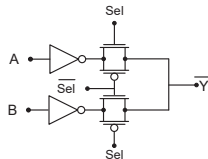
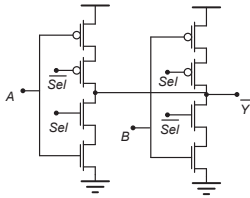
3. Design for Performance

3.D Latch Design

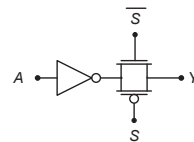


MUX

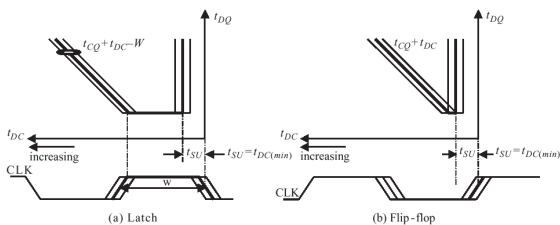
- 2-input MUX



Transmission Gates

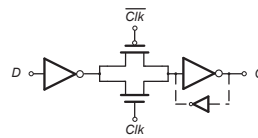


Latch vs. Flip-Flop



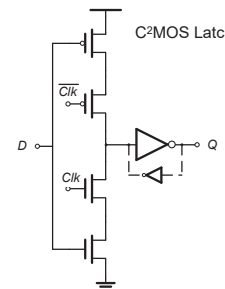
Latches

Transmission-Gate Latch

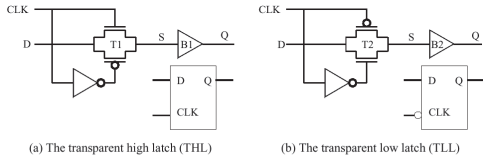


Usually without contention

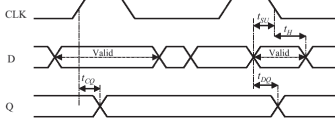
C²MOS Latch



Latches



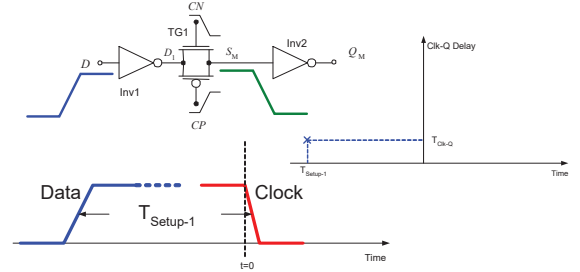
(a) The transparent high latch (THL) (b) The transparent low latch (TLL)



(c) Timing waveforms for the THL
Courtesy of IEEE Press, New York. © 2000

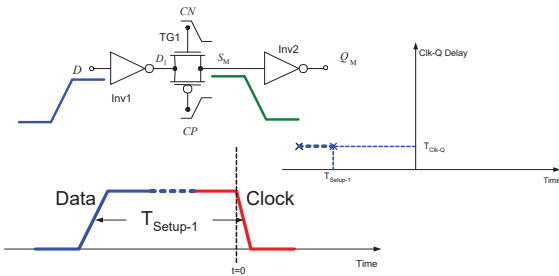
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



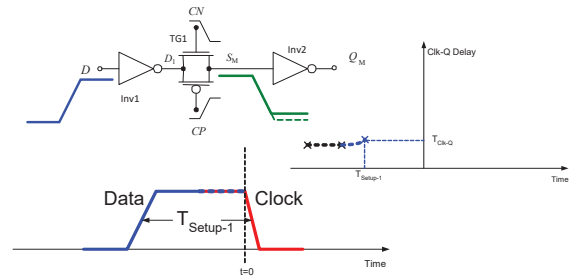
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



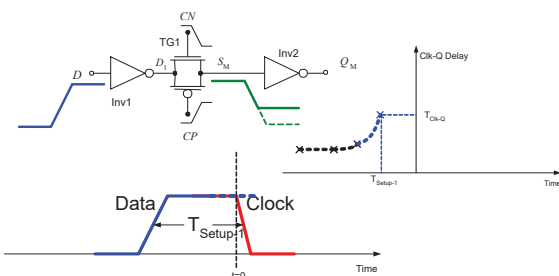
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



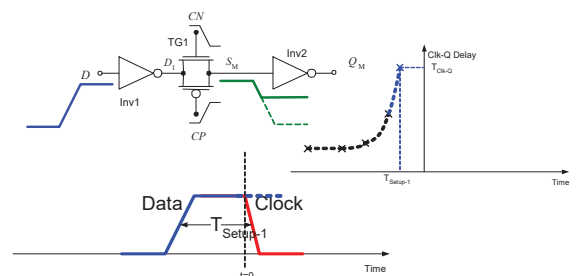
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



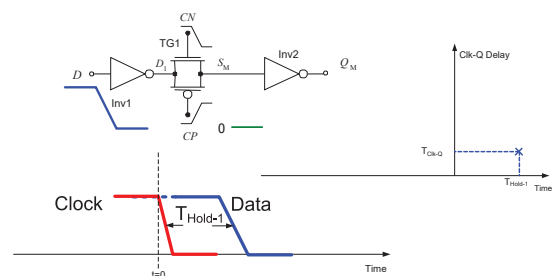
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



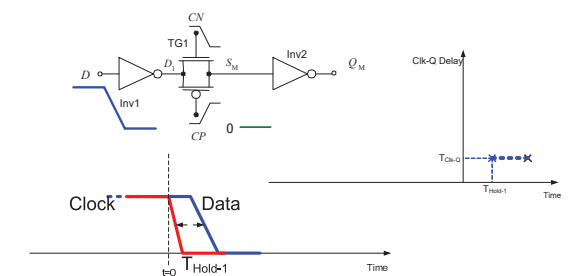
Setup-Hold Time Illustrations

Hold-1 case

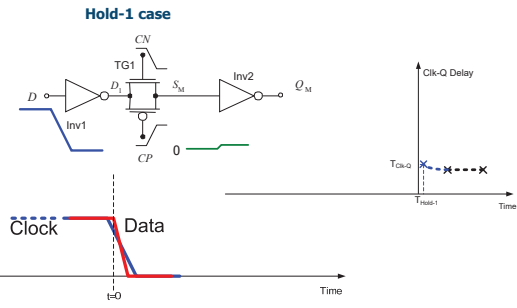


Setup-Hold Time Illustrations

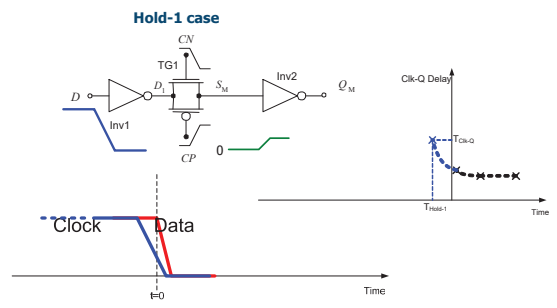
Hold-1 case



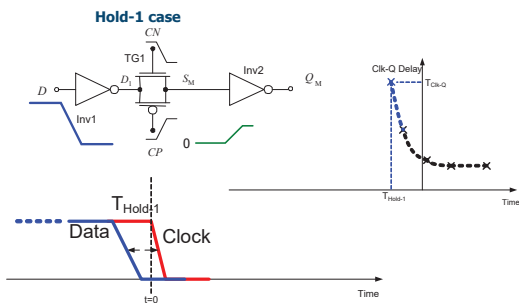
Setup-Hold Time Illustrations



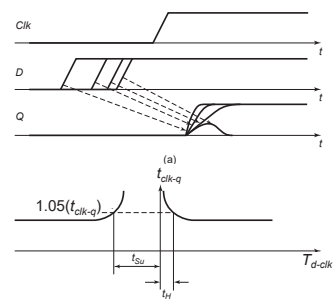
Setup-Hold Time Illustrations



Setup-Hold Time Illustrations



More Precise Setup Time



Generating Complementary Clocks

Latch t_{D-Q} and $t_{\text{Clk-Q}}$

t_{setup}

Key Point

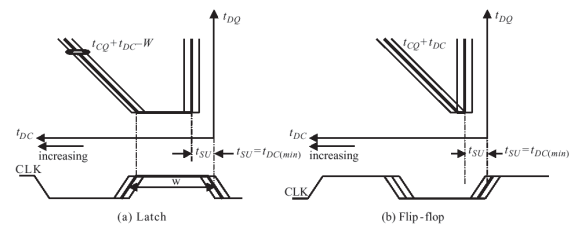
- Two ways to design a flip-flop
 - Latch pair
 - Pulsed latch



3. Design for Performance

3.E Flip-Flop Design

Latch vs. Flip-Flop



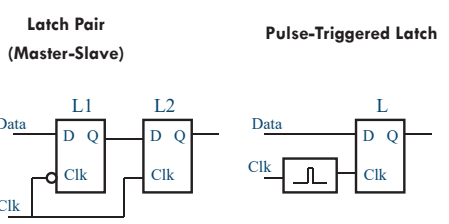
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Flip-Flops

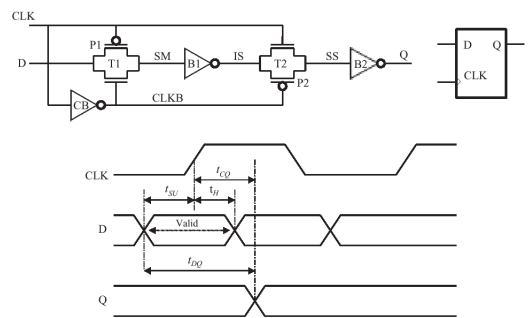
- Performance metrics
- Delay metrics
 - Inherent race immunity
 - 'Softness' (Clock skew absorption)
- Inclusion of logic
- Small (+constant) clock load
- Power/Energy Metrics
 - Power/energy
- Design robustness
 - Noise immunity

Scan Test

Types of Flip-Flops

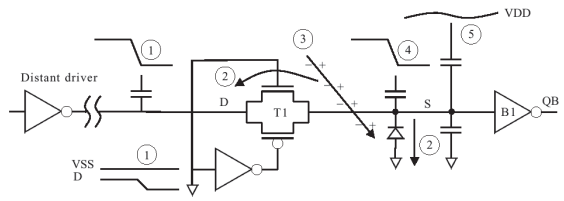


Latch Pair as a Flip-Flop



Sources of Noise

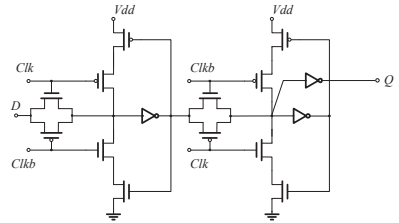
- 1 Noise on input
- 2 Leakage
- 3 α -Particle and cosmic rays
- 4 Unrelated signal coupling
- 5 Power supply ripple



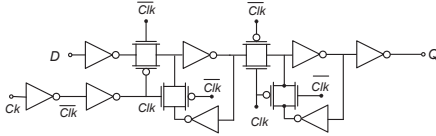
Courtesy of IEEE Press, New York. © 2000

Master-Slave Latch Pairs

- Example: PowerPC 603 (Gerosa, JSSC 12/94)



Flip-Flop Clk-Q, setup, hold



IECS2418 L11 FUP-FLOPS

Pulse-Triggered Latches

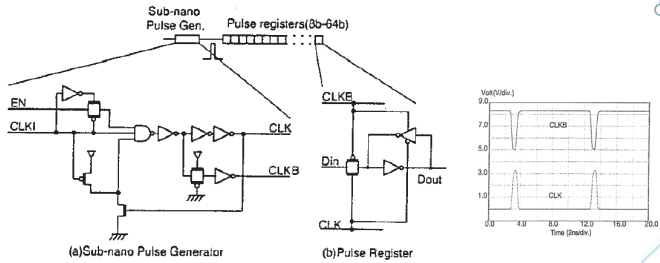
- First stage is a pulse generator
 - generates a pulse (glitch) on a rising edge of the clock
- Second stage is a latch
 - captures the pulse generated in the first stage
- Pulse generation results in a negative setup time
- Frequently exhibit a soft edge property
- Note: power is always consumed in the pulse generator
 - Often shared by a group (register)

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IECS2418 L11 FUP-FLOPS

Pulsed Latch

Simple pulsed latch



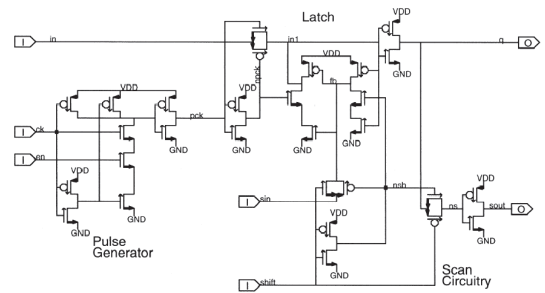
(a) Sub-nano Pulse Generator

(b) Pulse Register

Kozu, ISSCC'96

IECS2418 L11 FUP-FLOPS

Intel/HP Itanium 2



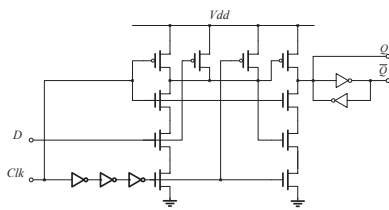
Naffziger, ISSCC'02

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IECS2418 L11 FUP-FLOPS

Pulsed Latches

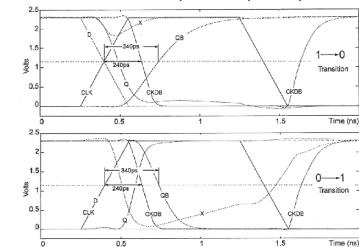
Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC'96



IECS2418 L11 FUP-FLOPS

HLFF Operation

1-0 and 0-1 transitions at the input with 0ps setup time



VDD=2.3V, 85°C, Typical Devices
C_{in}=40fF, C_{sp}=300fF

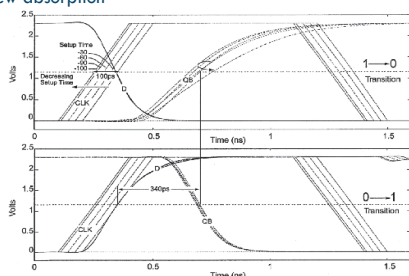
T_{reg}=T_{cl}=340ps
T_{haz}=180ps
T_{setup}=-90ps

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Hybrid Latch Flip-Flop

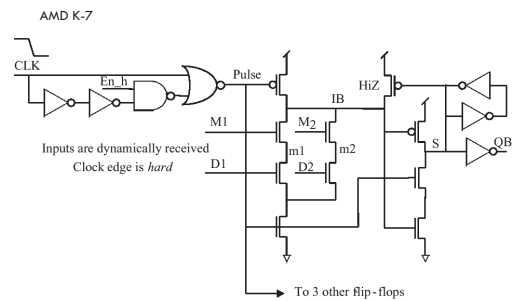
Skew absorption



Partovi et al, ISSCC'96

IECS2418 L11 FUP-FLOPS

Pulsed Latches



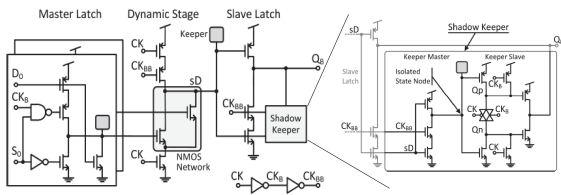
To 3 other flip-flops
Courtesy of IEEE Press, New York. © 2000

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IECS2418 L11 FUP-FLOPS

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Pulsed Latches

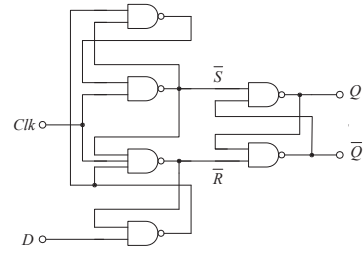


Used in a synthesized flow

Partovi, VLSI'12

Pulsed Latches

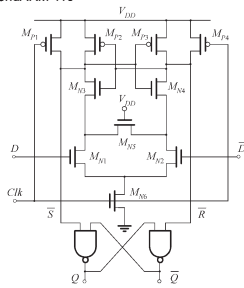
7474, from mid-1960's



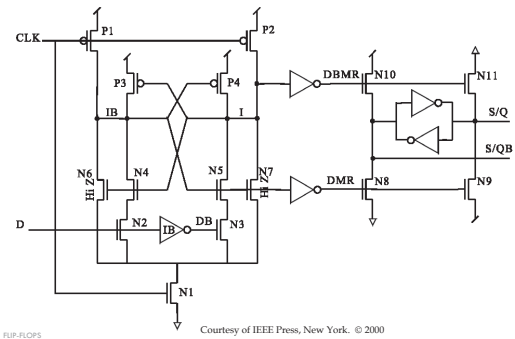
Pulsed Latches

Sense-amplifier-based flip-flop, Matsui 1992.
DEC Alpha 21264, StronoARM 110

First stage is a sense amplifier, precharged to high, when $Clk = 0$
After rising edge of the clock sense amplifier generates the pulse on S or R
The pulse is captured in S-R latch
Cross-coupled NAND has different propagation delays of rising and falling edges

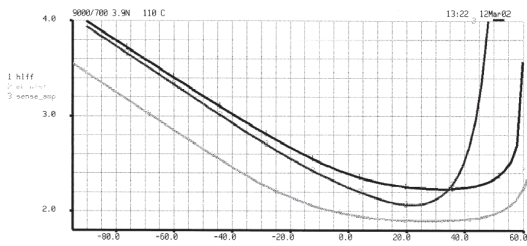


Sense Amplifier-Based Flip-Flop



Courtesy of IEEE Press, New York. © 2000

Sampling Window Comparison



Naffziger, JSSC 11/02

Next Lecture

- Memory