February 25, 2020, NY Times: Should robots have a face?

As automation comes to retail industries, companies are giving machines more humanlike features in order to make them liked, not feared.
Announcements

• Response to project abstracts sent
  • Please let me know if you didn’t receive it
  • Team web pages
    • Be careful not to leak proprietary info (interface tools via Hammer)

• Assignment 2 posted
Outline

• Module 3
  • Design of latches and flip-flops
3. Design for Performance

3. D Latch Design
MUX

• 2-input MUX

\[ g_A = 1.5 \quad g_{\text{Sel}} = 1.5 \]
Transmission Gates

\[ g_{sel} = 7 \]

\[ A \quad | \quad \text{G} \quad | \quad Y \]

\[ S \]

\[ S \]

\[ 2 \frac{1}{3} R \]

\[ 1.5 \]

\[ G_A = 1.5 \]

\[ \frac{R \parallel 2R}{\frac{2}{3} R} \]
Latch vs. Flip-Flop

(a) Latch

(b) Flip-flop

Latches

Transmission-Gate Latch

C\textsuperscript{2}MOS Latch

Usually without contention
Latches

(a) The transparent high latch (THL)  
(b) The transparent low latch (TLL)

(c) Timing waveforms for the THL

Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)

Data \( T_{\text{Setup-1}} \) Clock

\( t=0 \)
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)
Setup-Hold Time Illustrations

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Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)
Setup-Hold Time Illustrations

Hold-1 case

Clock

Data

$T_{Hold-1}$

$t=0$

$T_{Clk-Q}$

$T_{Hold-1}$

Time

Clk-Q Delay

$Q_M$

Inv2

$D_1$

$S_M$

$CN$

TG1

Inv1

$D$

$CP$
Setup-Hold Time Illustrations

Hold-1 case

Clock

Data

T_{Hold-1}

T_{Hold-1}

Inv1

Inv2

D

D

0

CN

TG1

S_M

Q_M

EECS241B L11 FLIP-FLOPS
Setup-Hold Time Illustrations

Hold-1 case

Clock | Data

Clk-Q Delay

T_{Hold-1}

T_{Clk-Q}

D

Inv1

D_1

CN

TG1

SM

Inv2

Q_M

Time

t=0
Setup-Hold Time Illustrations

Hold-1 case

Clock Data

Time

$D$ $D_1$ $S_M$ $Q_M$

Inv1 Inv2

$CN$ $TG1$ $CP$ 0

$T_{Hold-1}$ $T_{Clk-Q}$

Clk-Q Delay

Time

$T=0$
Setup-Hold Time Illustrations

Hold-1 case

Data

Clock

T_{Hold-1}

T_{Hold-1}

Clk-Q Delay

Time

D

Inv1

TG1

D_1

CN

CP

S_M

Inv2

Q_M

EECS241 B L11 FLIP-FLOPS
More Precise Setup Time

\[ t_{D}^{2}C \]

\[ t_{H} \]

\[ t_{Su} \]

1.05\( t_{clk-q} \)

EECS241B L11 FLIP-FLOPS
Generating Complementary Clocks
Latch $t_{D-Q}$ and $t_{Clk-Q}$

\[ GF = 9.8, \quad g_f = 1.5 \]

\[ g_A = \sqrt{GF} = \sqrt{1.5} = 1.2 \]

\[ g_i = 1.5 \]

\[ 0.7 \, RC = 30 \mu s = 5 \, t_{\text{unit}} \]

\[ g_i = g_f = 1.2 \]

\[ t_P = (g_f + g_f + g_f + p_1 + p_2) \, t_{\text{unit}} \]

\[ = (1.2 + 1.2 + 1.2 + 1.5 + 1) \, t_{\text{unit}} \]

\[ = 4.9 \, t_{\text{unit}} = 1 \, t_{04} \]
$t_{\text{setup}}$

![Diagram of a flip-flop circuit with voltage and timing labels.]

$V_{\text{DD}}$  

$D$  

$S$  

$CLK$  

$Q$  

$2.7 \text{ V}$  

$2.2 \text{ V}$  

$\Rightarrow 2.45 \text{ V}$  

$\tau_{p, \text{c}^{2} \text{mos}, 0.5 \rightarrow 0.89}$  

$= 2.1 RC = \frac{2.1}{0.7} \tau_{p} = 3.2 2\tau_{v} = 1.3 \text{ FO4}$

$\tau_{DC} = \tau_{\text{c}^{2} \text{mos}, Q} = 1.0 \text{ FO4}$
Key Point

- Two ways to design a flip-flop
  - Latch pair
  - Pulsed latch
3. Design for Performance

3.E Flip-Flop Design
Latch vs. Flip-Flop

(a) Latch

(b) Flip-flop

Flip-Flops

• Performance metrics

• Delay metrics
  • Insertion delay
  • Inherent race immunity
  • ‘Softness’ (Clock skew absorption)
  • Inclusion of logic
  • Small (+constant) clock load

\[
t_{SU} + t_{ck-q} + t_{ck-q} - t_r
\]

• Power/Energy Metrics
  • Power/energy

• Design robustness
  • Noise immunity
Scan Test