EE241B : Advanced Digital Circuits

Lecture 11 – Flip-Flops

Borivoje Nikolić

February 25, 2020, NY Times: Should robots have a face?

As automation comes to retail industries, companies are giving machines more humanlike features in order to make them liked, not feared.

Announcements

- Response to project abstracts sent
  - Please let me know if you didn't receive it
  - Team web pages
  - Be careful not to leak proprietary info (interface tools via Hammer)
- Assignment 2 posted

Outline

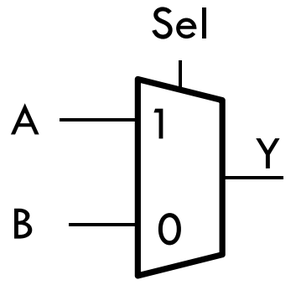
- Module 3
  - Design of latches and flip-flops

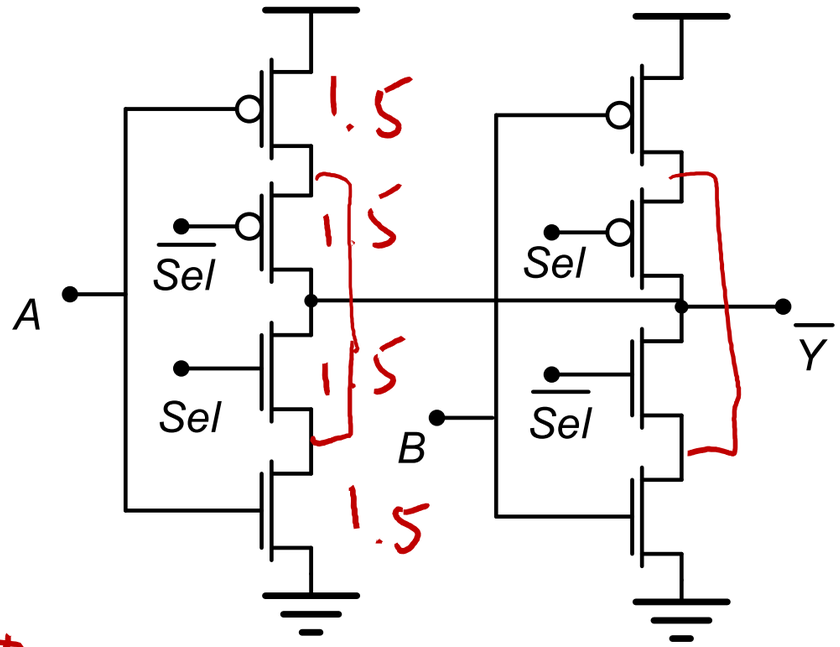
3. Design for Performance

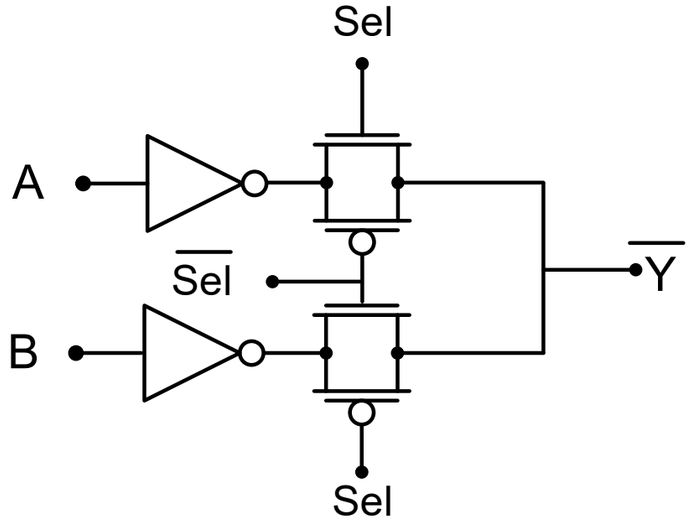
3.D Latch Design

MUX

- 2-input MUX



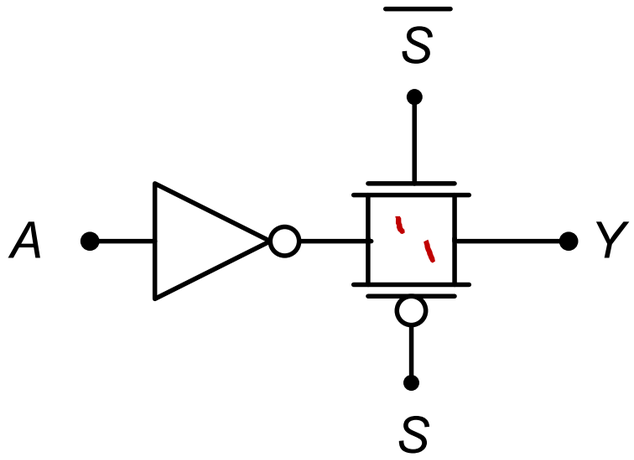


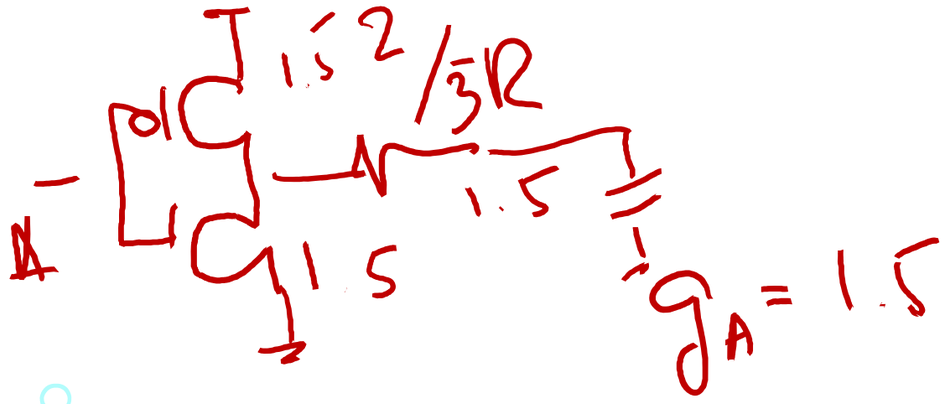


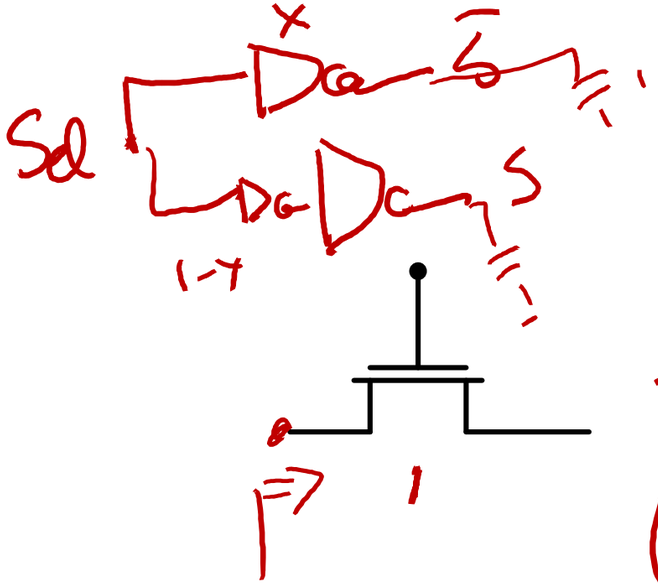
$g_A = 1.5$

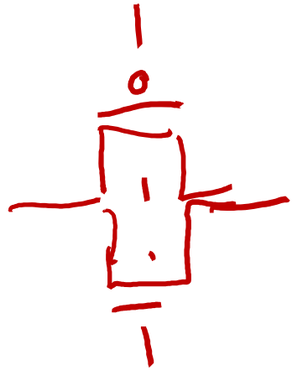
$g_{Sel} = 1.5$

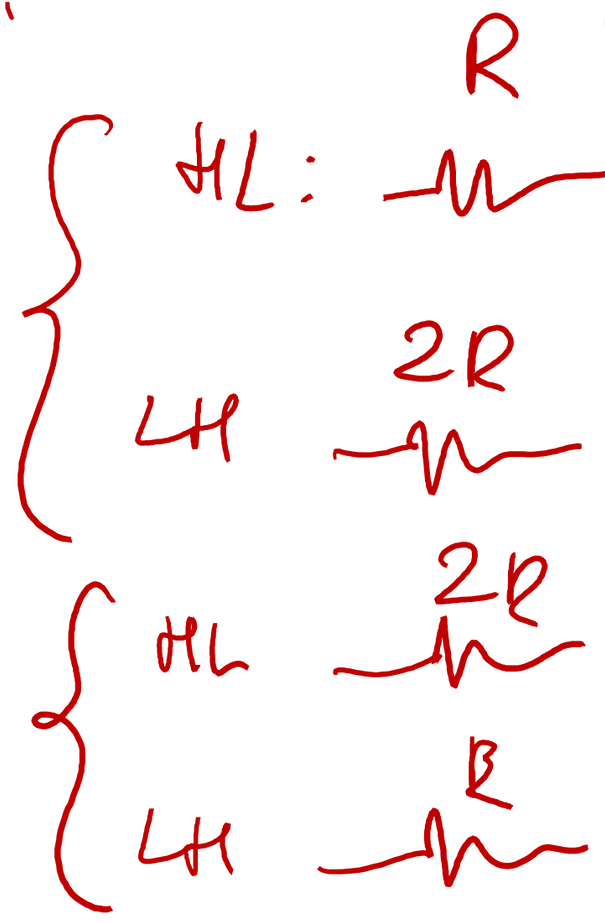
Transmission Gates



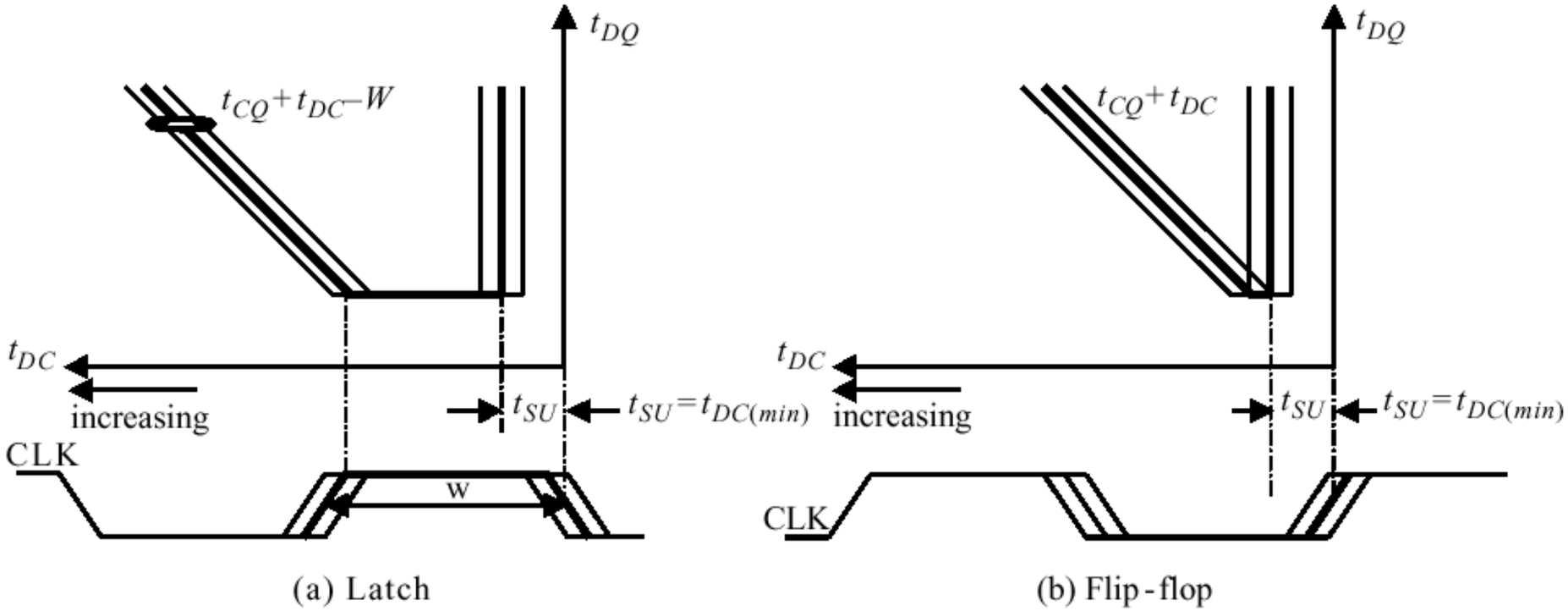






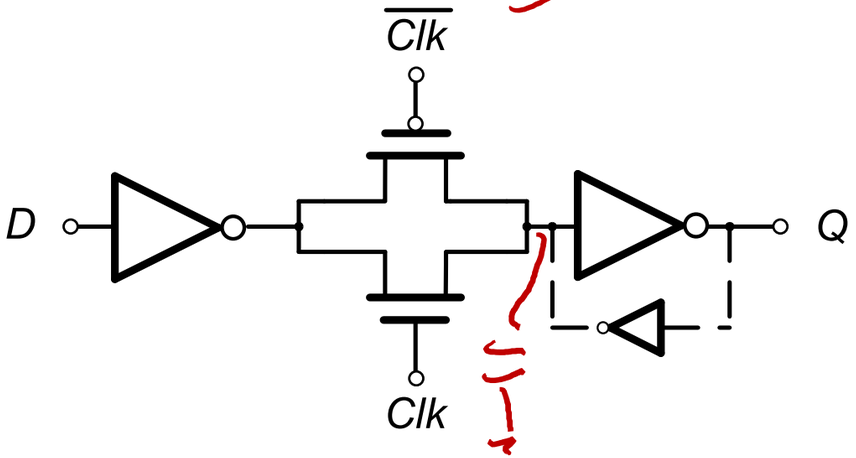


Latch vs. Flip-Flop

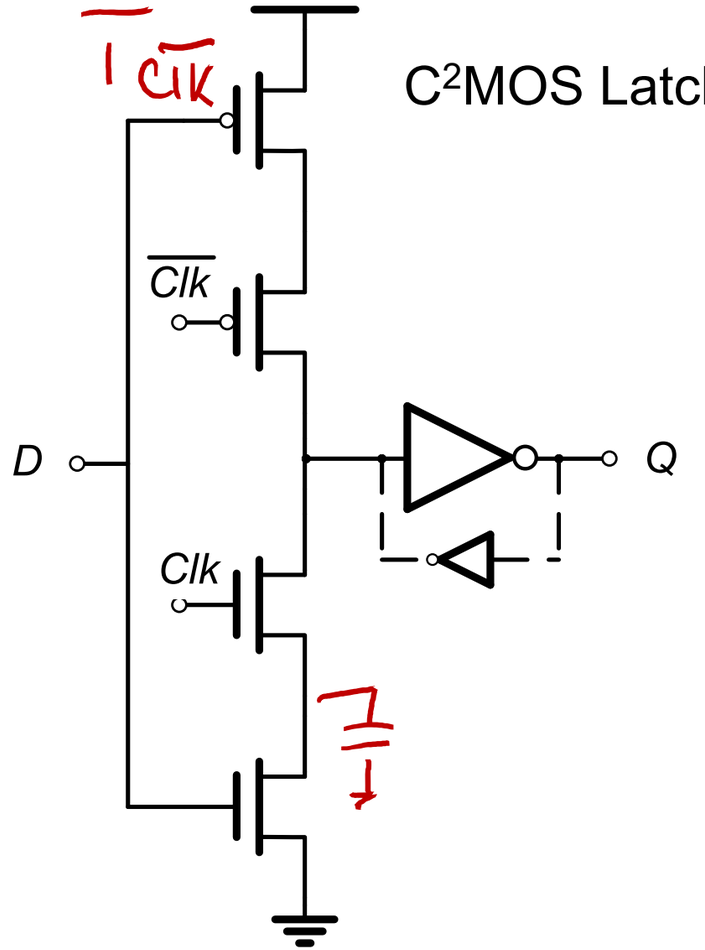


Latches

Transmission-Gate Latch

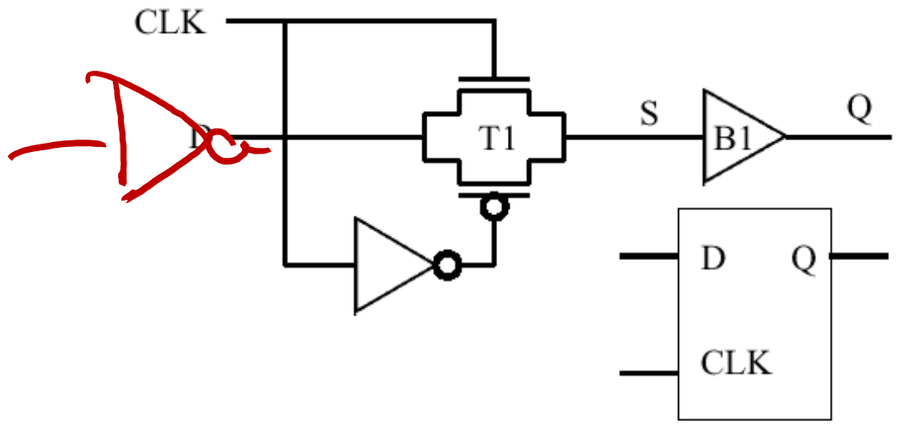


C²MOS Latch

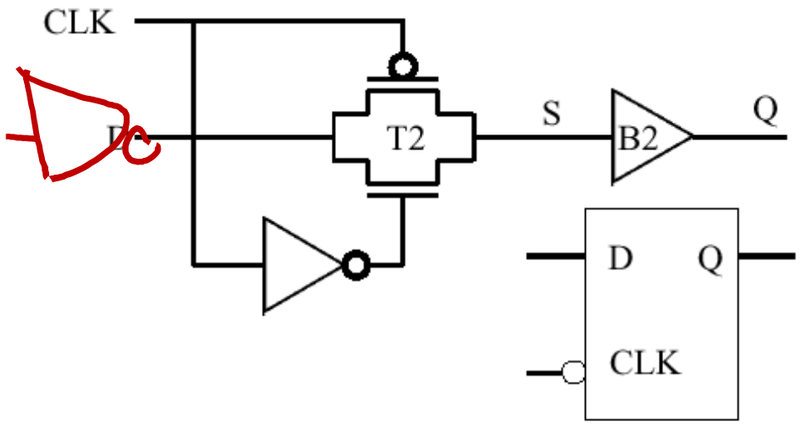


Usually without contention

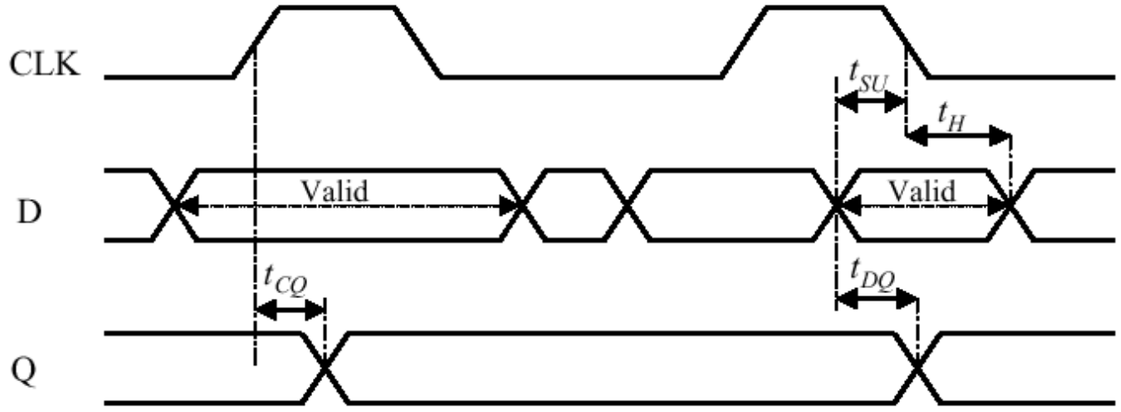
Latches



(a) The transparent high latch (THL)

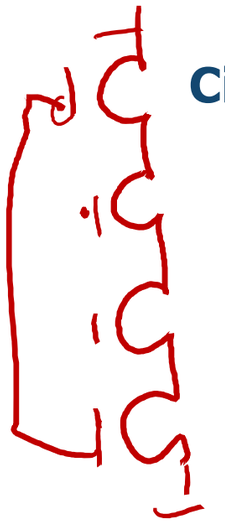


(b) The transparent low latch (TLL)

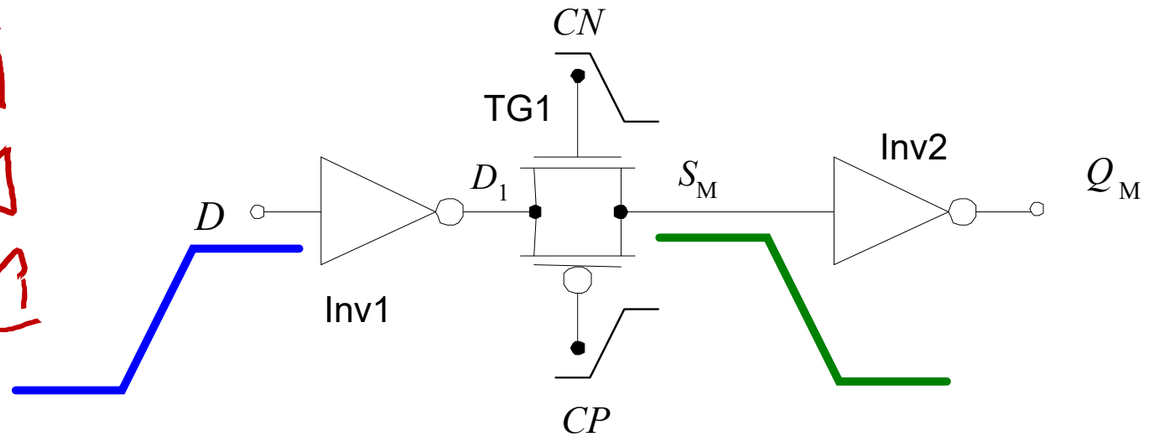


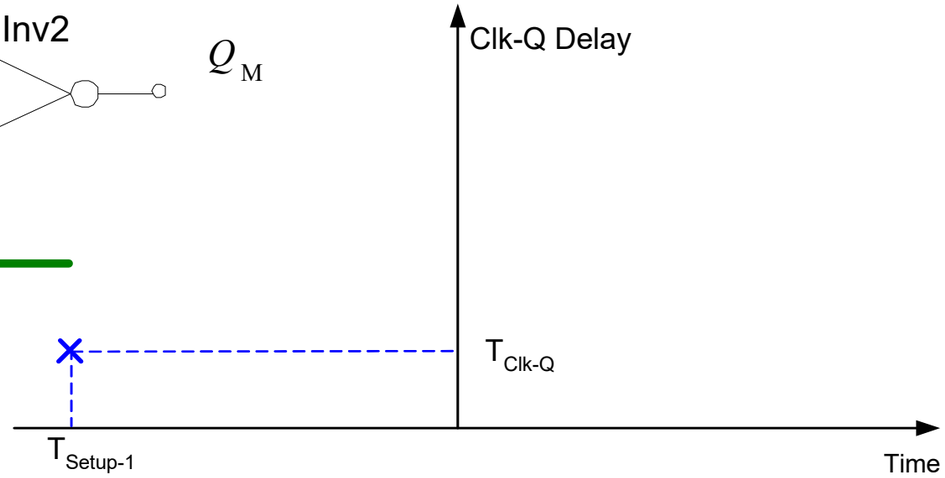
(c) Timing waveforms for the THL

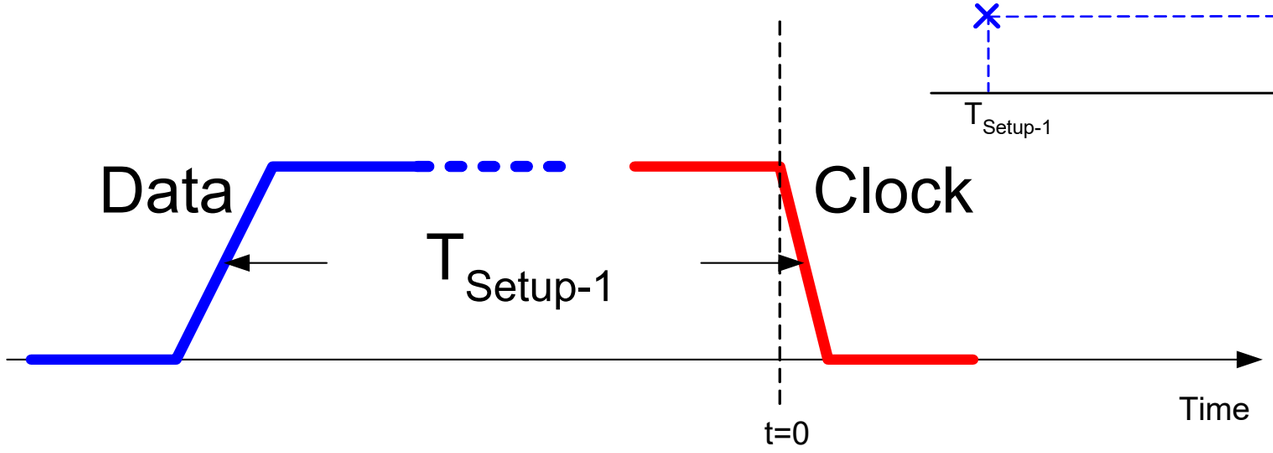
Setup-Hold Time Illustrations



Circuit before clock arrival (Setup-1 case)







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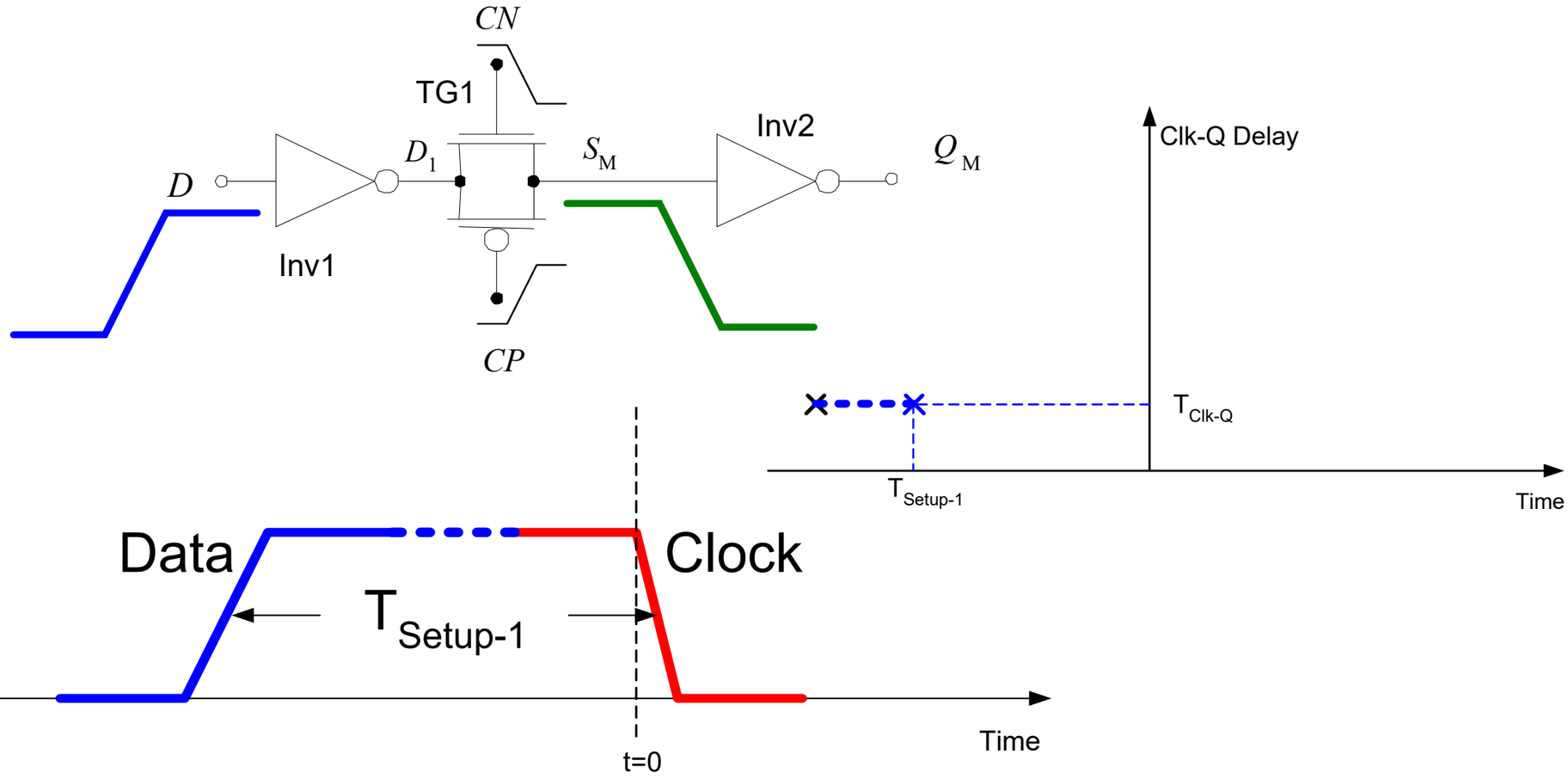

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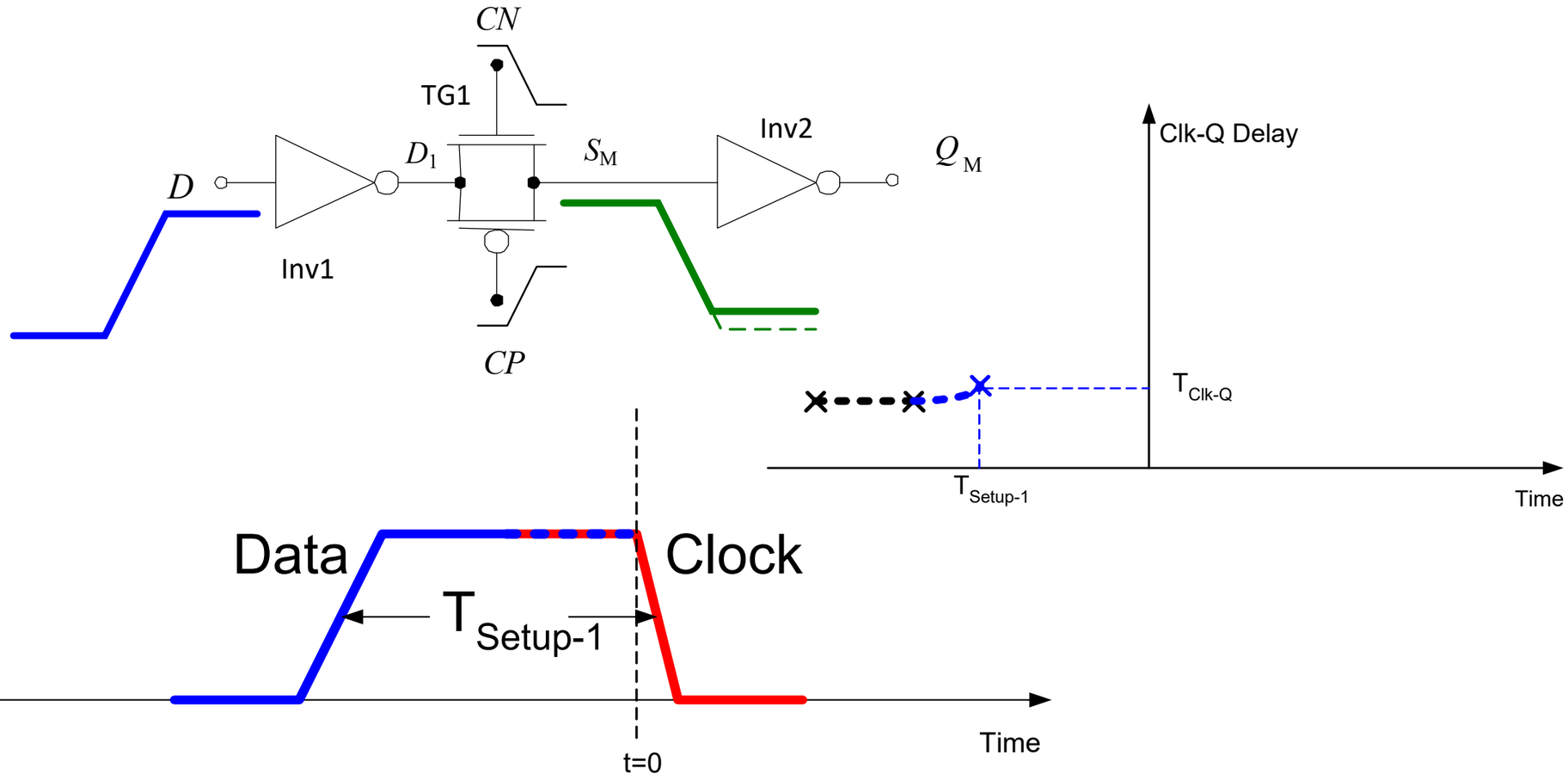

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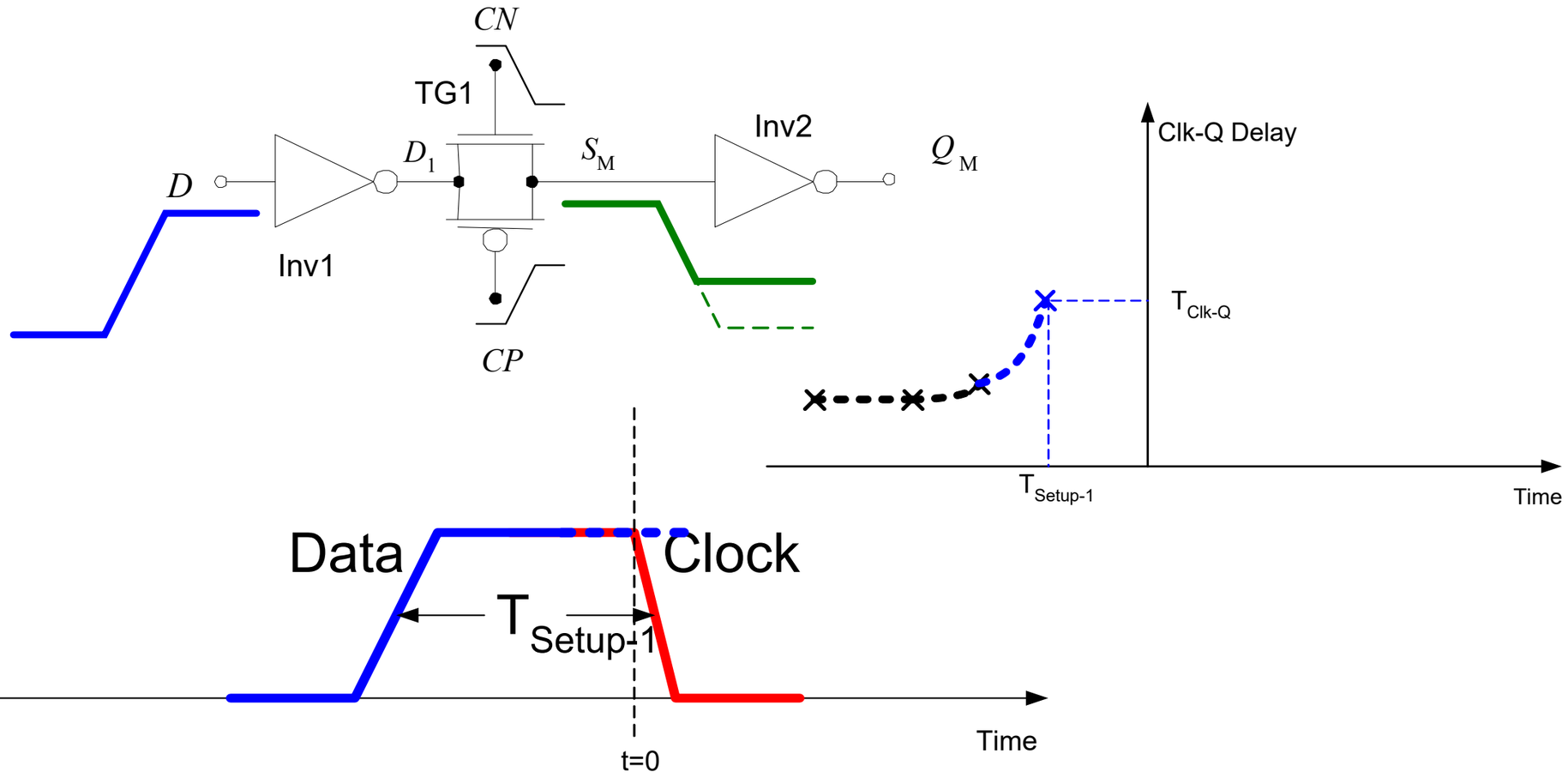

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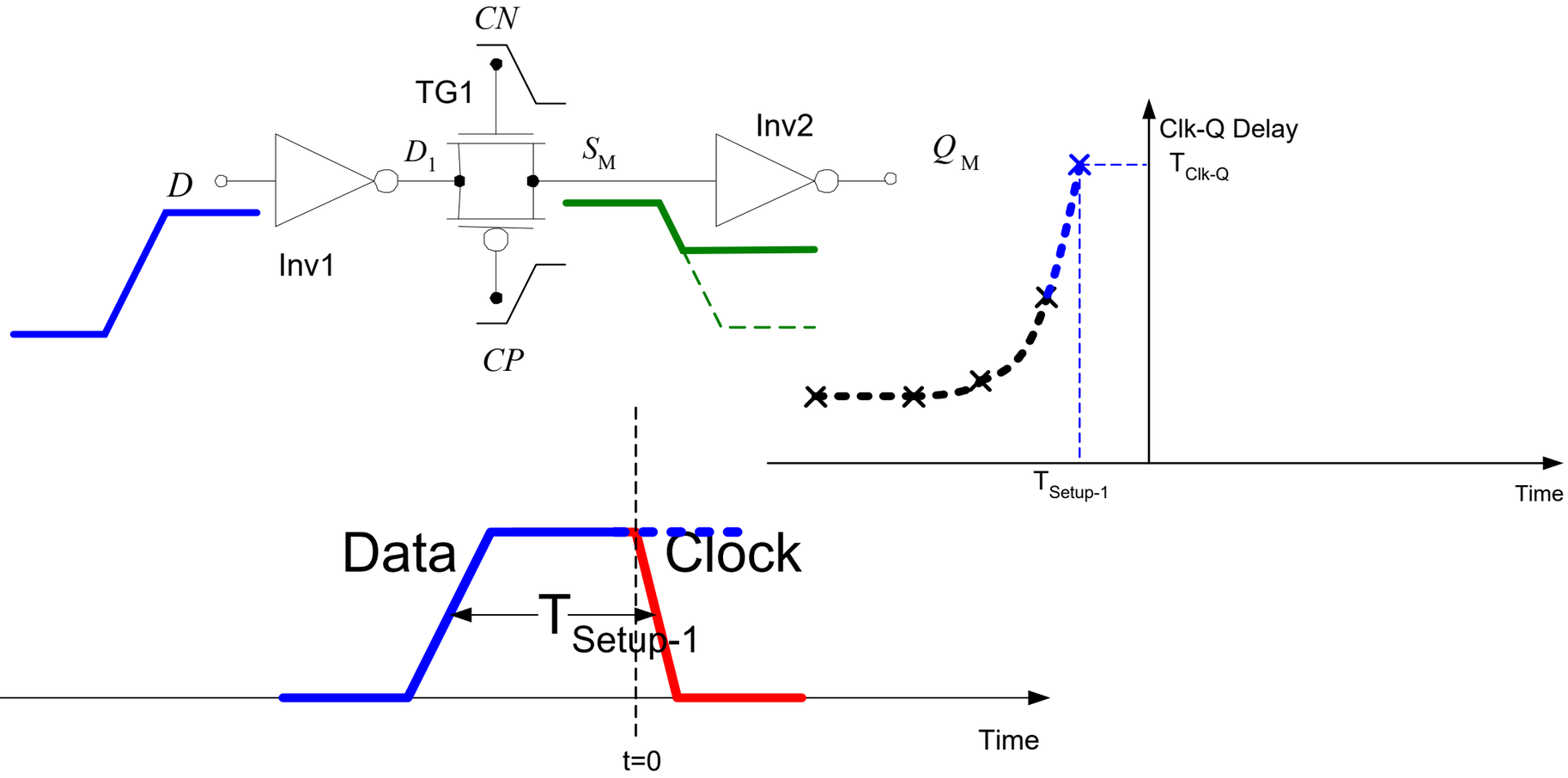
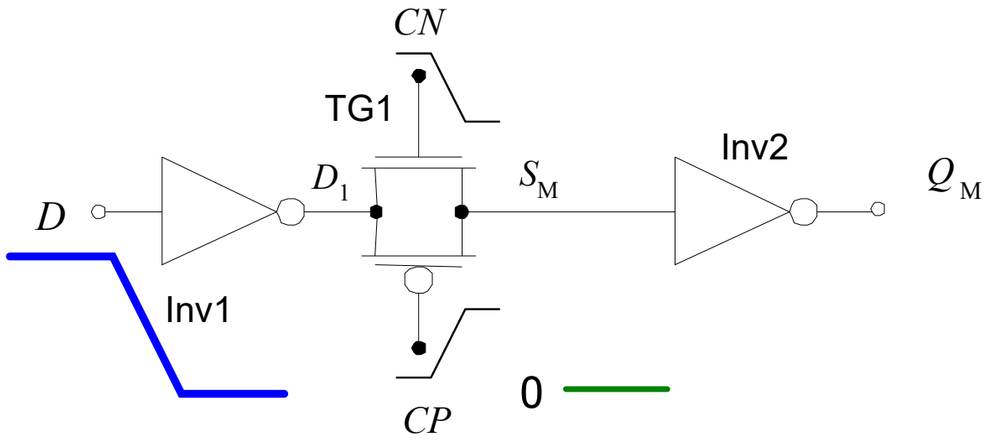
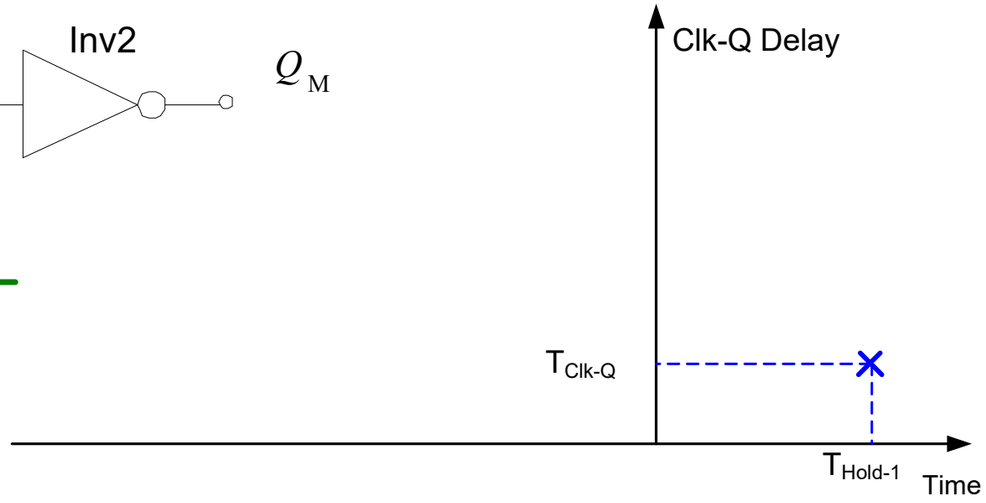
Circuit before clock arrival (Setup-1 case)

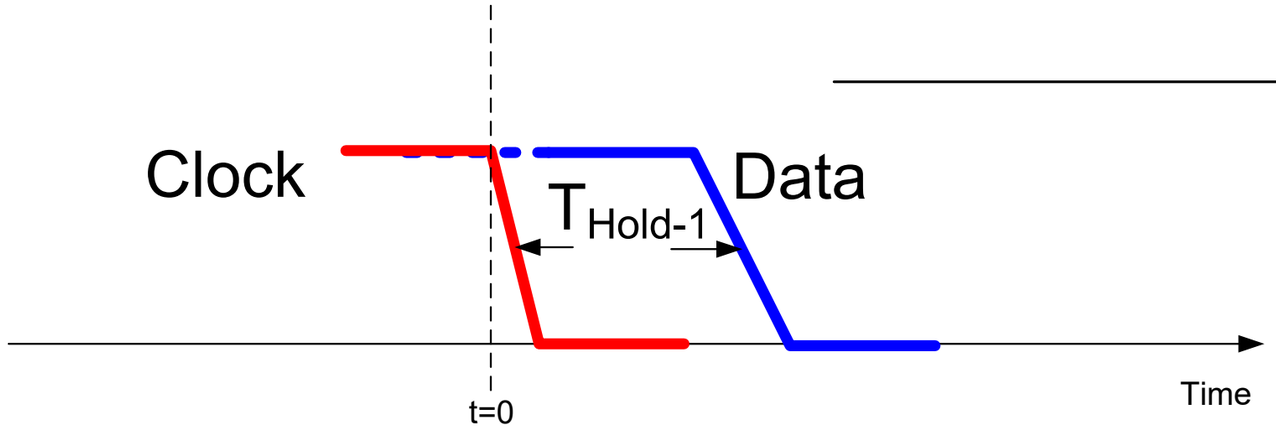


Setup-Hold Time Illustrations

Hold-1 case

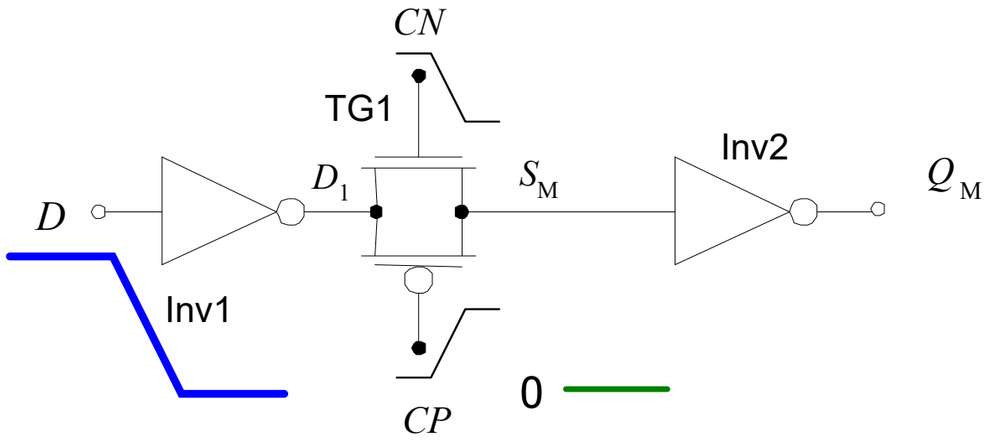


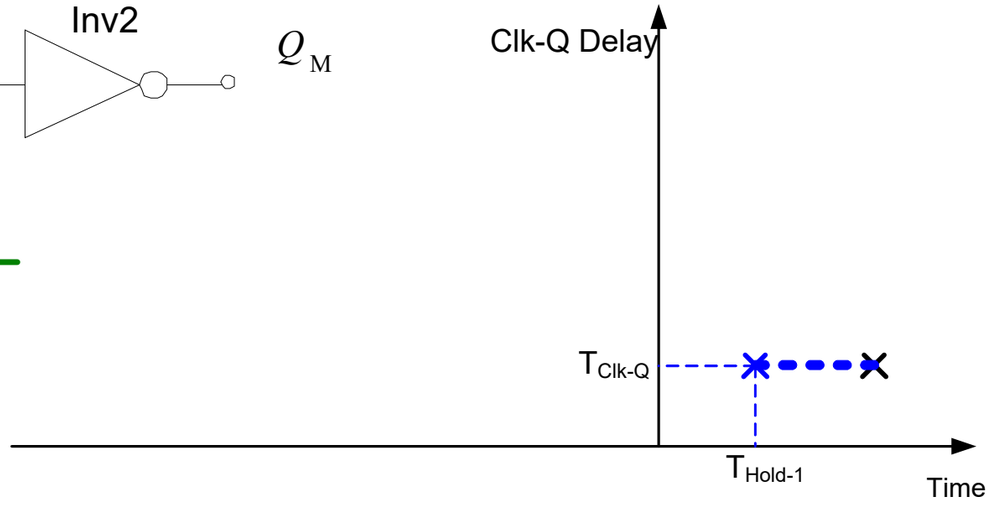


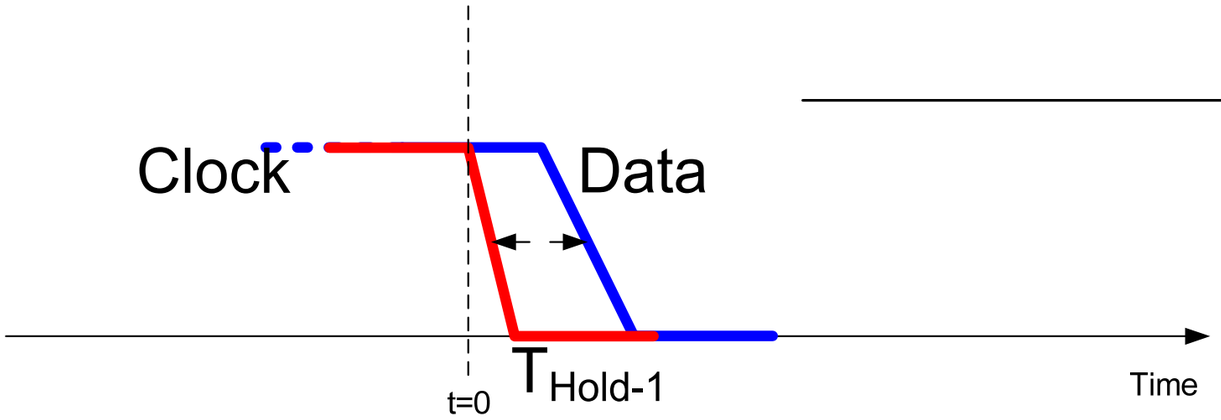


Setup-Hold Time Illustrations

Hold-1 case







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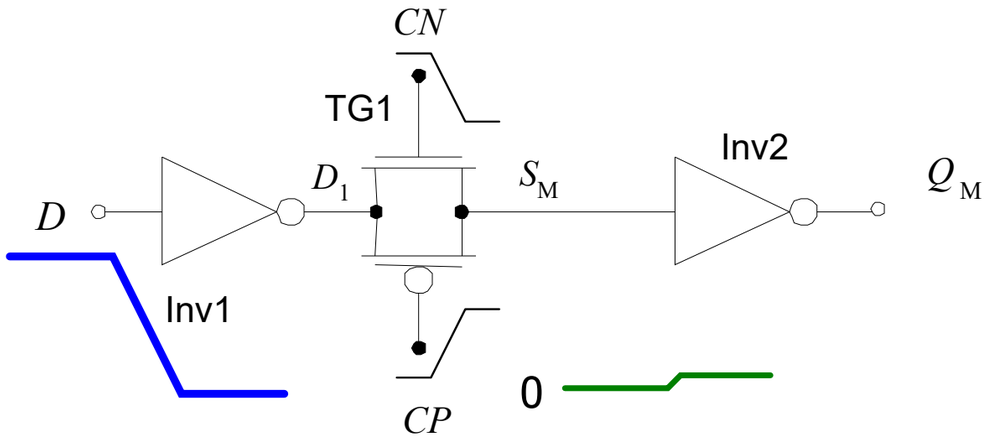
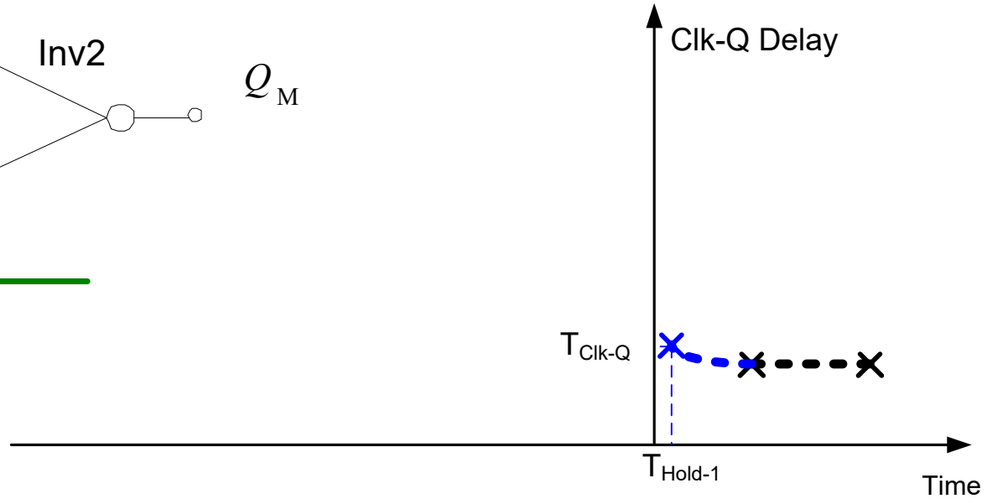
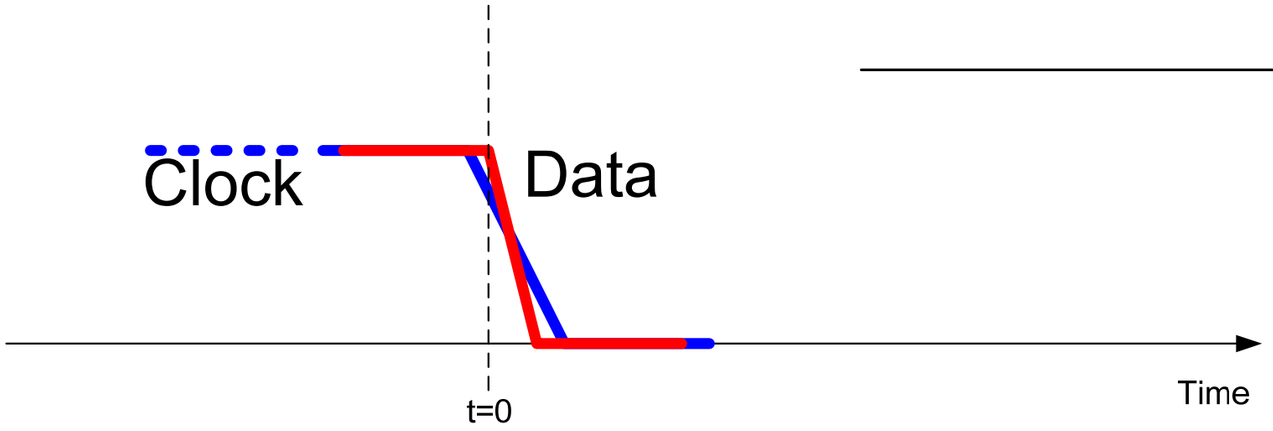
Hold-1 case







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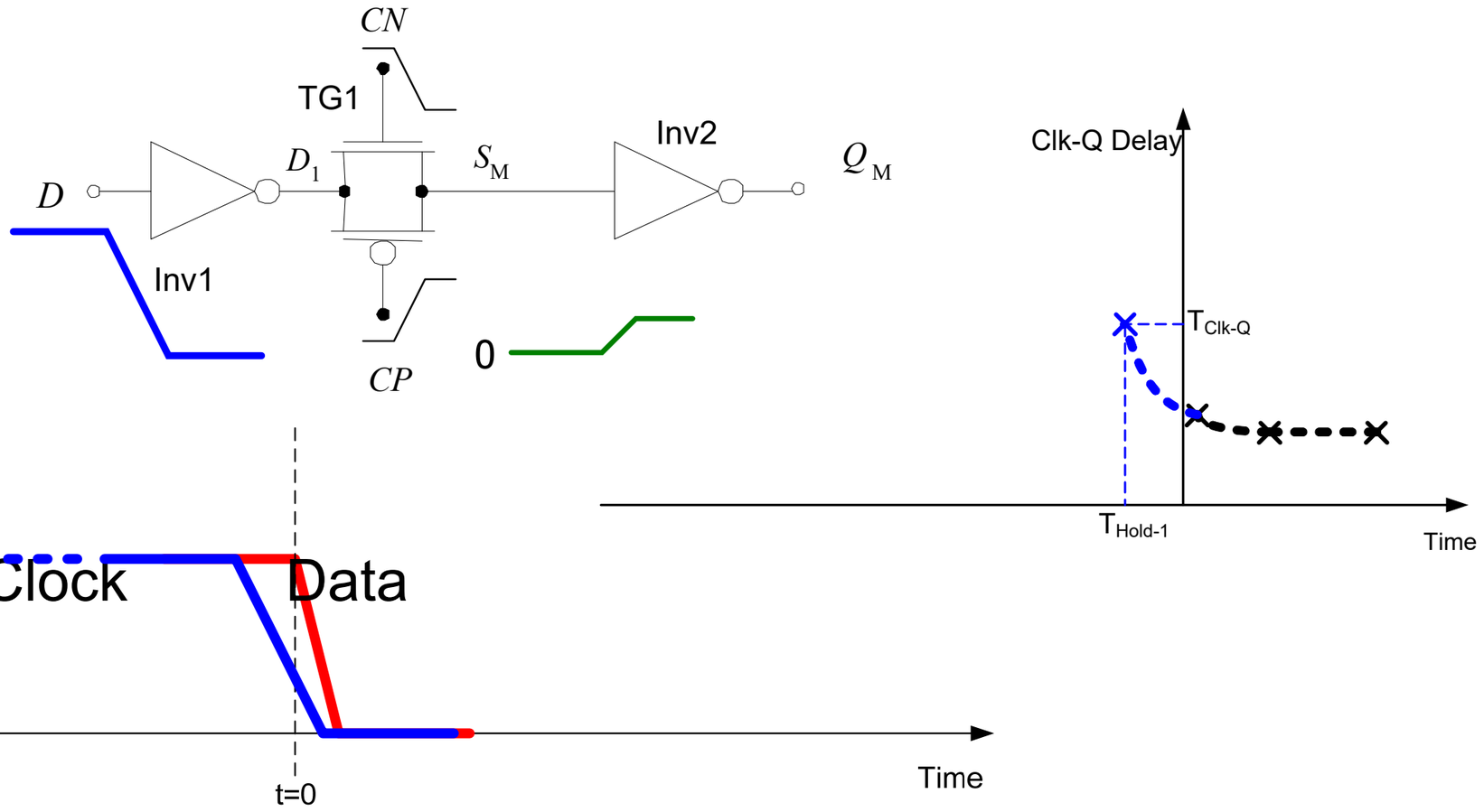

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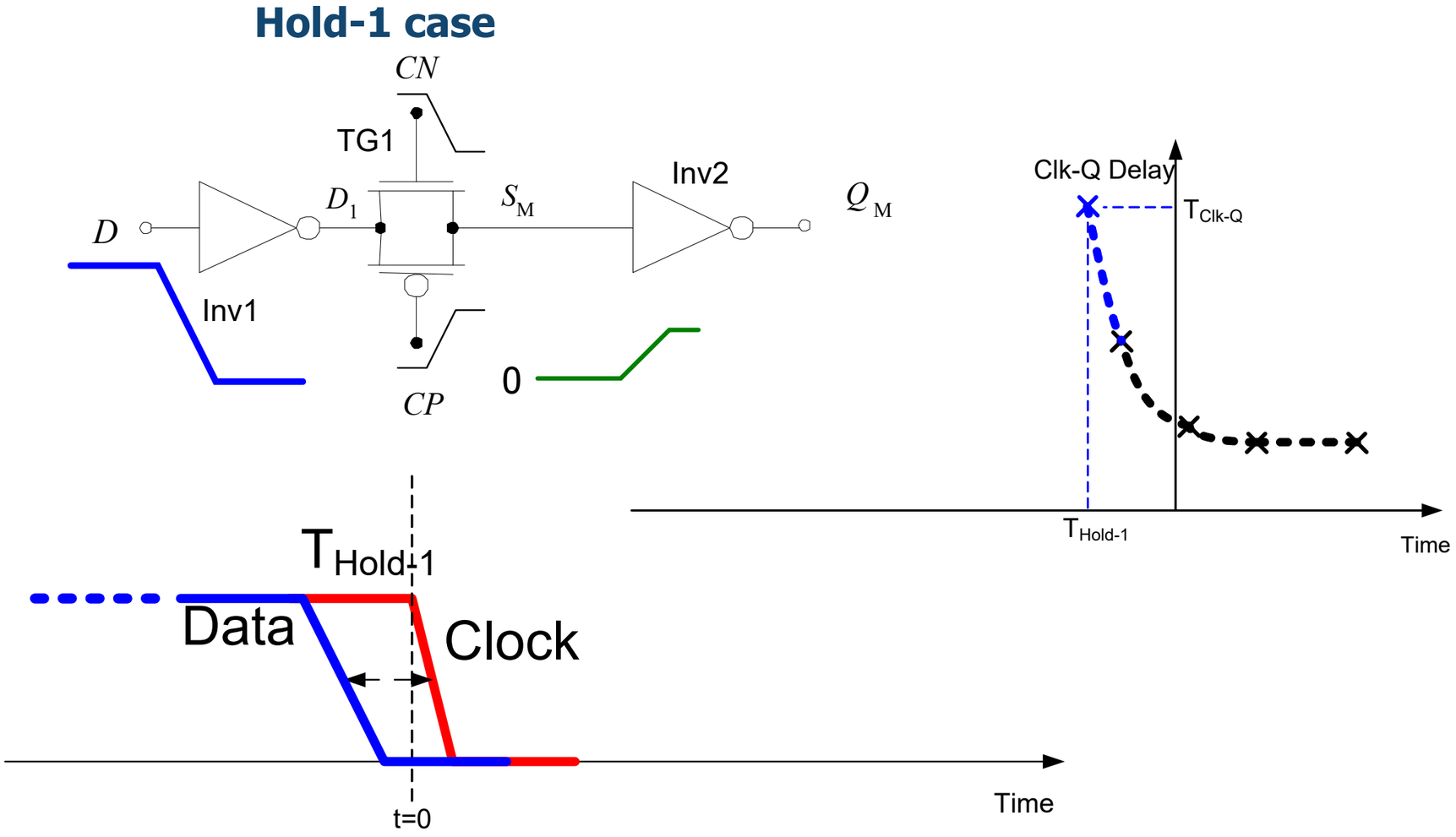
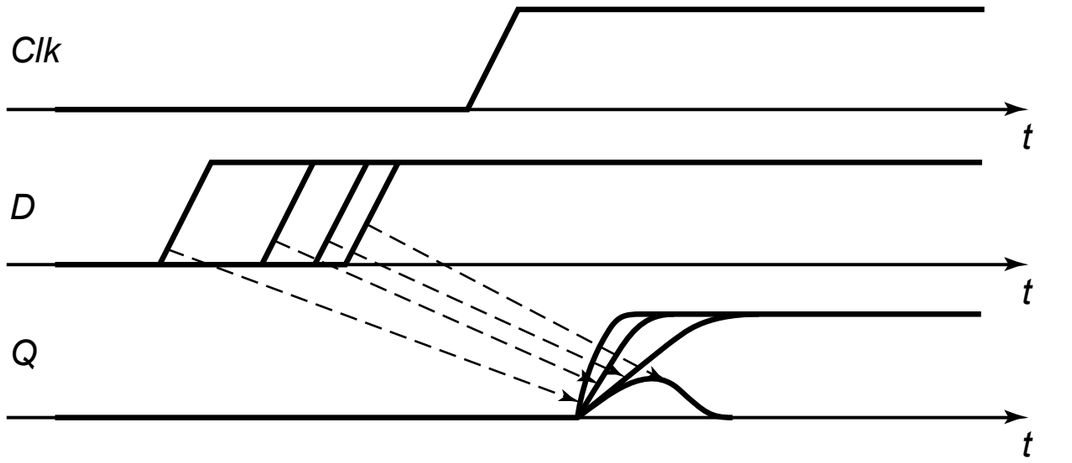
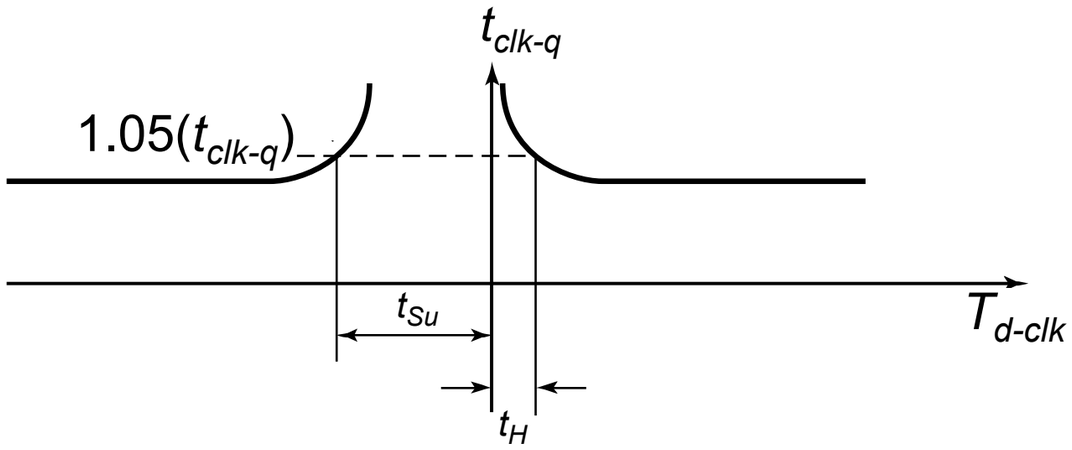


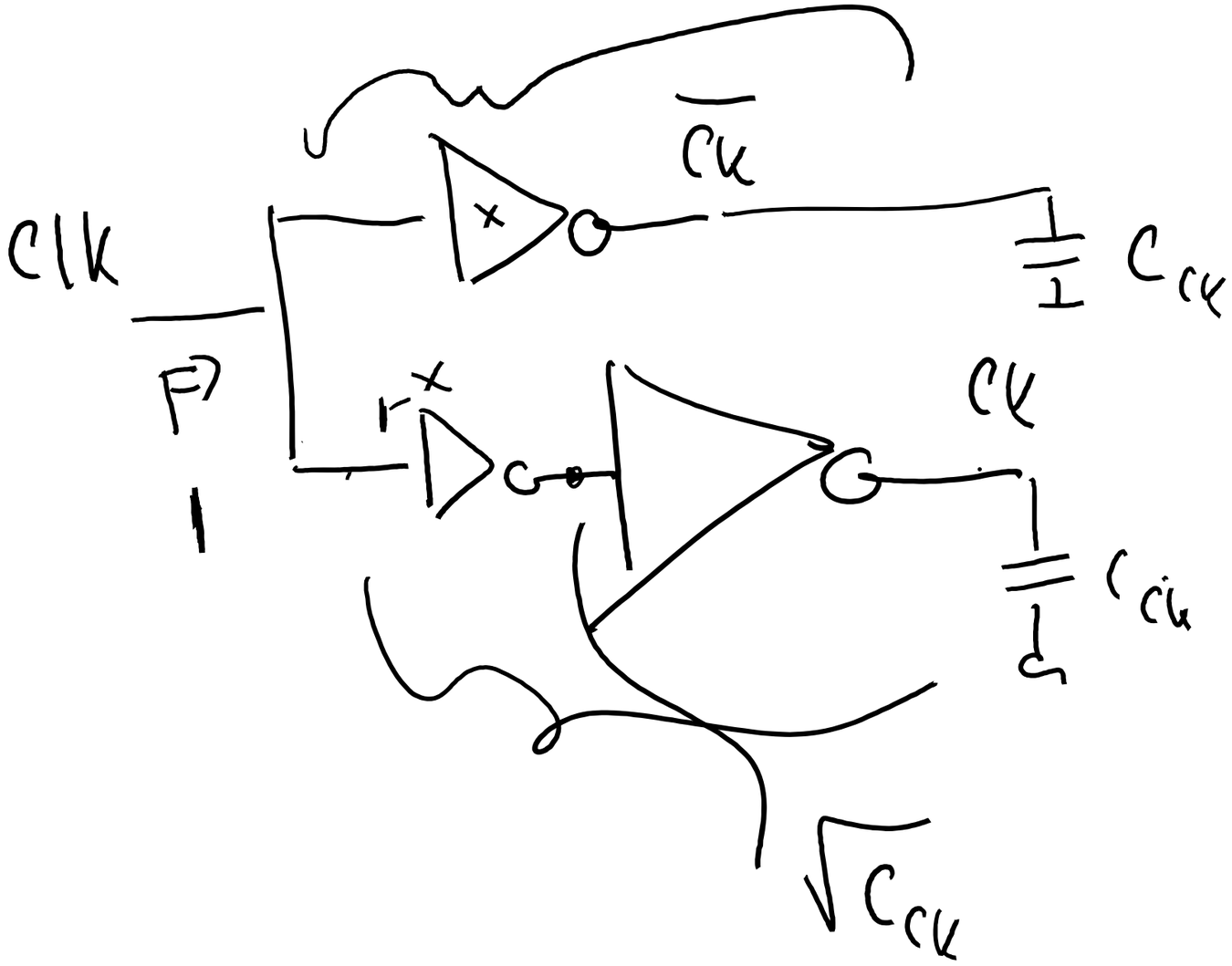
More Precise Setup Time



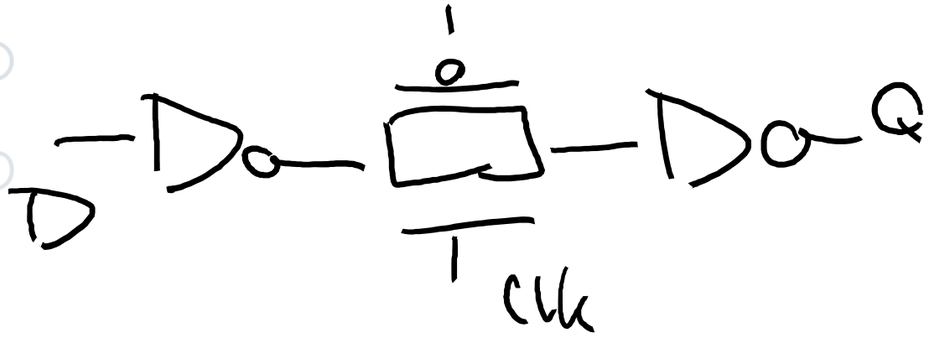
(a)



Generating Complementary Clocks

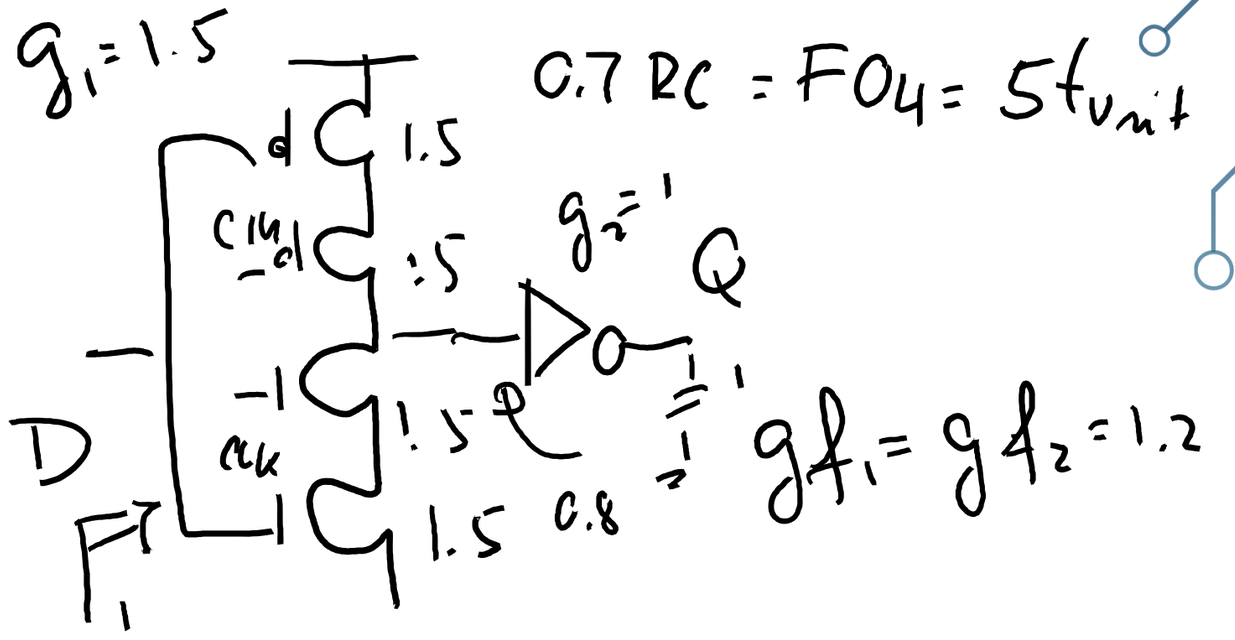


Latch t_{D-Q} and t_{Clk-Q}



$$GF = g_1 f_1 \cdot g_2 f_2 = 1.5$$

$$gf = \sqrt{GF} = \sqrt{1.5} = 1.2$$

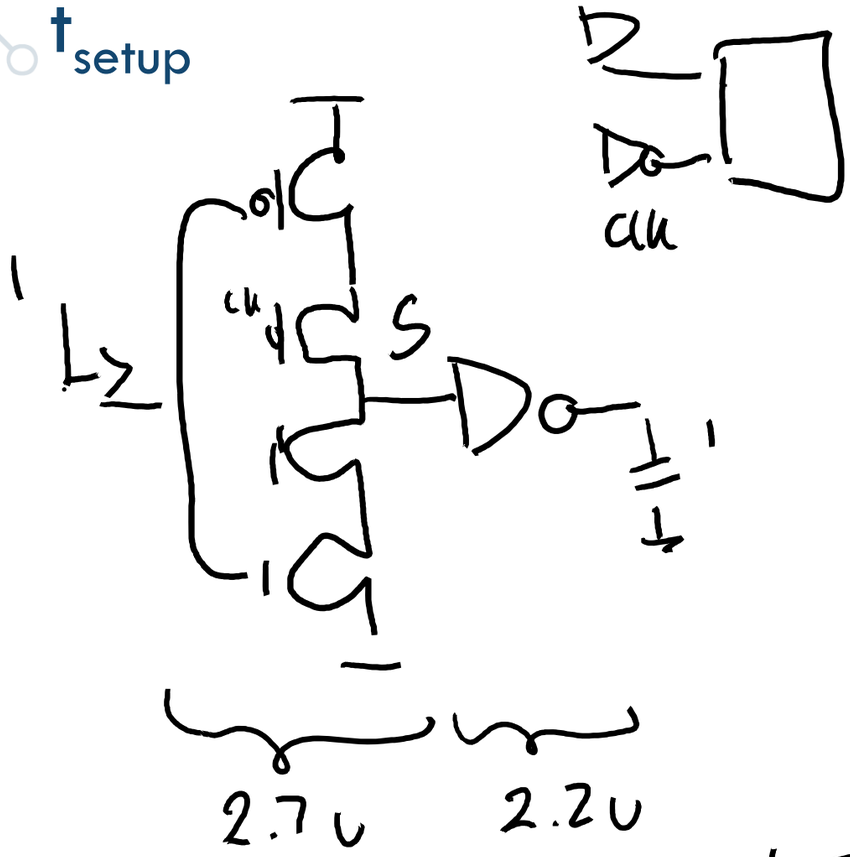


$$t_p = (g_1 f_1 + g_2 f_2 + p_1 + p_2)\, t_{unit}$$

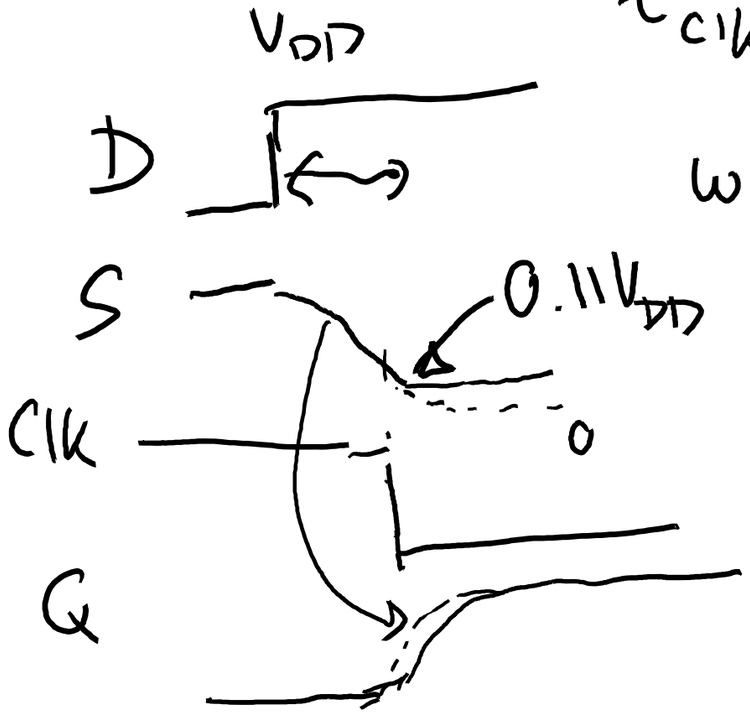
$$= (1.2 + 1.2 + 1.5 + 1)\, t_{unit}$$

$$= 4.9\, t_{unit} = 1\ \text{FO4}$$

t_{setup}



$\hookrightarrow 2.45u$



$t_{clk-Q,nom} = 1$ FO4

what t_{D-Clk} causes

$t_{clk-Q} \Rightarrow 1.05$ FO4

$\frac{1}{1.05 \times 1}$ FO4

$t_{p,c^2MOS,0.5 \to 0.89} = 2.1RC = \frac{2.1}{0.7} t_p = 3 \cdot 2.2 t_u = 1.3$ FO4

$t_{SU} = 1.3$ FO4

$t_{DC} = t_{clk-Q} = 1.0$ FO4

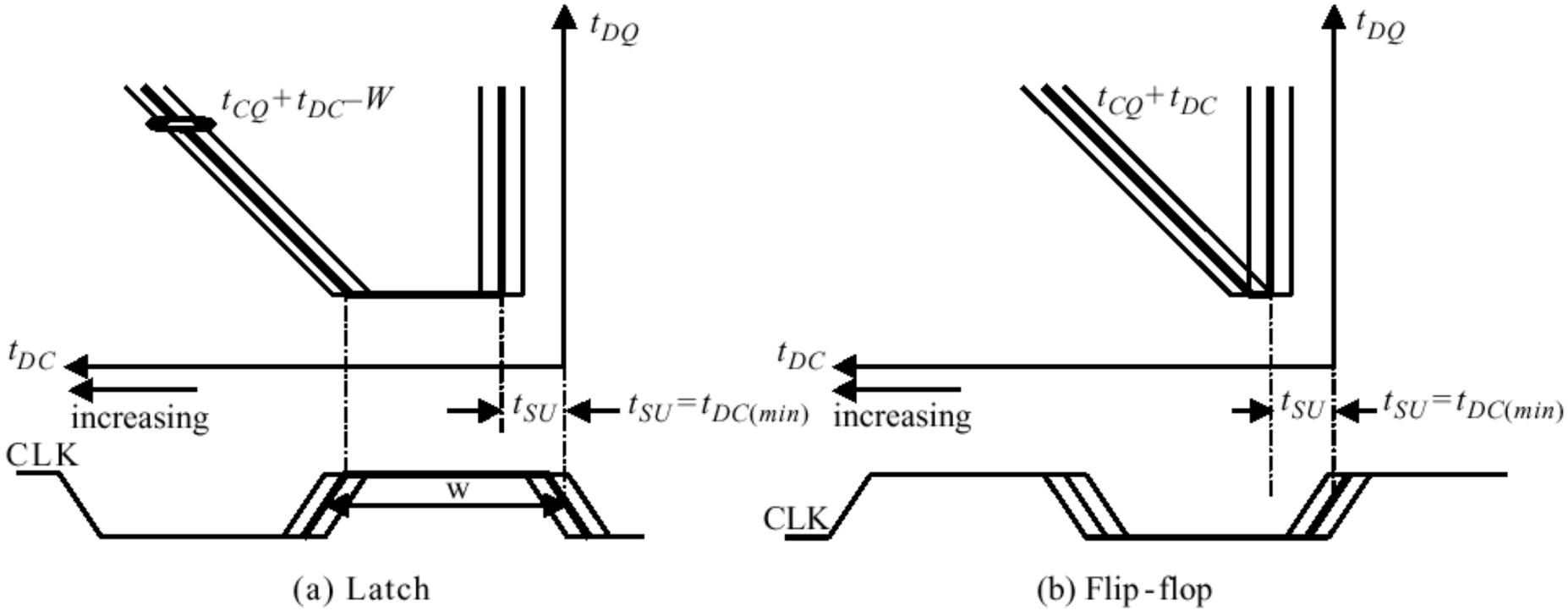
Key Point

- Two ways to design a flip-flop
  - Latch pair
  - Pulsed latch

3. Design for Performance

3.E Flip-Flop Design

Latch vs. Flip-Flop



Flip-Flops

- Performance metrics
- Delay metrics
  - Insertion delay
  - Inherent race immunity
  - 'Softness' (Clock skew absorption)
  - Inclusion of logic
  - Small (+constant) clock load
- Power/Energy Metrics
  - Power/energy
- Design robustness
  - Noise immunity

$t_{su} + t_{ck-q}$

$t_{ck-q} - t_h$

Scan Test