

# EE241B : Advanced Digital Circuits

## Lecture 12 – Flip-Flops, Memory

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March 3, 2020,  
Presidential primary election



### Announcements

- Assignment 2 due on Friday
- Quiz 2 on Tuesday, March 10

### Outline

- Module 3
  - Design of flip-flops
  - SRAM basics

### 3. Design for Performance

#### 3.D Latch Design



### Lecture 11 Errata

- Latch  $t_{D-Q}$  (with  $C_L = C_{in}$ )
  - $t_{D-Q} = 4.9 t_{unit} \sim 1 \text{ FO4}$  (not 1.25 FO4)
  - $t_{su} = 6.6 t_{unit} \sim 1.3 \text{ FO4}$  (not 1.55 FO4)

### 3. Design for Performance

#### 3.E Flip-Flop Design



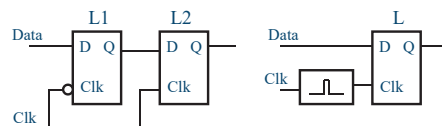
### Key Point

- Two ways to design a flip-flop
  - Latch pair
  - Pulsed latch

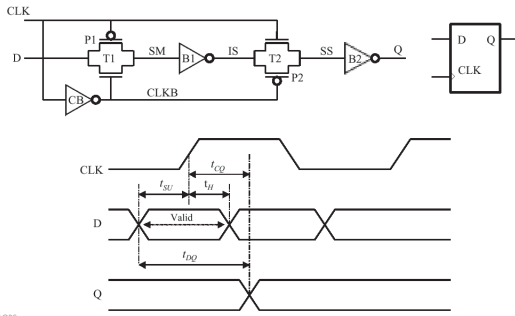
### Types of Flip-Flops

Latch Pair (Master-Slave)

Pulse-Triggered Latch



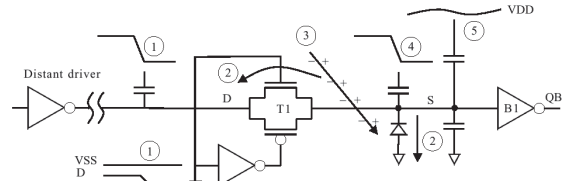
## Latch Pair as a Flip-Flop



HECS2418 L11 FUP-FLOPS

## Sources of Noise

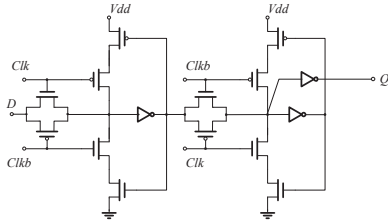
- ① Noise on input
- ② Leakage
- ③  $\alpha$ -Particle and cosmic rays
- ④ Unrelated signal coupling
- ⑤ Power supply ripple



Courtesy of IEEE Press, New York. © 2000

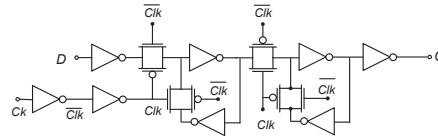
## Master-Slave Latch Pairs

- Example: PowerPC 603 (Gerosa, JSSC 12/94)



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## Flip-Flop Clk-Q, setup, hold



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## Flip-Flop Timing Characterization

- Combinational logic delay is a function of output load and input slope
- Sequential timing (flip-flop):
  - $t_{clk-q}$  is function of output load and clock rise time
  - $t_{su}$ ,  $t_{H}$  are functions of D and Clk rise/fall times

Hikoic, Shuo Fall 2019 © UCS

## Pulse-Triggered Latches

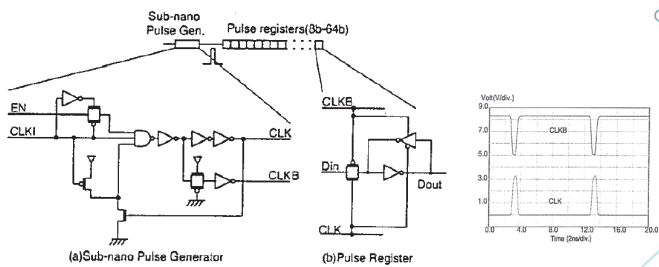
- First stage is a pulse generator
  - generates a pulse (glitch) on a rising edge of the clock
- Second stage is a latch
  - captures the pulse generated in the first stage
- Pulse generation results in a negative setup time
- Frequently exhibit a soft edge property
- Note: power is always consumed in the pulse generator
  - Often shared by a group (register)

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## Pulsed Latch

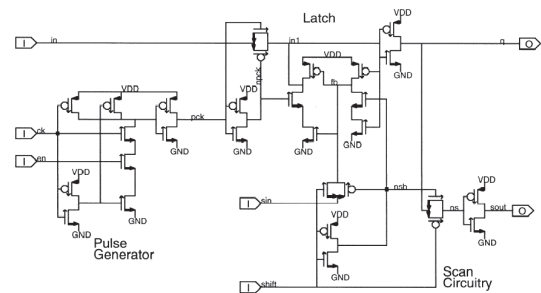
Simple pulsed latch



Kozu, ISSCC'96

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## Intel/HP Itanium 2



Naffziger, ISSCC'02

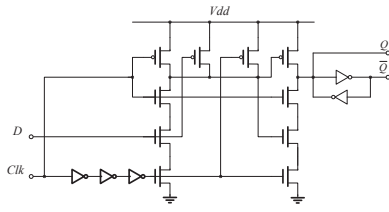
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## Pulsed Latches

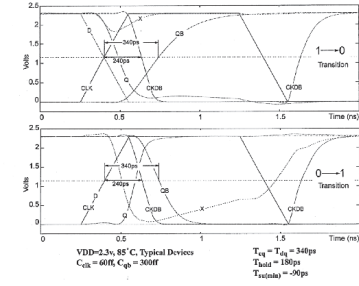
Hybrid Latch Flip-Flop, AMD K-6  
Partovi, ISSCC'96



IEEECS2418.L11.FLP-FLOPS

## HLFF Operation

1-0 and 0-1 transitions at the input with Ops setup time

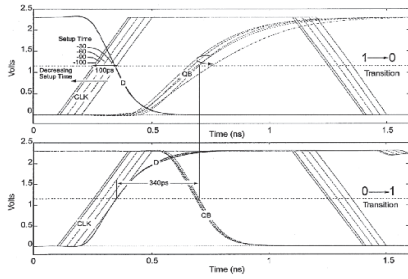


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## Hybrid Latch Flip-Flop

Skew absorption

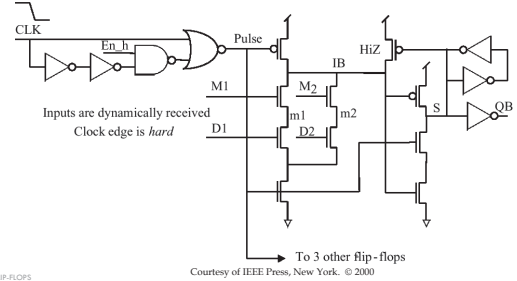


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Partovi et al, ISSCC'96

## Pulsed Latches

AMD K-7

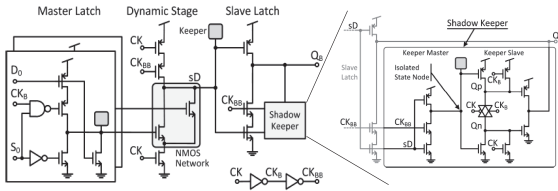


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## Pulsed Latches



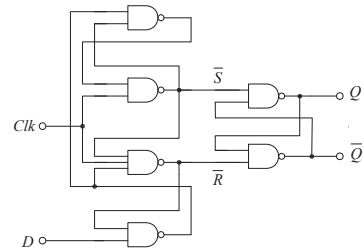
Used in a synthesized flow

Partovi, VLSI'12

IEEECS2418.L11.FLP-FLOPS

## Pulsed Latches

7474, from mid-1960's



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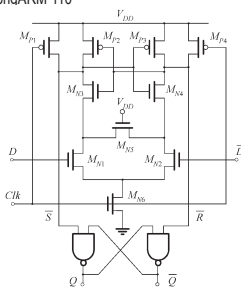
IEEECS2418.L11.FLP-FLOPS

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## Pulsed Latches

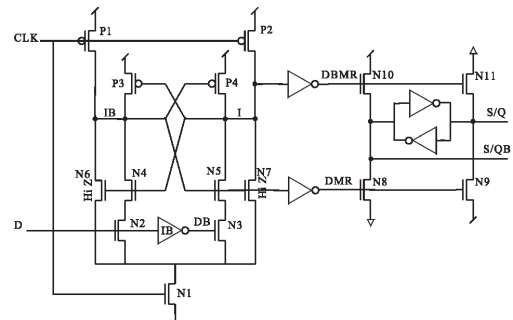
Sense-amplifier-based flip-flop, Matsui 1992.  
DEC Alpha 21264, StrongARM 110

First stage is a sense amplifier, precharged to high, when  $Clk = 0$   
After rising edge of the clock sense amplifier generates the pulse on S or R  
The pulse is captured in S-R latch  
Cross-coupled NAND has different propagation delays of rising and falling edges



IEEECS2418.L11.FLP-FLOPS

## Sense Amplifier-Based Flip-Flop



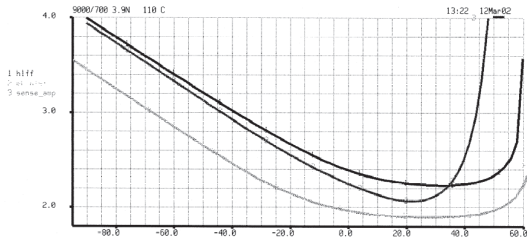
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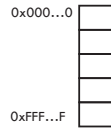
## Sampling Window Comparison



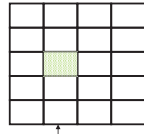
Naffziger, JSSC 11/02

## Random Access Memory Architecture

- Conceptual: Linear array of addresses
  - Each box holds some data
  - Not practical to physically realize
    - millions of 32b/64b words



- Create a 2-D array
  - Decode Row and Column address to get data

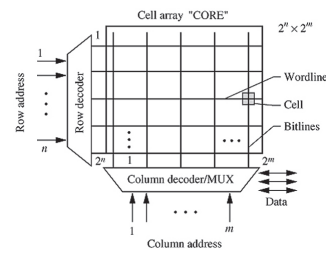


## 3. Memory

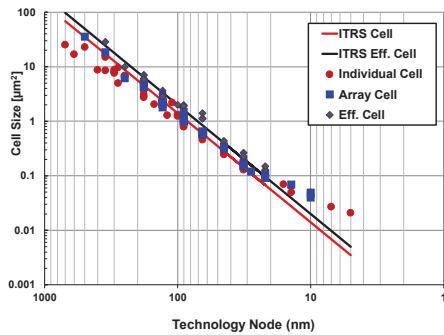


## Basic Memory Array (From 151/251A)

- Core
  - Wordlines to access rows
  - Bitlines to access columns
  - Data multiplexed onto columns
- Decoders
  - Addresses are binary
  - Row/column MUXes are 'one-hot' - only one is active at a time

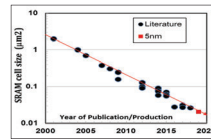


## SRAM Cell Trends

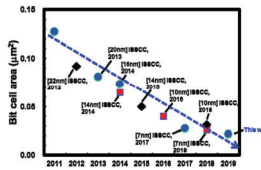


## SRAM Scaling or Not?

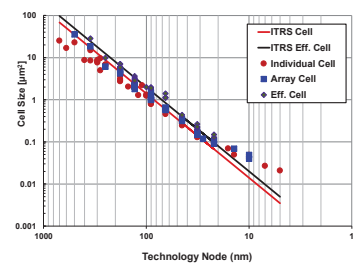
- TSMC at IEDM'19



- TSMC at ISSCC'20



- Bora's spreadsheet



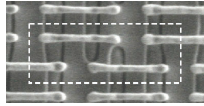
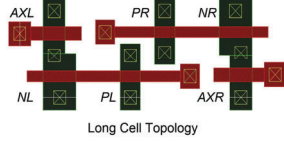
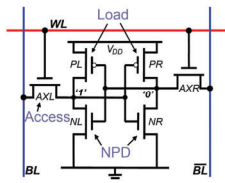
## SRAM Topics

- Basics and trends
- Static retention margin
- Static read/write margins
- Dynamic margins
- Assist techniques
- Periphery, redundancy and error correction
- Scaling options

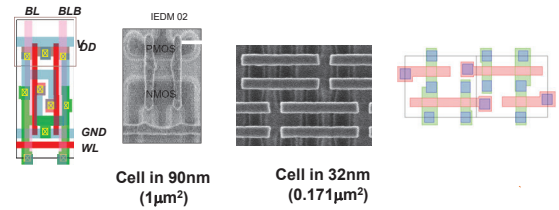


## 3. Memory 3.A SRAM Basics and Trends

# 6-T SRAM Cell

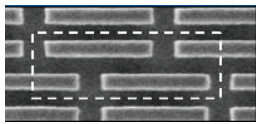


# SRAM Cell Design Trends



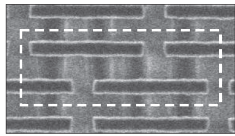
- Key enabling technology:
- Impact:

# SRAM Cell Trends (22nm)



0.092µm² cell in 22nm from Intel (IDF'09)

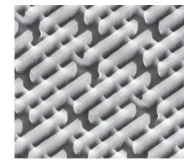
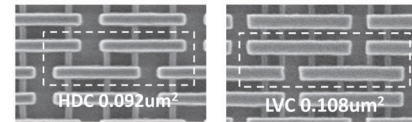
- A little analysis by using a ruler:
- Aspect ratio 2.9
  - Height ~178nm, Width ~518nm
  - Gate ~45nm (Lg is smaller)



0.346µm² cell in 45nm from Intel (IEDM'07)

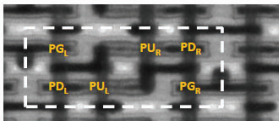
# 22nm SRAM – Discrete Widths

- FinFET cell design



E. Karl, ISSCC'12

# 14nm SRAM

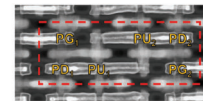


- Aspect ratio ~2.5
- Cell area = 0.05µm²
  - Height = 140nm (2 gate p)
  - Width = 350nm
  - Lg ~ 32nm

E. Karl, ISSCC'15

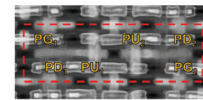
# 10nm SRAM

HDC  
0.0312 µm²



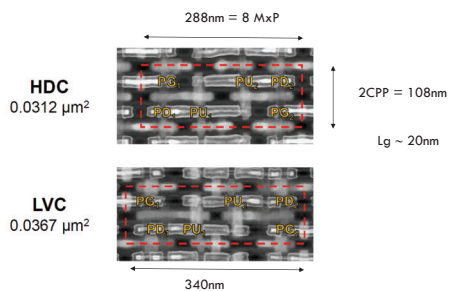
- HDC 1:1:1
- LVC 1:1:2

LVC  
0.0367 µm²



Guo, ISSCC'18

# 10nm SRAM + Ruler



# Next Lecture

- SRAM read and write