Announcements

- Assignment 2 due on Friday
- Quiz 2 on Tuesday, March 10

Outline

- Module 3
  - Design of flip-flops
  - SRAM basics

Lecture 11 Errata

- Latch $t_{DQ}$ (with $C_L = C_{IN}$)
  - $t_{DQ} \approx 4.9 \times t_{\text{setup}} \sim 1.25 \text{ FO4}$ (not 1.25 FO4)
  - $t_{\text{setup}} \approx 6.6 \times t_{\text{setup}} \sim 1.3 \text{ FO4}$ (not 1.55 FO4)

Key Point

- Two ways to design a flip-flop
  - Latch pair
  - Pulsed latch

Types of Flip-Flops

- Latch Pair
  - (Master-Slave)
- Pulse-Triggered Latch
Latch Pair as a Flip-Flop

Master-Slave Latch Pairs
* Example: PowerPC 603 (Gerosa, JSSC 12/94)

Flip-Flop Timing Characterization
* Combinational logic delay is a function of output load and input slope
* Sequential timing (flip-flop):
  * $t_{dQ}$ is function of output load and clock rise time
  * $t_{dQ}, t_r$ are functions of D and Clk rise/fall times

Pulse-Triggered Latches
* First stage is a pulse generator
  * generates a pulse (glitch) on a rising edge of the clock
* Second stage is a latch
  * captures the pulse generated in the first stage
* Pulse generation results in a negative setup time
* Frequently exhibit a soft edge property
* Note: power is always consumed in the pulse generator
  * Often shared by a group (register)

Pulsed Latch
Simple pulsed latch

Intel/HP Itanium 2

Flip-Flop Clk-Q, setup, hold
Pulsed Latches

Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC'96

Hybrid Latch Flip-Flop

Skew absorption

Partovi et al, ISSCC'96

HLFF Operation

1-0 and 0-1 transitions at the input with 0ps setup time

Pulsed Latches

AMD K-7

Inputs are dynamically received
Clock edge is fast

To 3 other flip-flops


Sense-Amplifier-Based Flip-Flop

DEC Alpha 21264, StrongARM 110

First stage is a sense amplifier, precharged to
high, when Clk = 0
After rising edge of the clock sense amplifier
generates the pulse on
S or R
The pulse is captured in
S-R latch
Cross-coupled NAND has different propagation
delays of rising and falling edges

Pulsed Latches

7474, from mid-1960's

Use in synthesized flow

Partovi, VLSI'12

Pulsed Latches

Sense Amplifier-Based Flip-Flop

3. Memory

Random Access Memory Architecture
- Conceptual: Linear array of addresses
  - Each box holds some data
  - Not practical to physically realize
    - millions of 32b/64b words
- Create a 2-D array
  - Decode Row and Column address to get data

Basic Memory Array (From 151/251A)
- Core
  - Wordlines to access rows
  - Bitlines to access columns
  - Data multiplexed onto columns
- Decoders
  - Addresses are binary
  - Row/column MUXes are ‘one-hot’ - only one is active at a time

SRAM Cell Trends

SRAM Scaling or Not?
- TSMC at IEDM’19
- Bora’s spreadsheet

SRAM Topics
A. Basics and trends
B. Static retention margin
C. Static read/write margins
D. Dynamic margins
D. Assist techniques
E. Periphery, redundancy and error correction
F. Scaling options
6-T SRAM Cell

• Improve CD control by unidirectional poly
• Special SRAM design rules

SRAM Cell Design Trends

• Key enabling technology:
• Impact:

Cell in 90nm (1µm²)
Cell in 32nm (0.171µm²)

SRAM Cell Trends (22nm)

A little analysis by using a ruler:
• Aspect ratio 2.9
• Height ~178nm, Width ~518nm
• Gate ~ 4.5nm (Lg is smaller)

22nm SRAM – Discrete Widths

• FinFET cell design

14nm SRAM

• Aspect ratio ~2.5
• Cell area = 0.05µm²
• Height = 140nm (2 gate p)
• Width = 350nm
• Lg ~ 32nm

10nm SRAM

• HDC 1:1:1
• LVC 1:1:2

10nm SRAM + Ruler

• SRAM read and write