

EE241B : Advanced Digital Circuits

Lecture 12 – Flip-Flops, Memory

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March 3, 2020,

Presidential primary election

Announcements

- **Assignment 2 due on Friday**
 - Quiz 2 on Tuesday, March 10



Outline

- **Module 3**
 - Design of flip-flops
 - SRAM basics



3. Design for Performance

3.D Latch Design

Lecture 1 1 Errata

- Latch t_{D-Q} (with $C_L = C_{in}$)
 - $t_{D-Q} = 4.9 t_{unit} \sim 1 \text{ FO4}$ (not 1.25 FO4)
 - $t_{su} = 6.6 t_{unit} \sim 1.3 \text{ FO4}$ (not 1.55 FO4)



3. Design for Performance

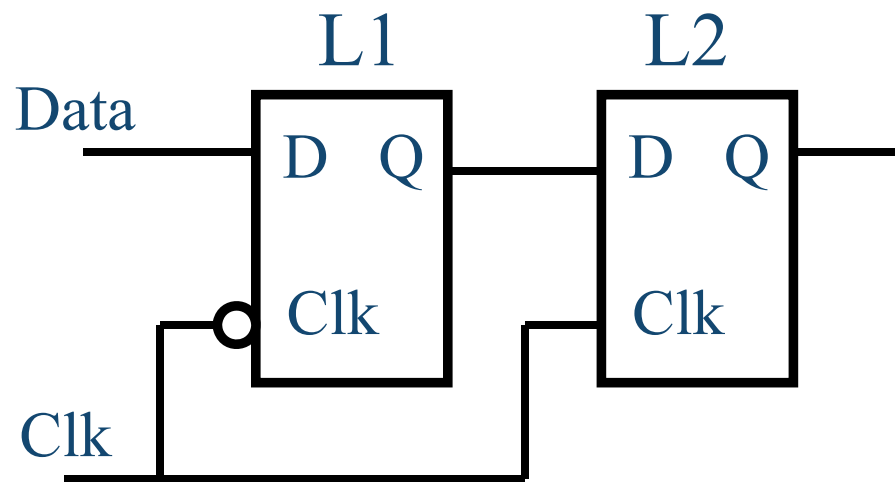
3.E Flip-Flop Design

Key Point

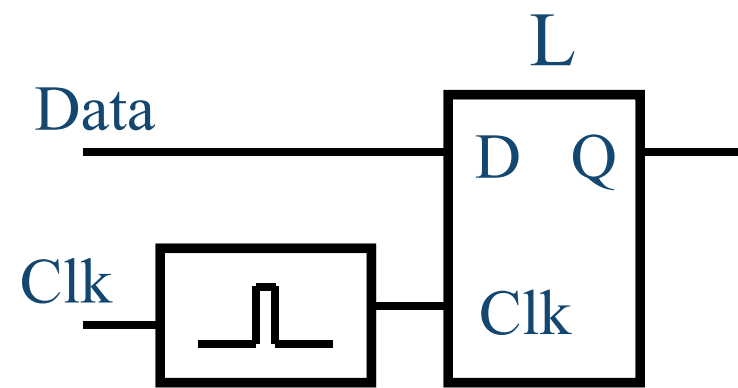
- Two ways to design a flip-flop
 - Latch pair
 - Pulsed latch

Types of Flip-Flops

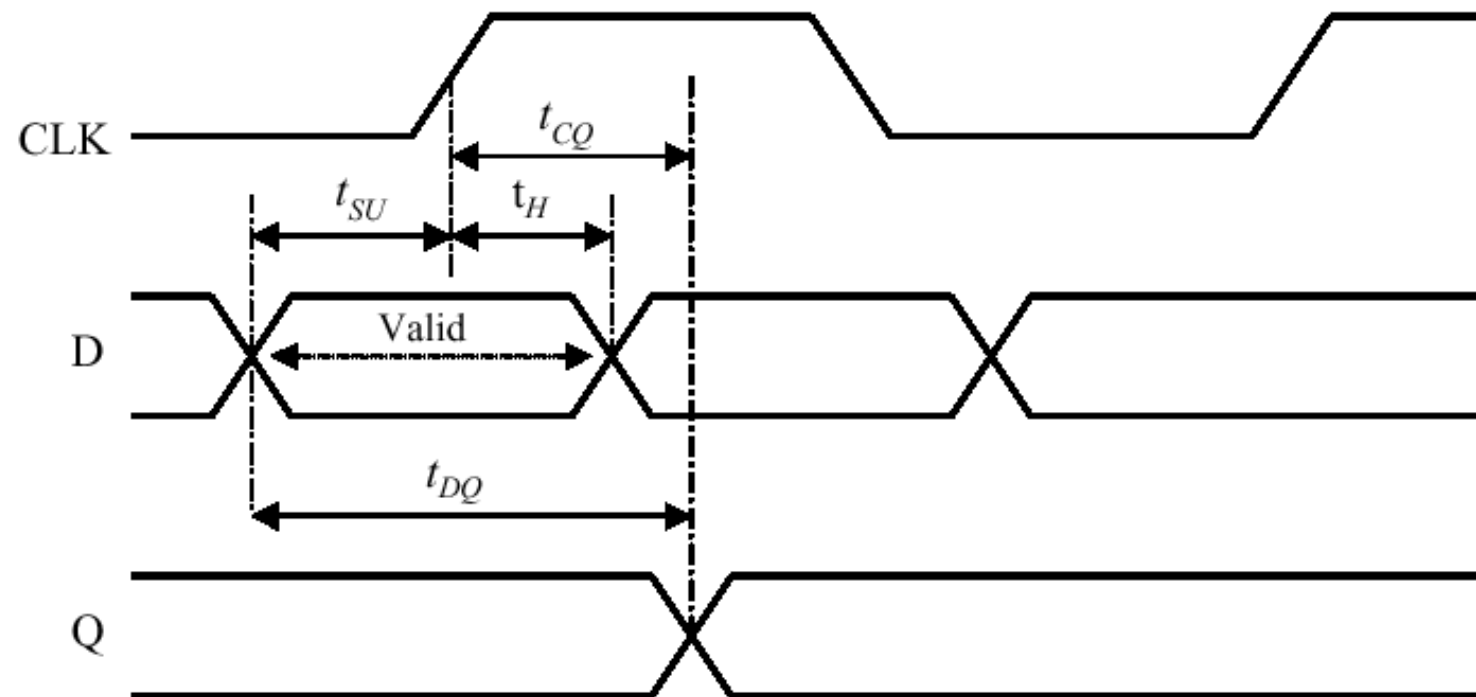
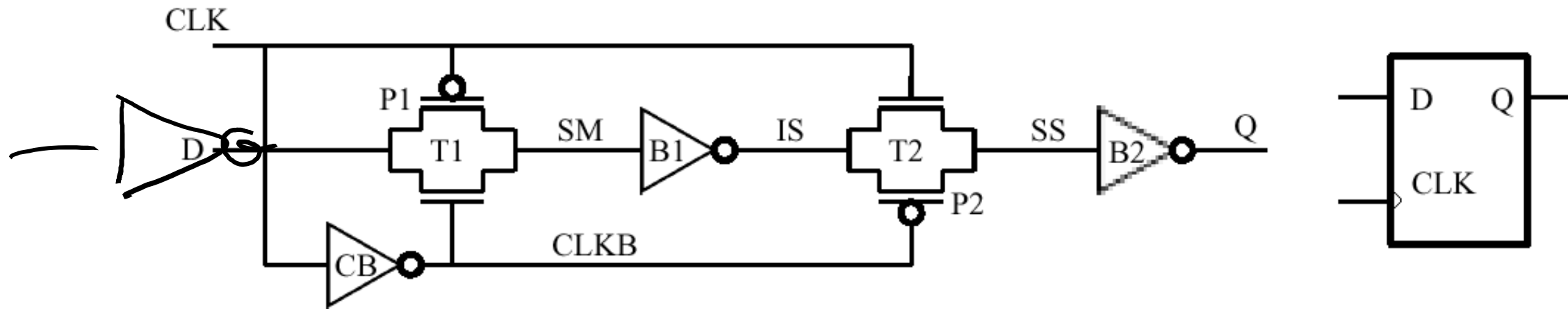
Latch Pair (Master-Slave)



Pulse-Triggered Latch

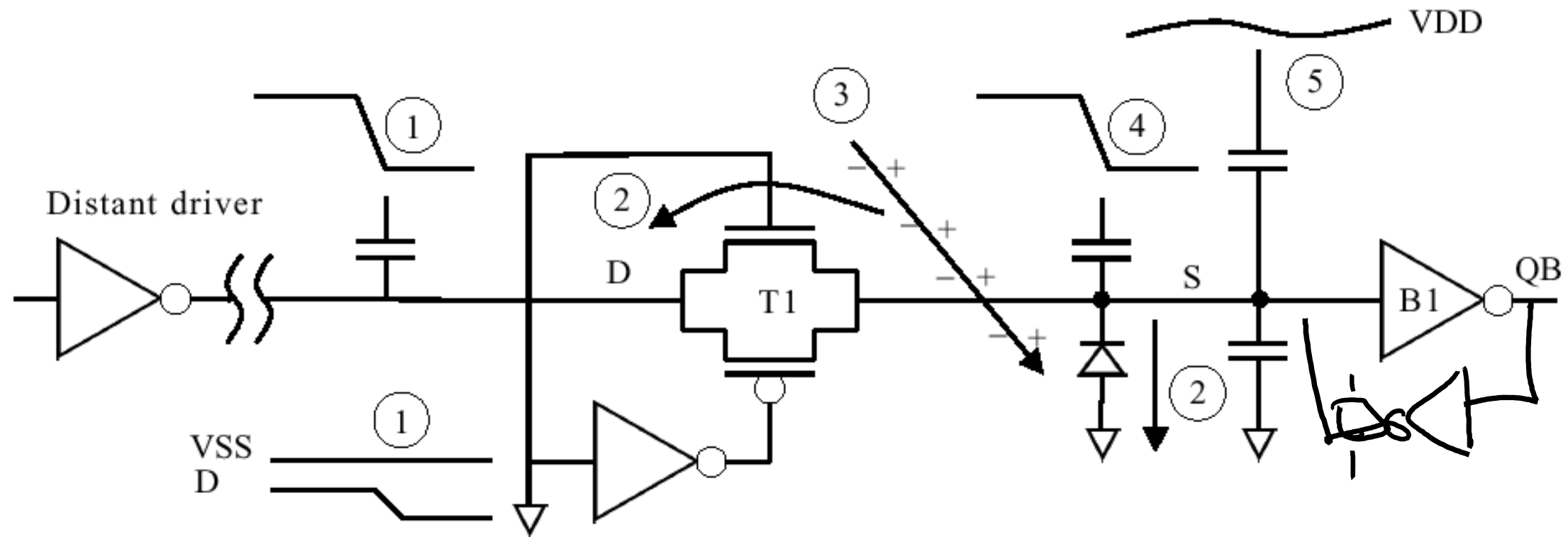


Latch Pair as a Flip-Flop



Sources of Noise

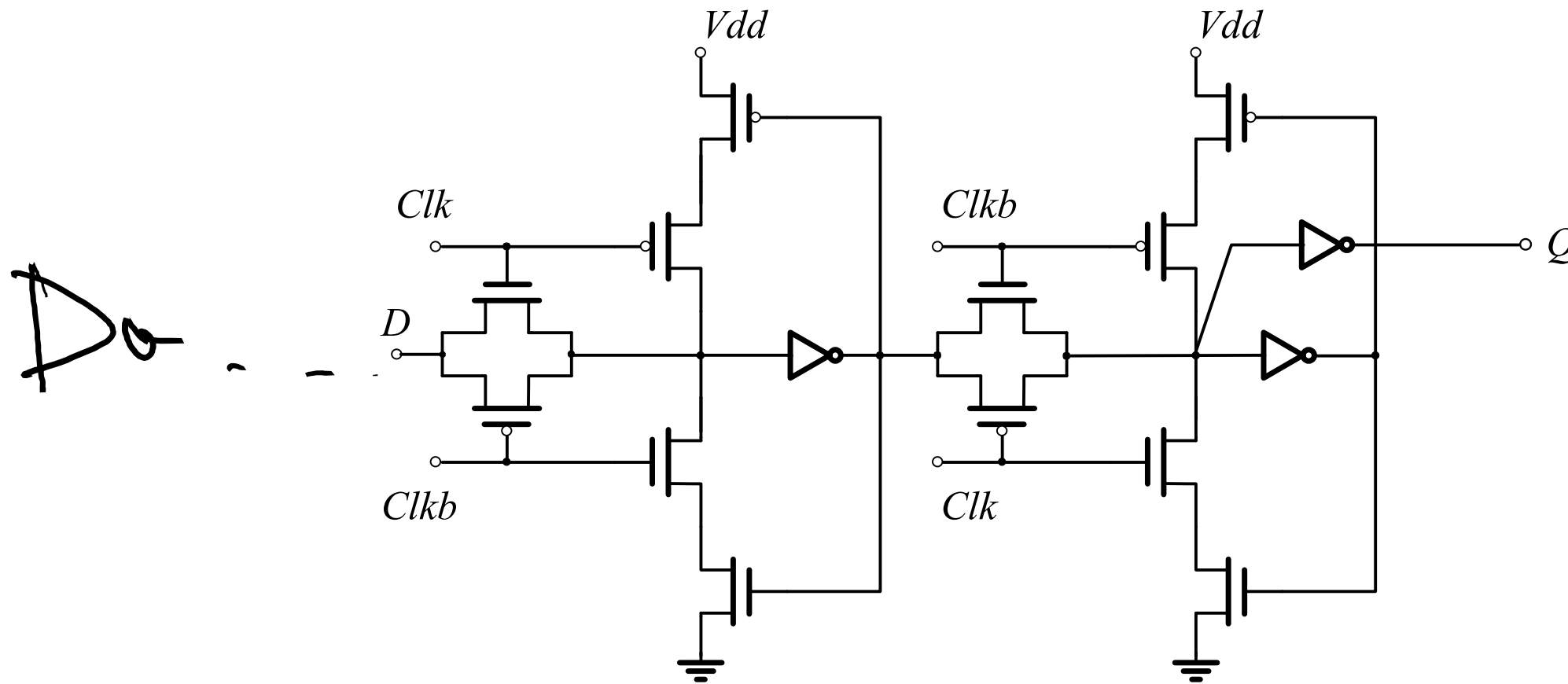
- ① Noise on input
- ② Leakage
- ③ α -Particle and cosmic rays
- ④ Unrelated signal coupling
- ⑤ Power supply ripple



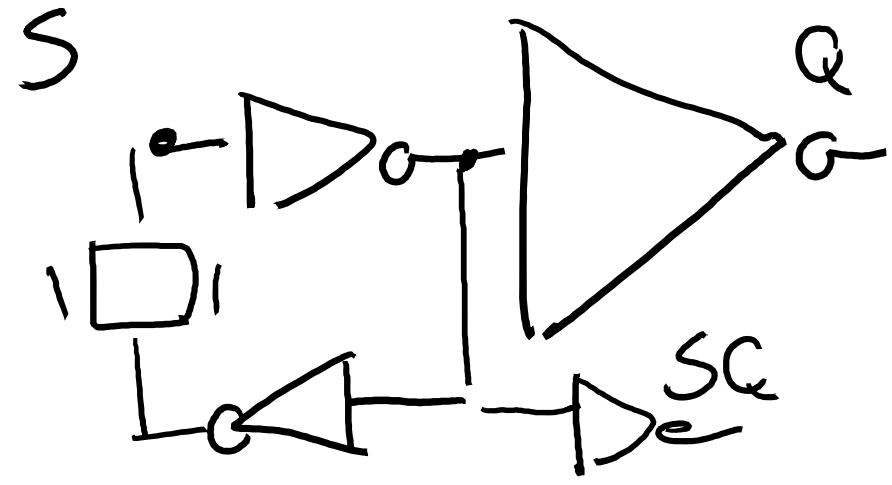
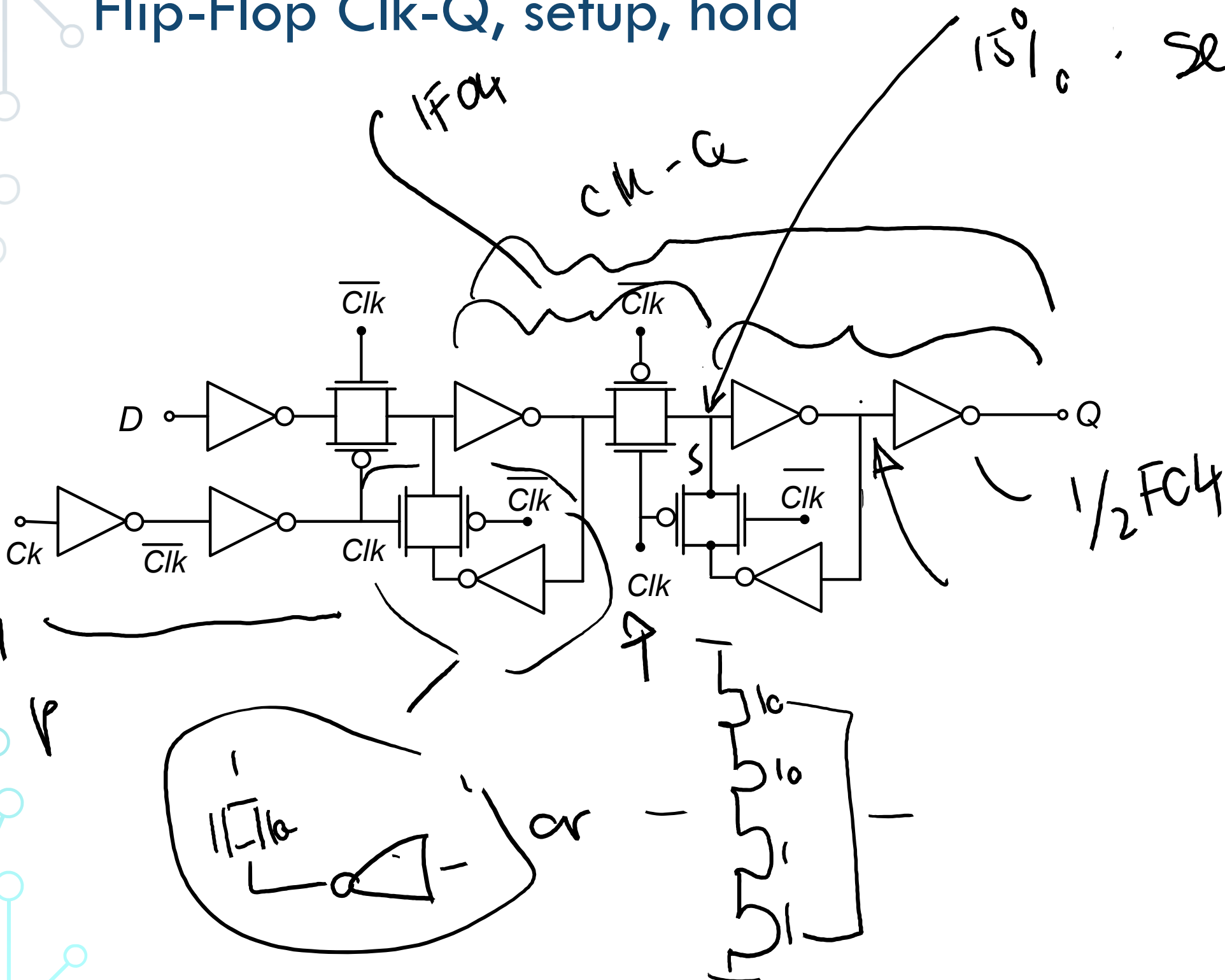
Courtesy of IEEE Press, New York. © 2000

Master-Slave Latch Pairs

- Example: PowerPC 603 (Gerosa, JSSC 12/94)

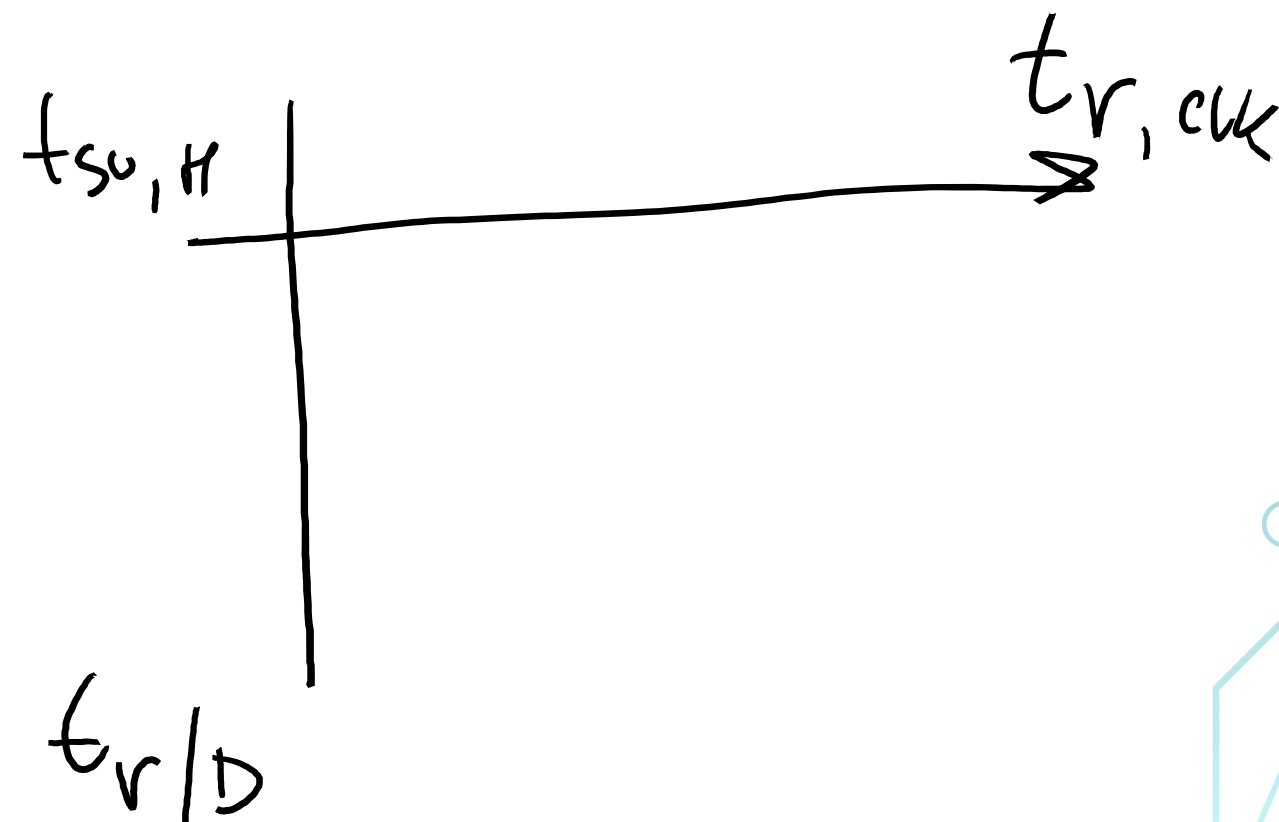
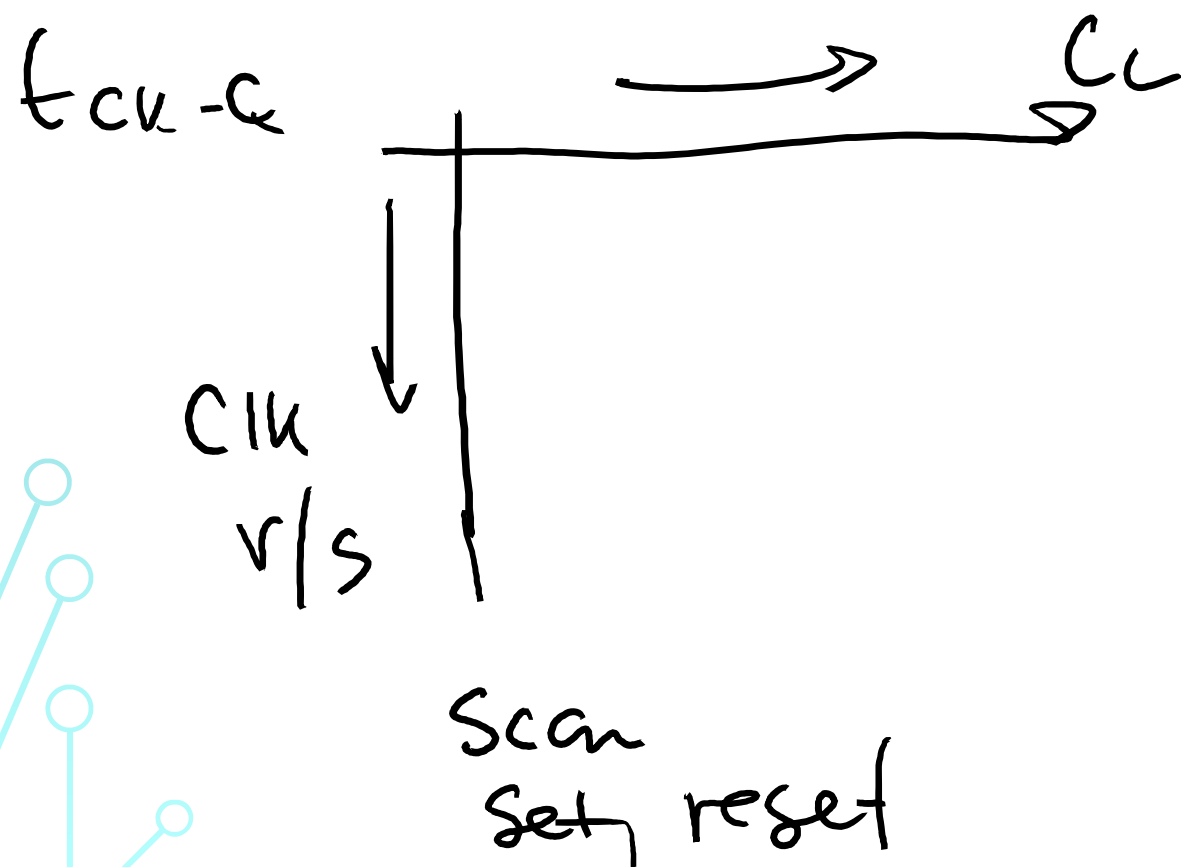


Flip-Flop Clk-Q, setup, hold



Flip-Flop Timing Characterization

- Combinational logic delay is a function of output load and input slope
- Sequential timing (flip-flop):
 - $t_{\text{clk-q}}$ is function of output load and clock rise time
 - $t_{\text{su}}, t_{\text{H}}$ are functions of D and Clk rise/fall times

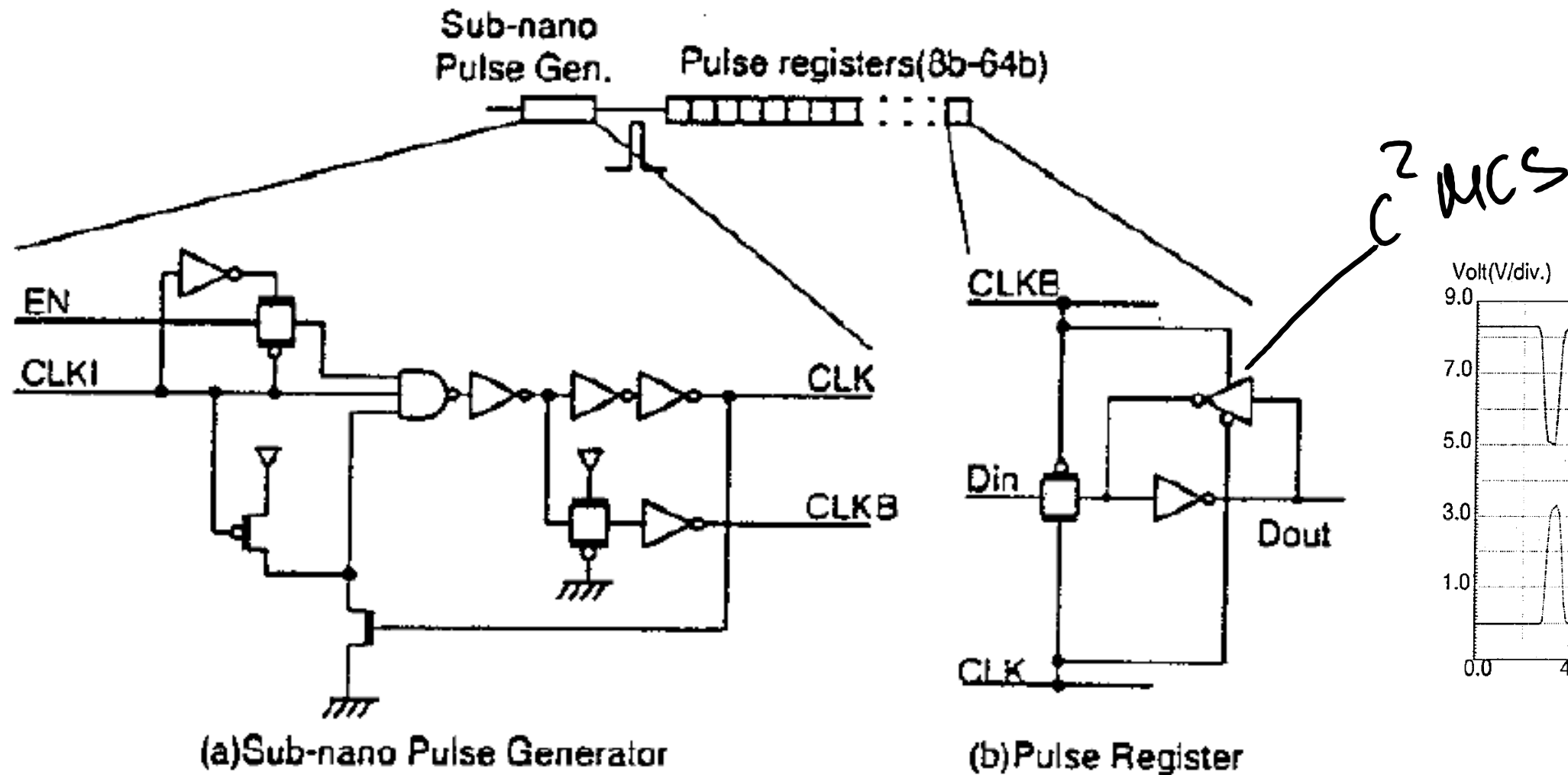


Pulse-Triggered Latches

- First stage is a pulse generator
 - generates a pulse (glitch) on a rising edge of the clock
- Second stage is a latch
 - captures the pulse generated in the first stage
- Pulse generation results in a negative setup time
- Frequently exhibit a soft edge property
- Note: power is always consumed in the pulse generator
 - Often shared by a group (register)

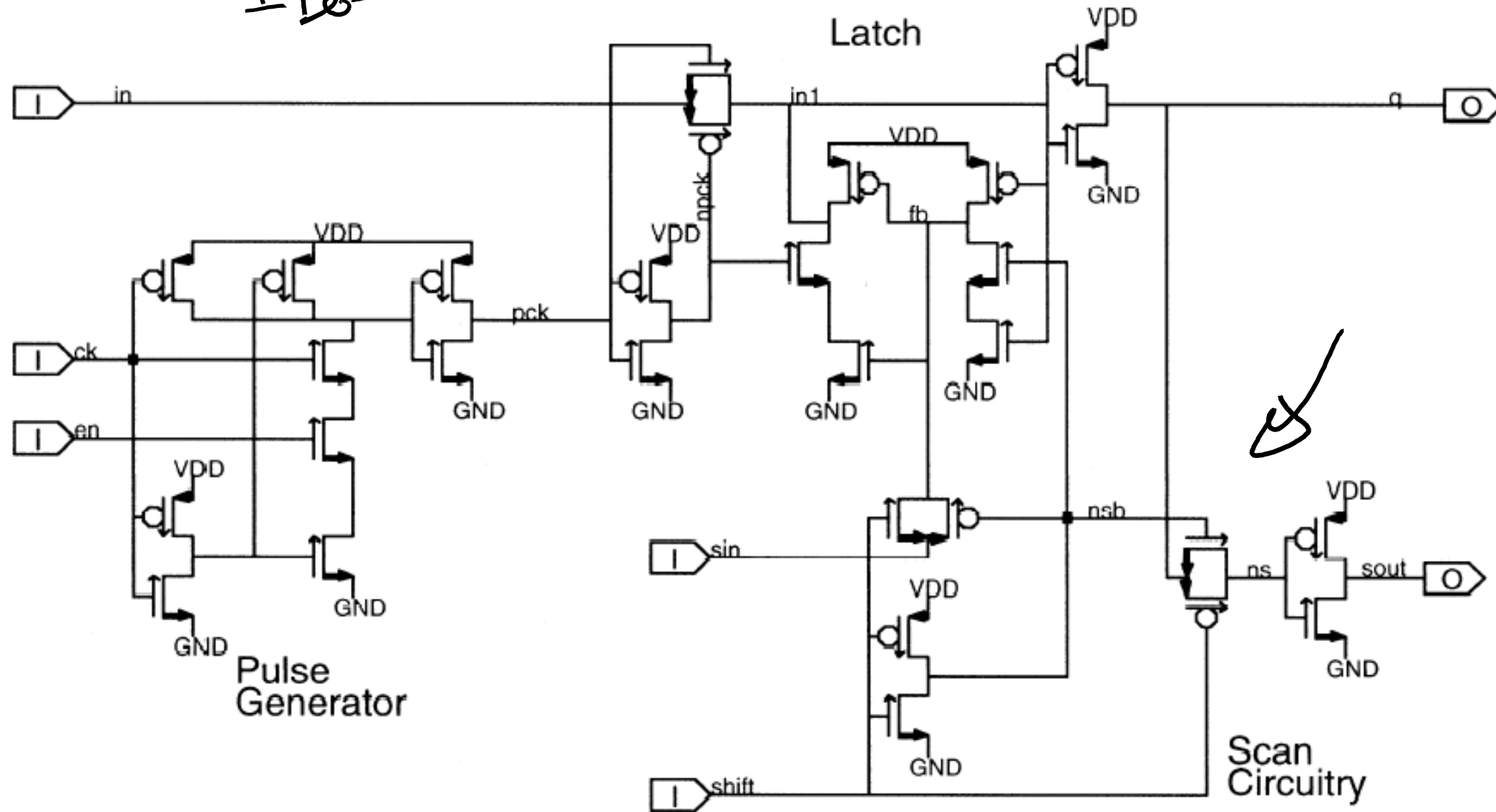
Pulsed Latch

Simple pulsed latch



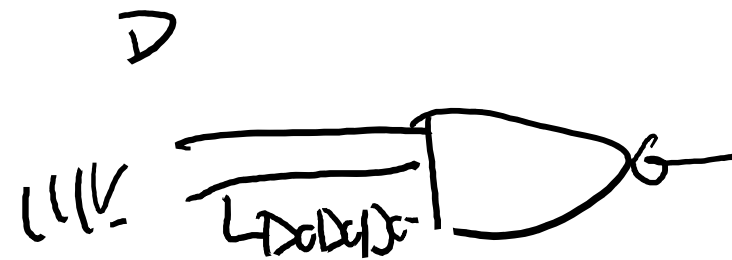
Kozu, ISSCC'96

Intel/HP Itanium 2

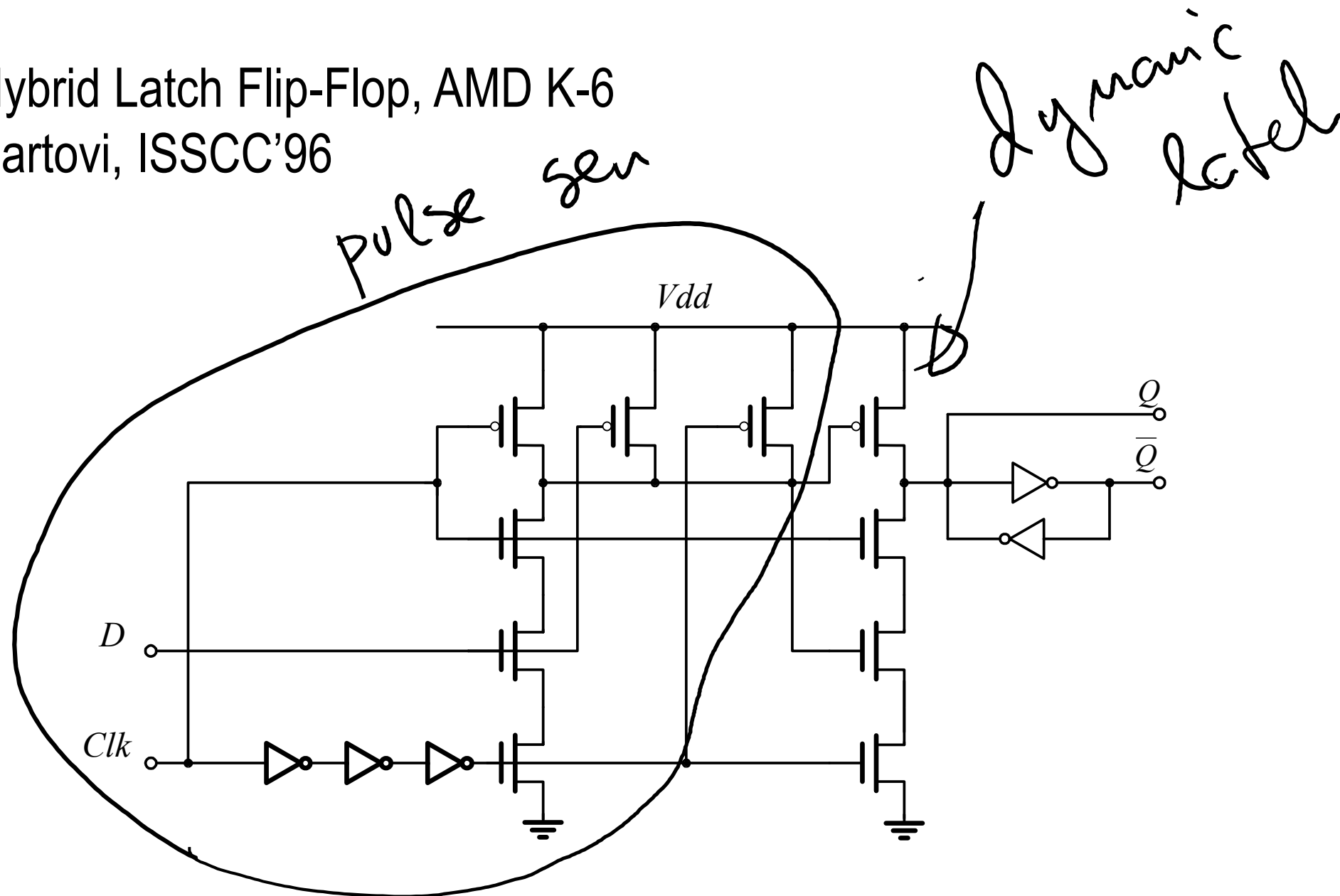


Naffziger, ISSCC'02

Pulsed Latches

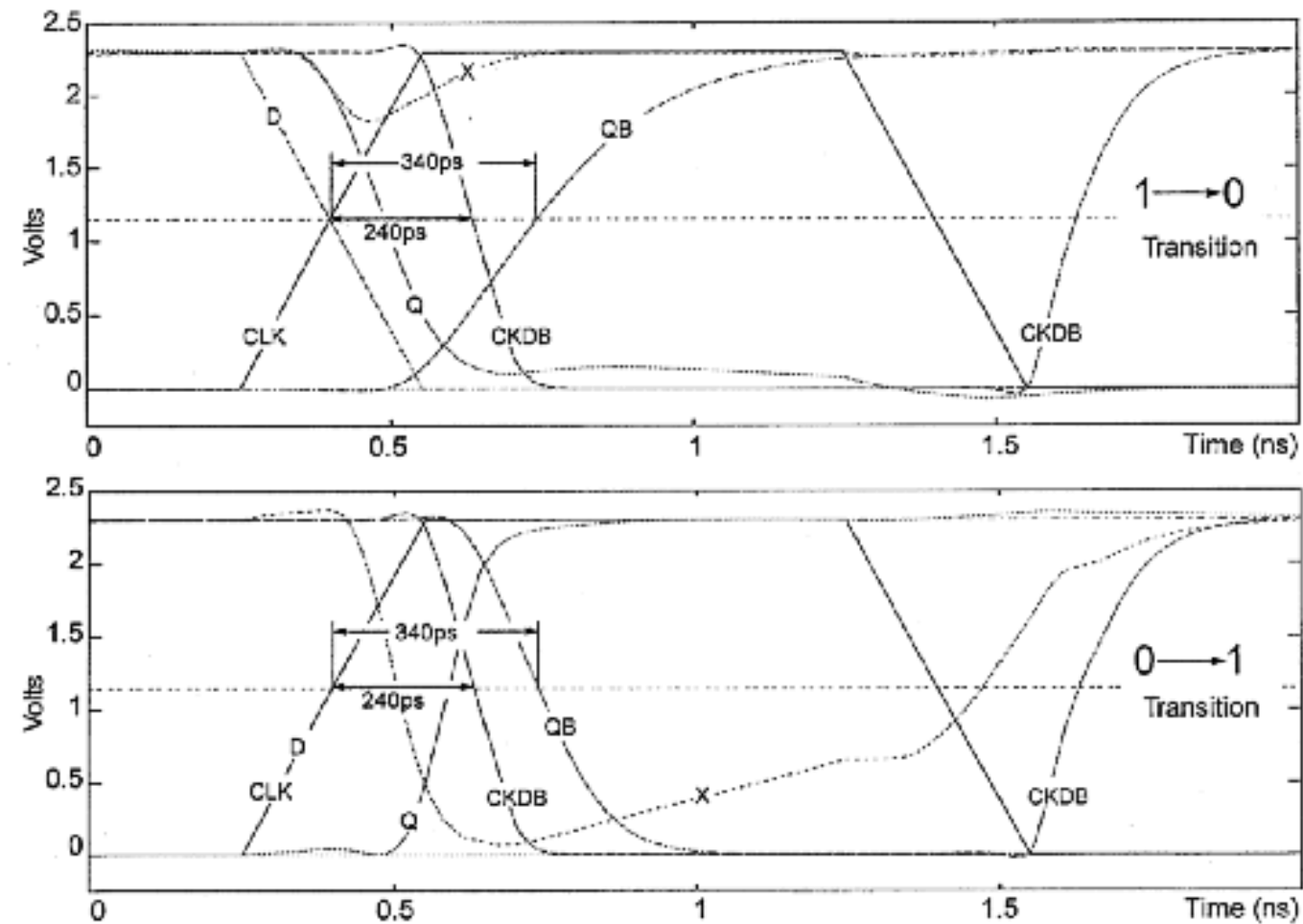


Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC'96



HLFF Operation

1-0 and 0-1 transitions at the input with 0ps setup time

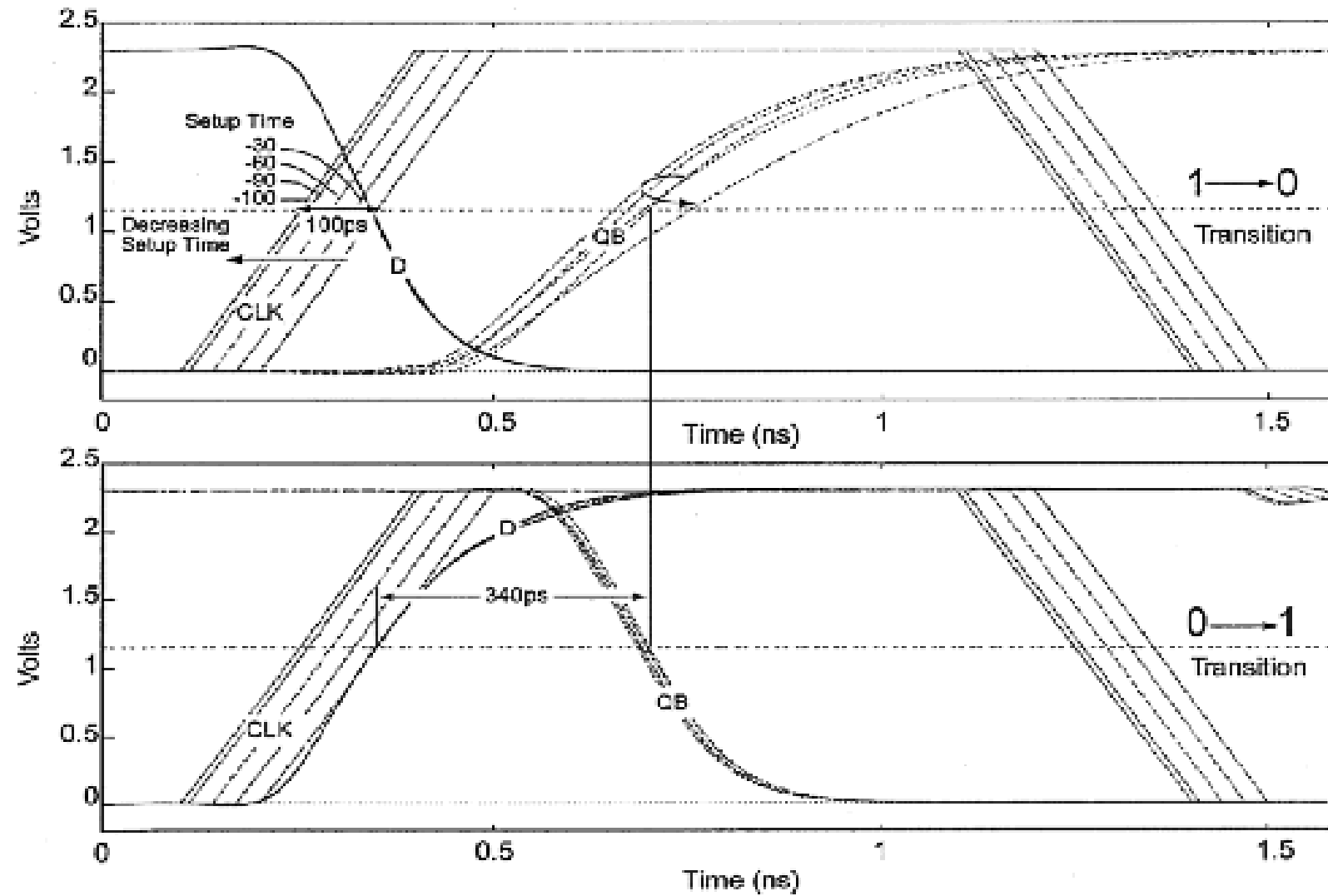


VDD=2.3v, 85°C, Typical Devices
C_{clk} = 60ff, C_{qb} = 300ff

T_{cq} = T_{dq} = 340ps
T_{hold} = 180ps
T_{su(min)} = -90ps

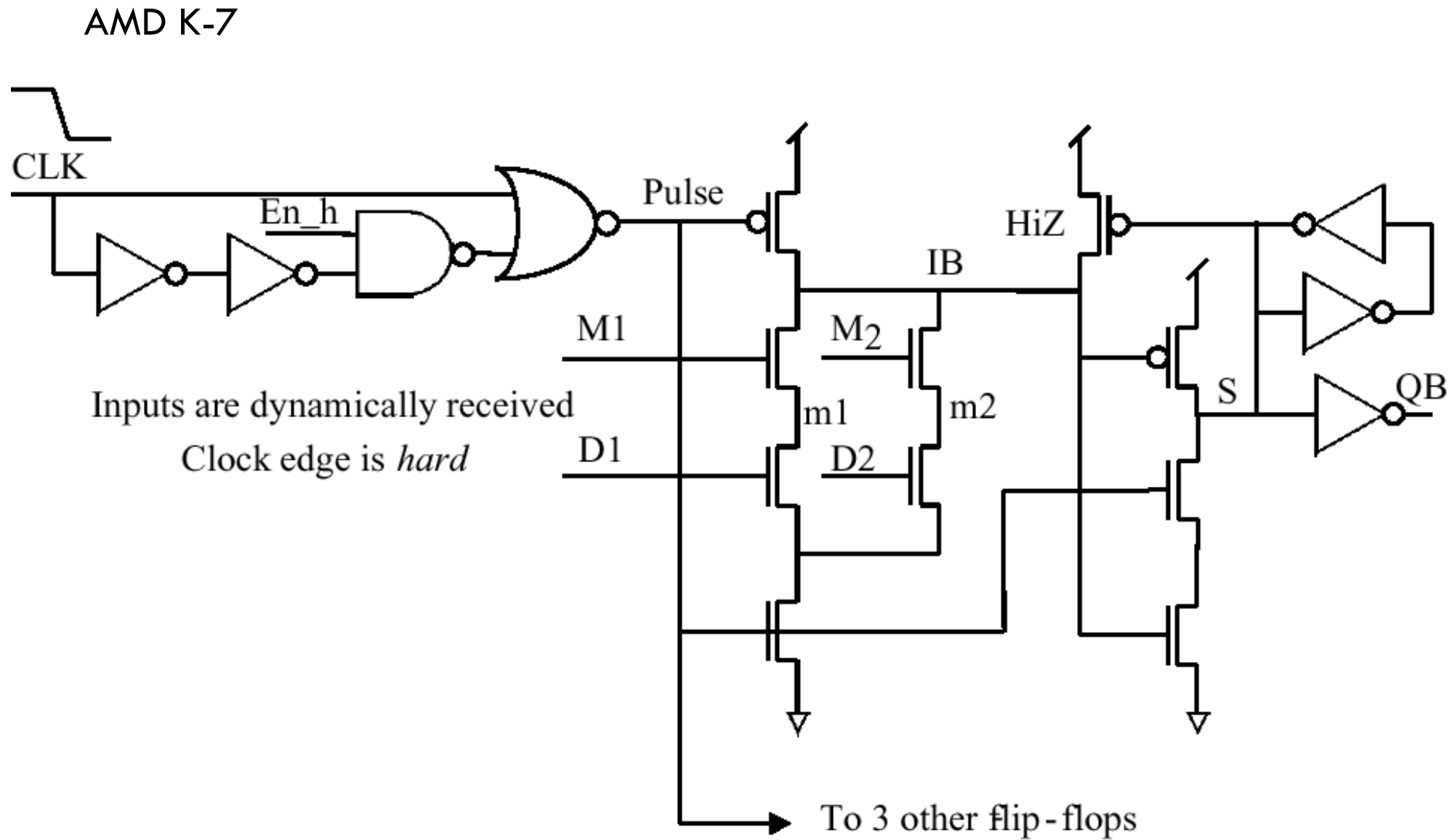
Hybrid Latch Flip-Flop

Skew absorption

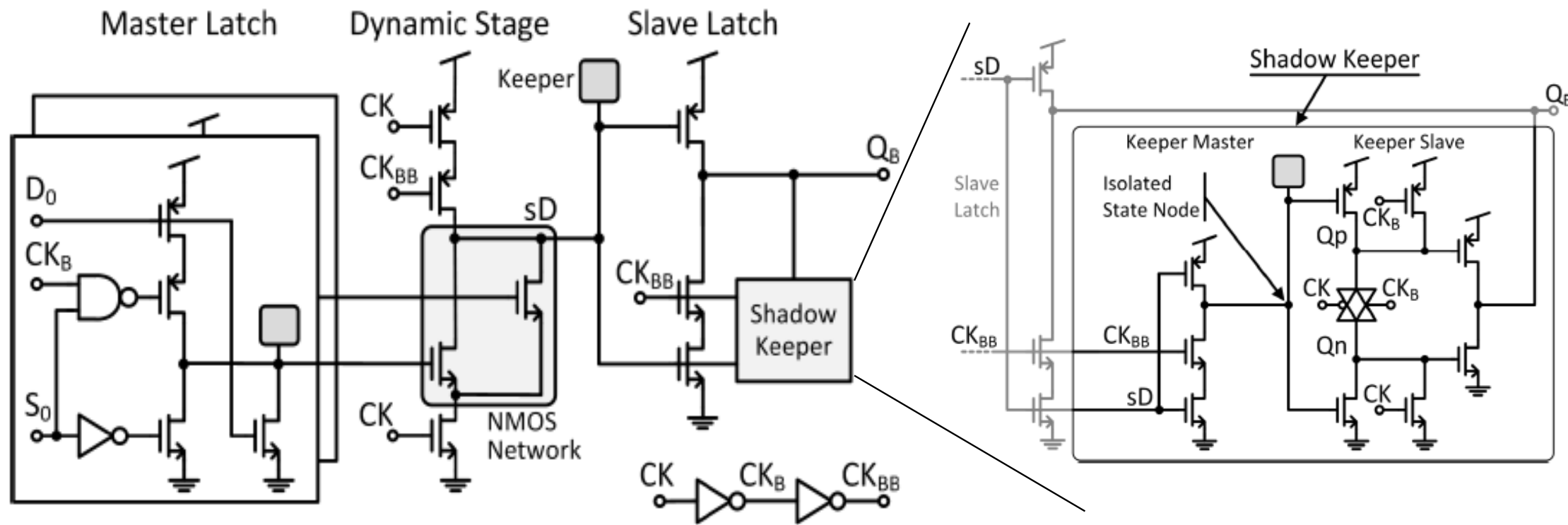


Partovi et al, ISSCC'96

Pulsed Latches



Pulsed Latches

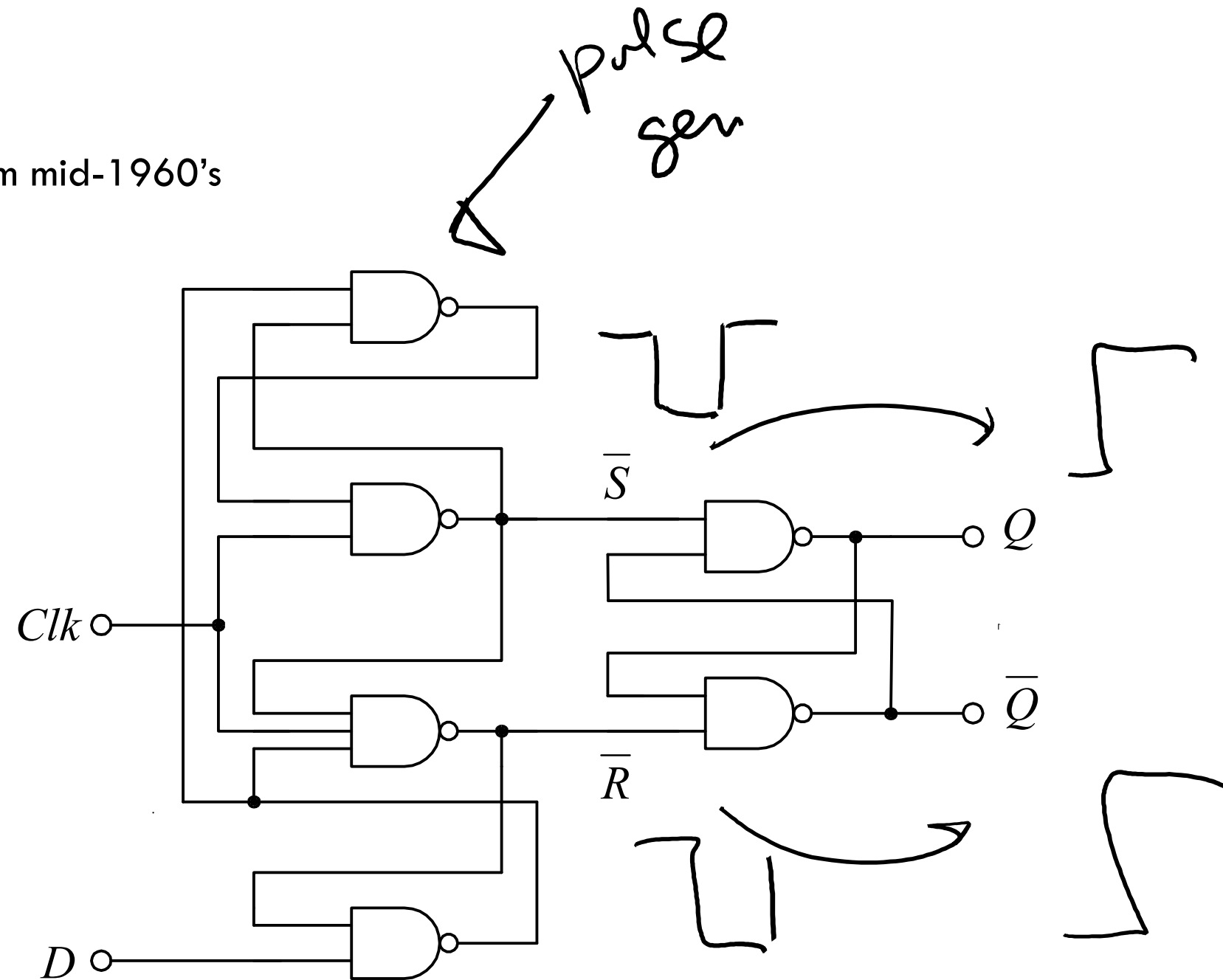


Used in a synthesized flow

Partovi, VLSI'12

Pulsed Latches

7474, from mid-1960's



Pulsed Latches

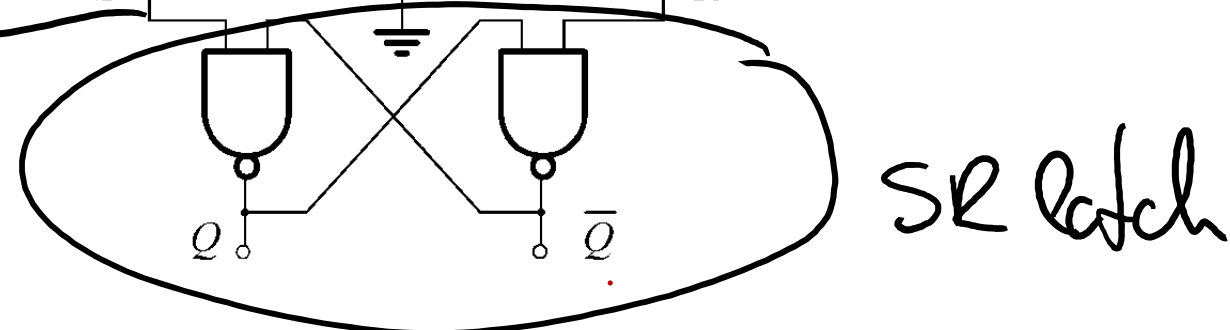
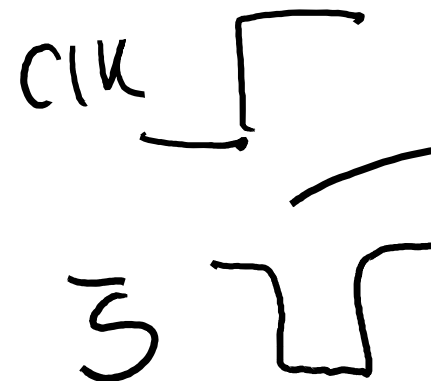
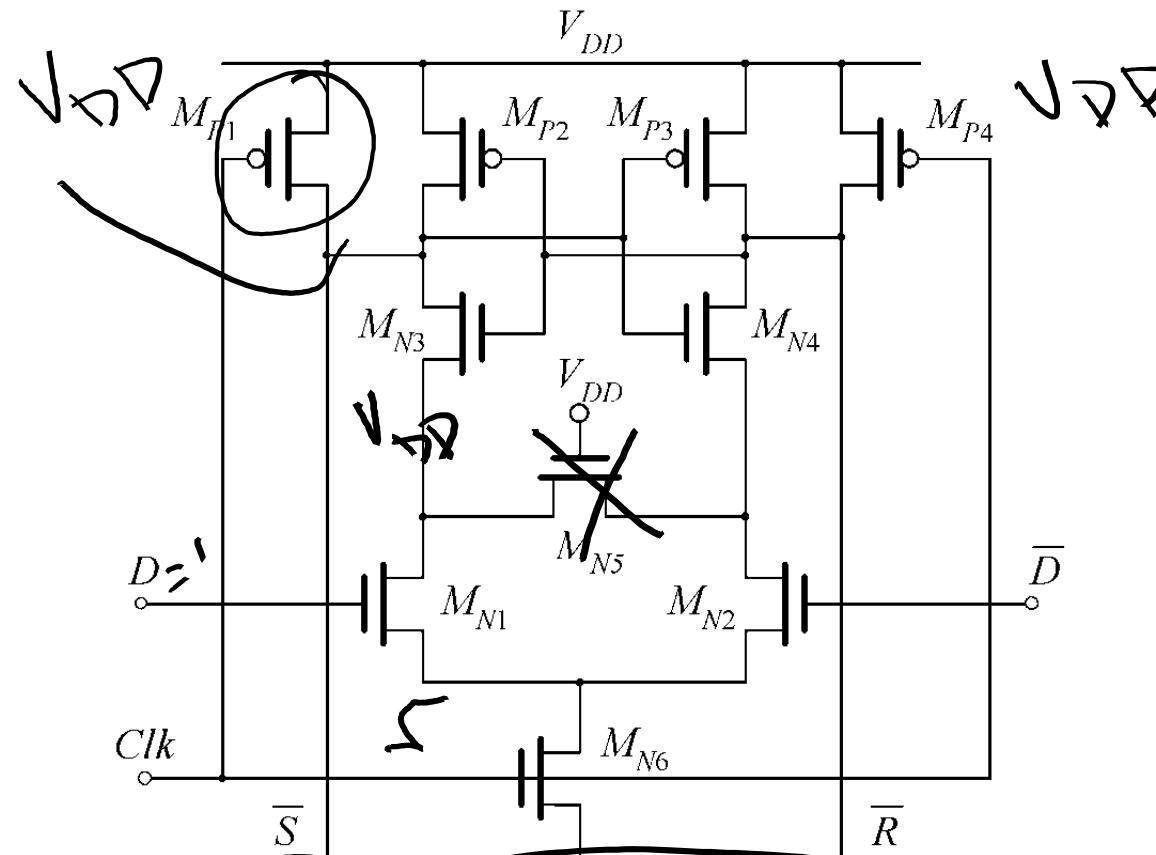
Sense-amplifier-based flip-flop, Matsui 1992.
DEC Alpha 21264, StrongARM 110

First stage is a sense amplifier, precharged to high, when $Clk = 0$

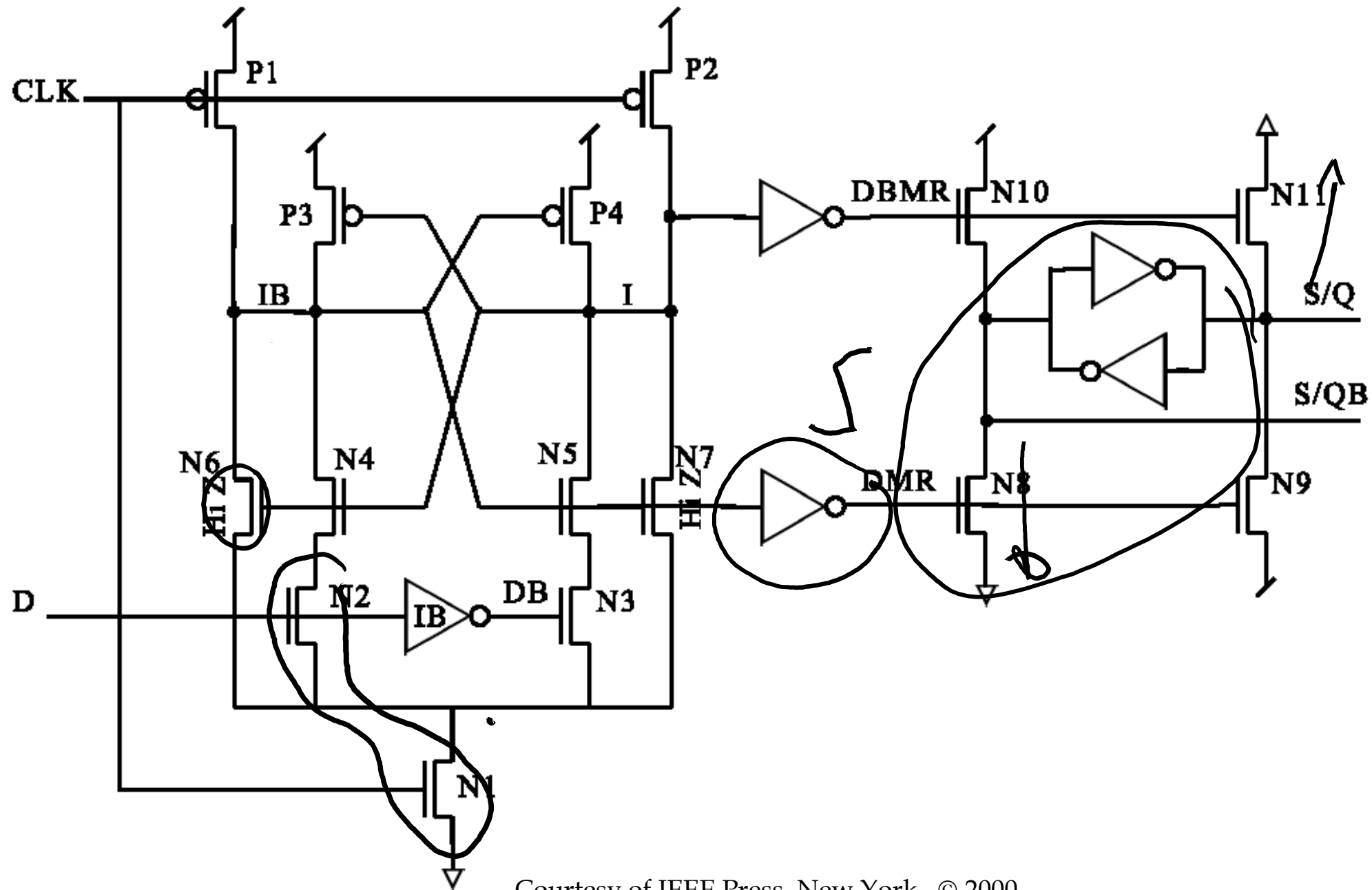
After rising edge of the clock sense amplifier generates the pulse on S or R

The pulse is captured in S-R latch

Cross-coupled NAND has different propagation delays of rising and falling edges

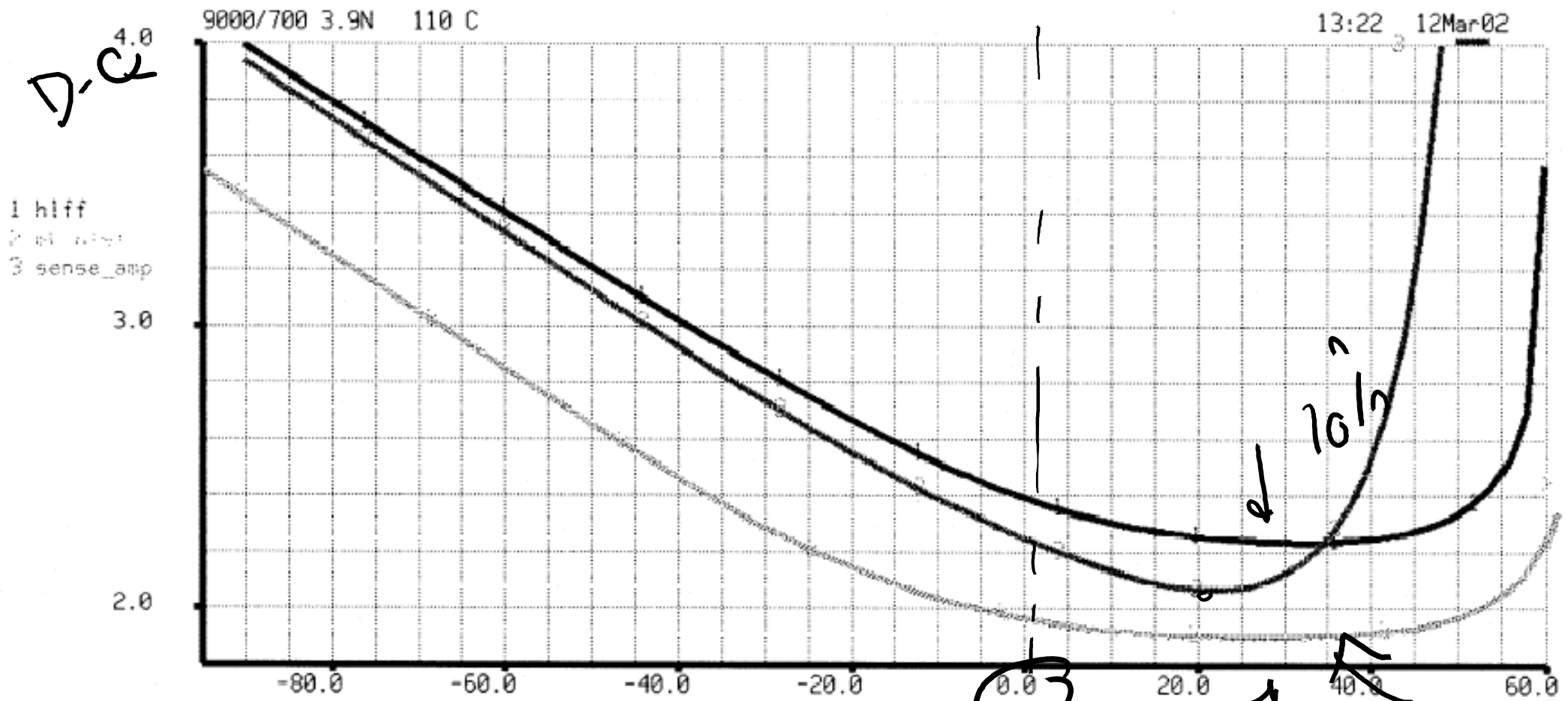


Sense Amplifier-Based Flip-Flop



Courtesy of IEEE Press, New York. © 2000

Sampling Window Comparison



D-Q
1 hiff
2
3 sense_amp

D-CLK

TG

10/2

Naffziger, JSSC 11/02

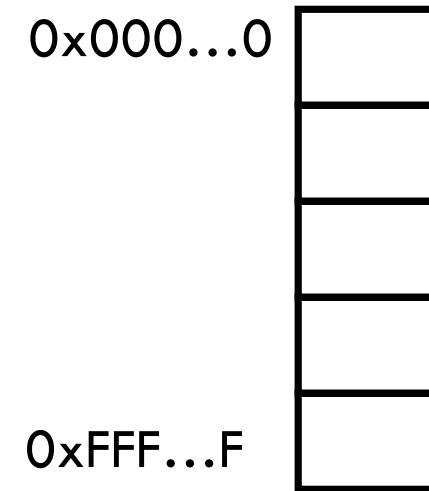
Horium II



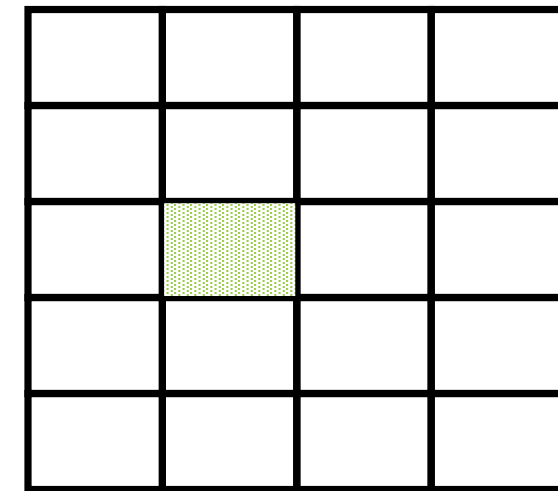
3. Memory

Random Access Memory Architecture

- **Conceptual: Linear array of addresses**
 - Each box holds some data
 - Not practical to physically realize
 - millions of 32b/64b words
- **Create a 2-D array**
 - Decode Row and Column address to get data



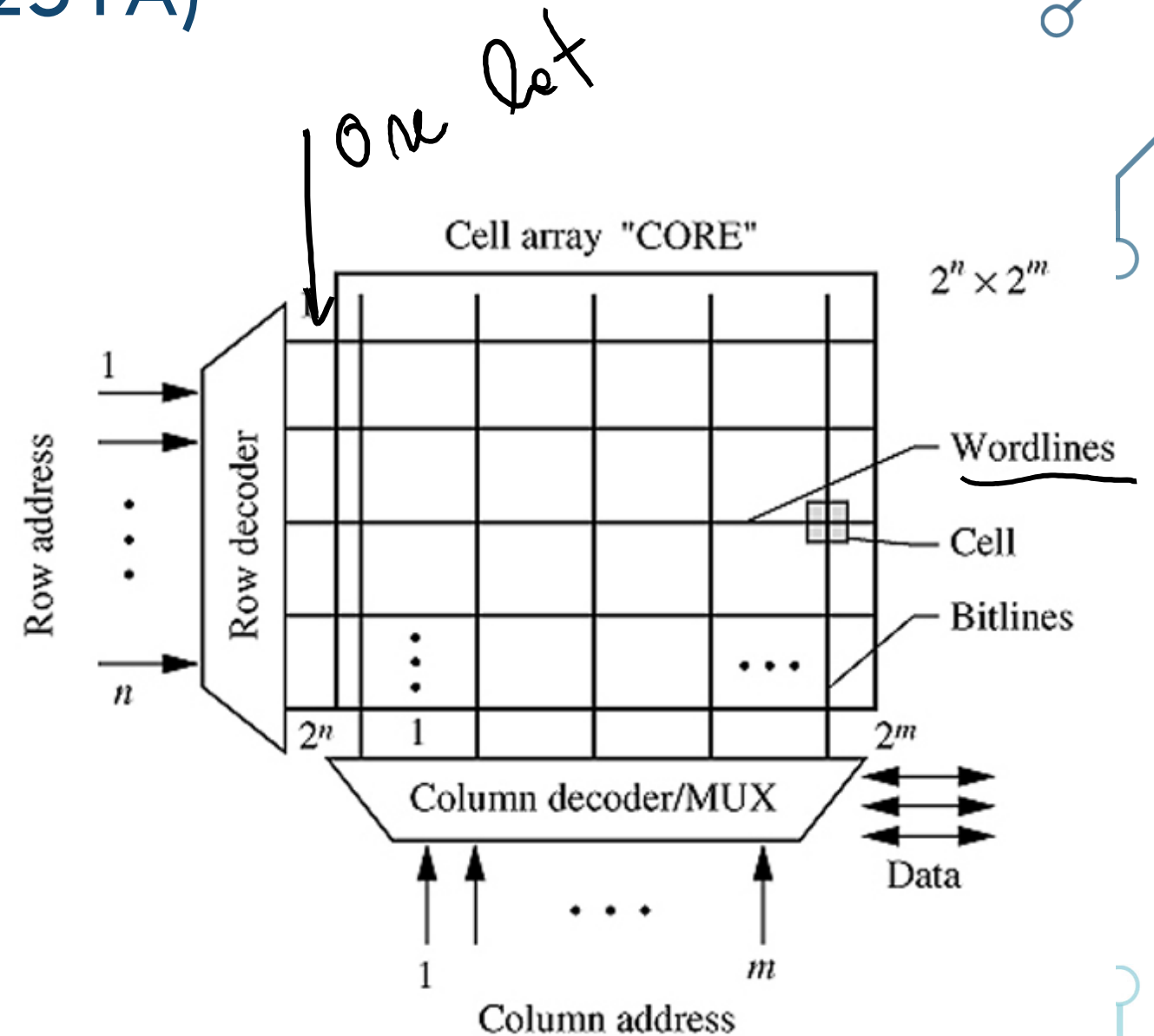
VcW



Column

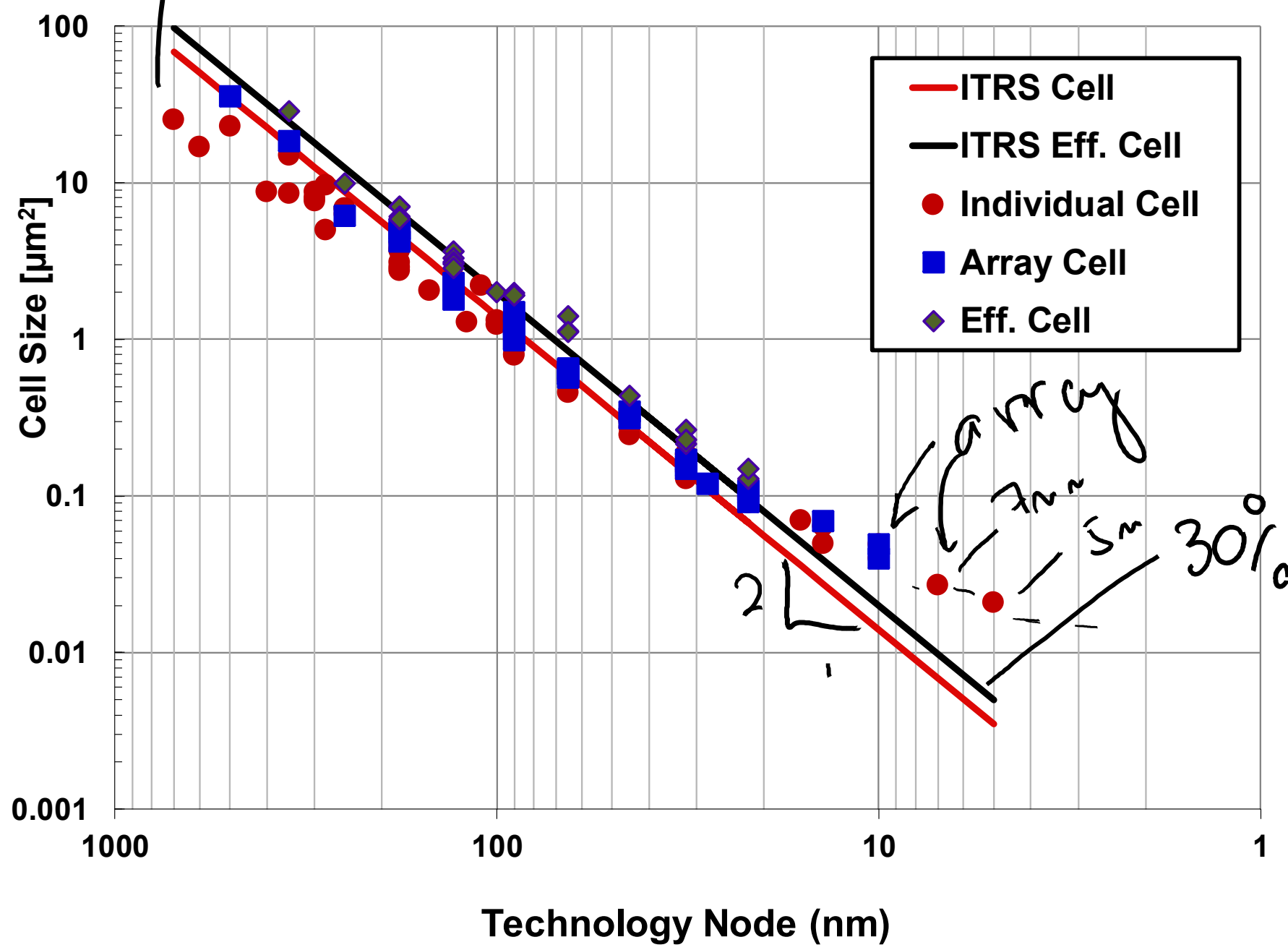
Basic Memory Array (From 151/251A)

- Core
 - Wordlines to access rows
 - Bitlines to access columns
 - Data multiplexed onto columns
- Decoders
 - Addresses are binary
 - Row/column MUXes are 'one-hot' - only one is active at a time



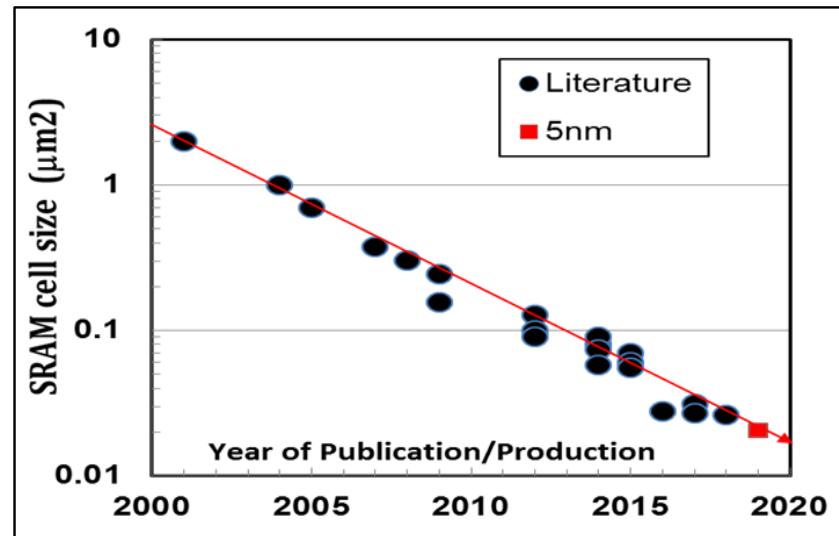
SRAM Cell Trends

2 layers
640

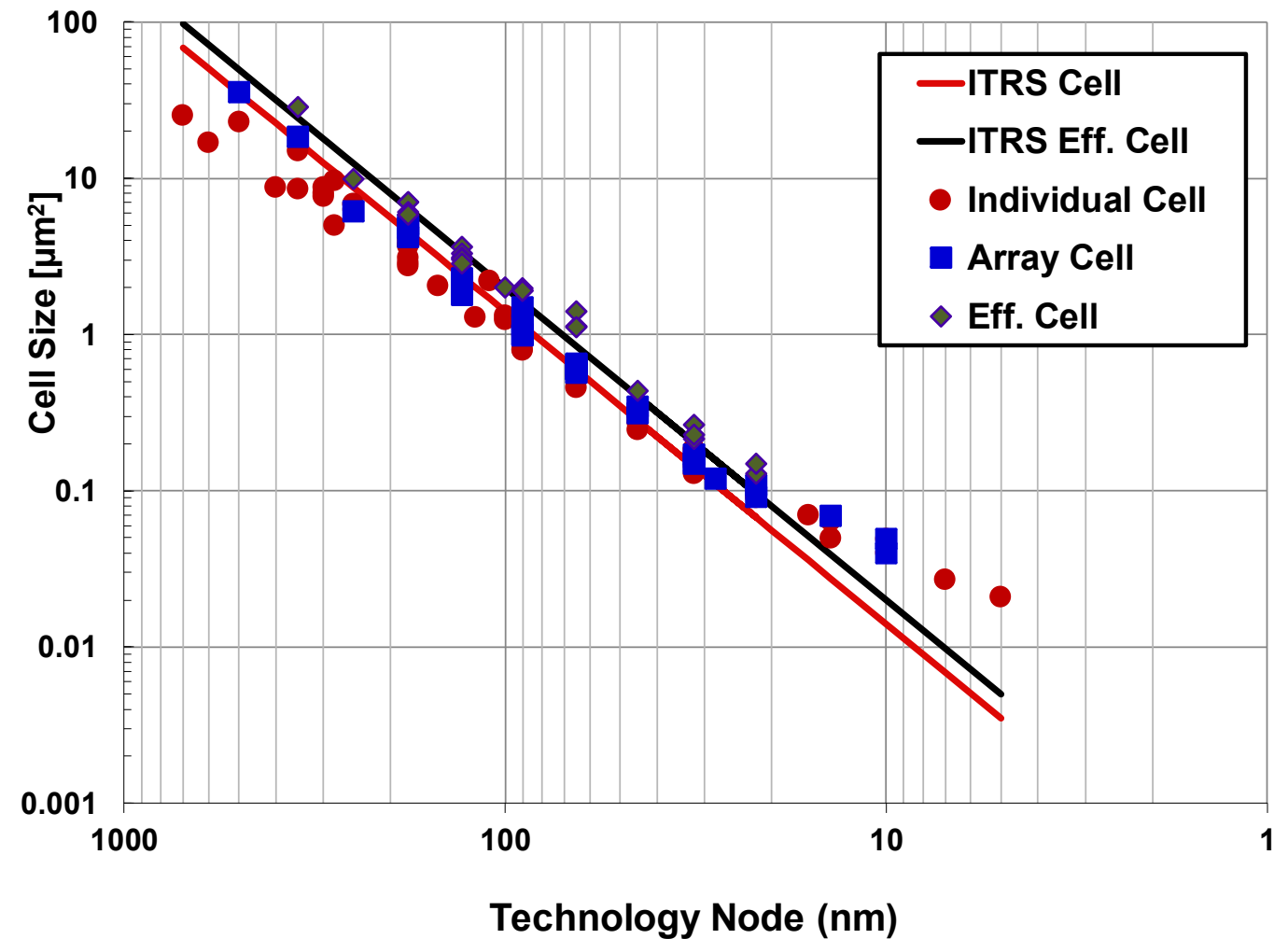


SRAM Scaling or Not?

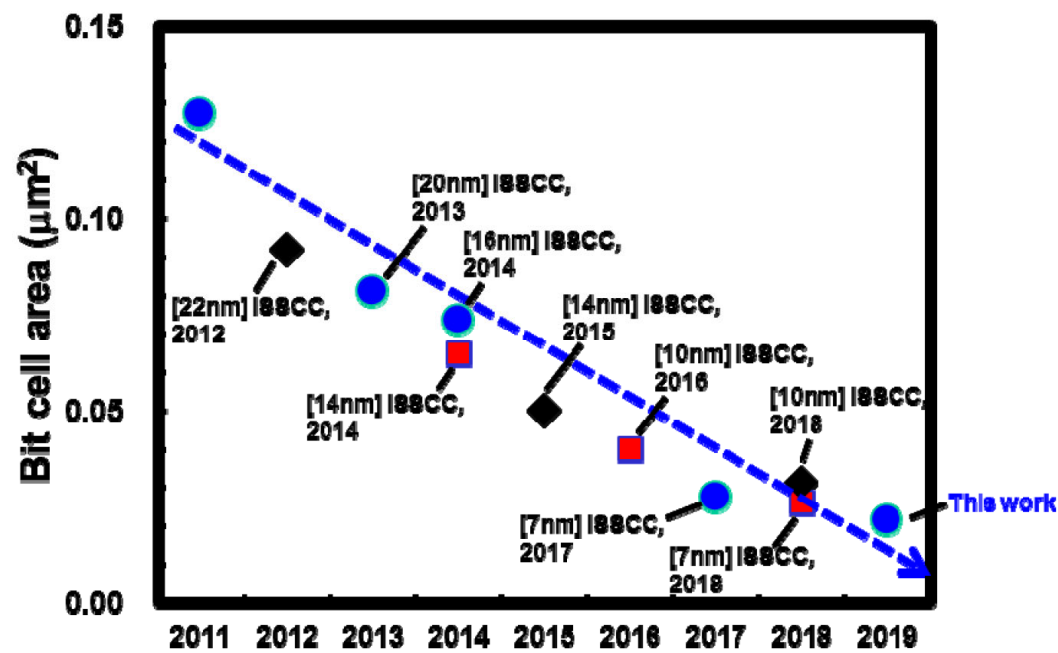
- TSMC at IEDM'19



- Bora's spreadsheet



- TSMC at ISSCC'20





SRAM Topics

A. Basics and trends

B. Static retention margin

C. Static read/write margins

D. Dynamic margins

D. Assist techniques

E. Periphery, redundancy and error correction

F. Scaling options

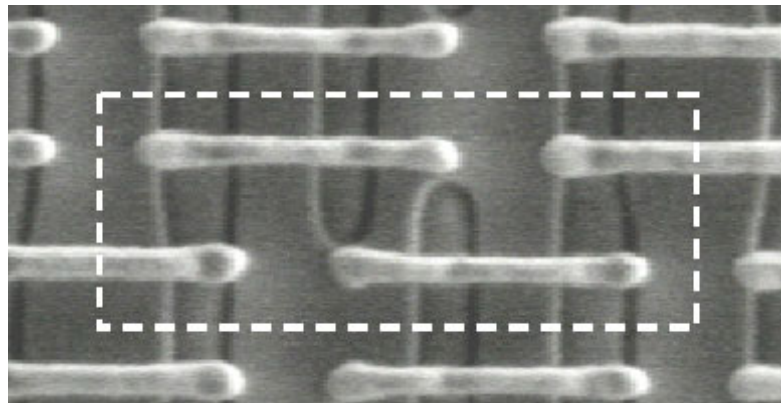
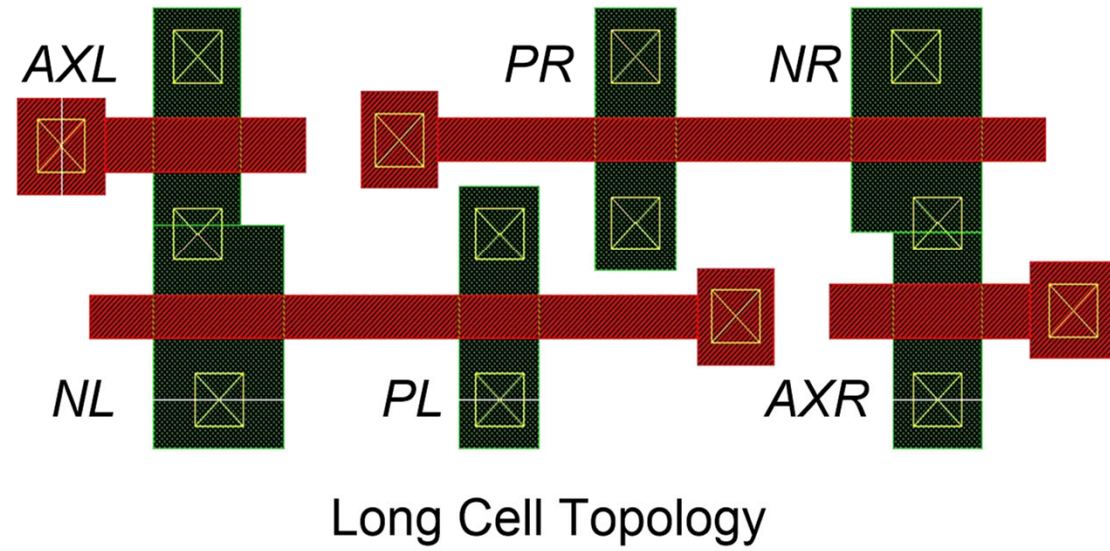
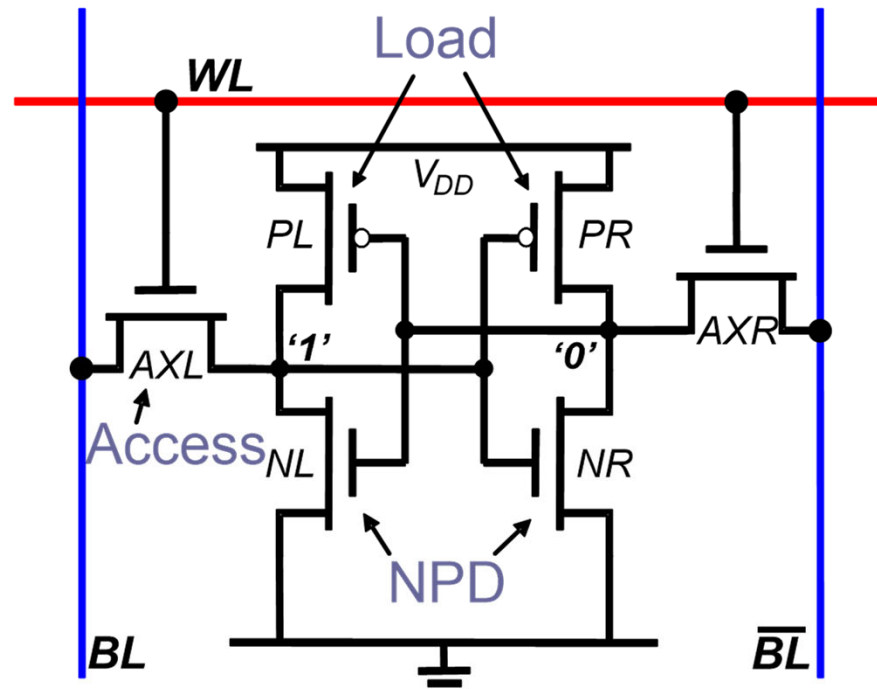




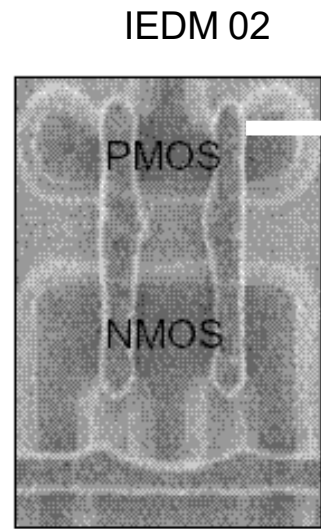
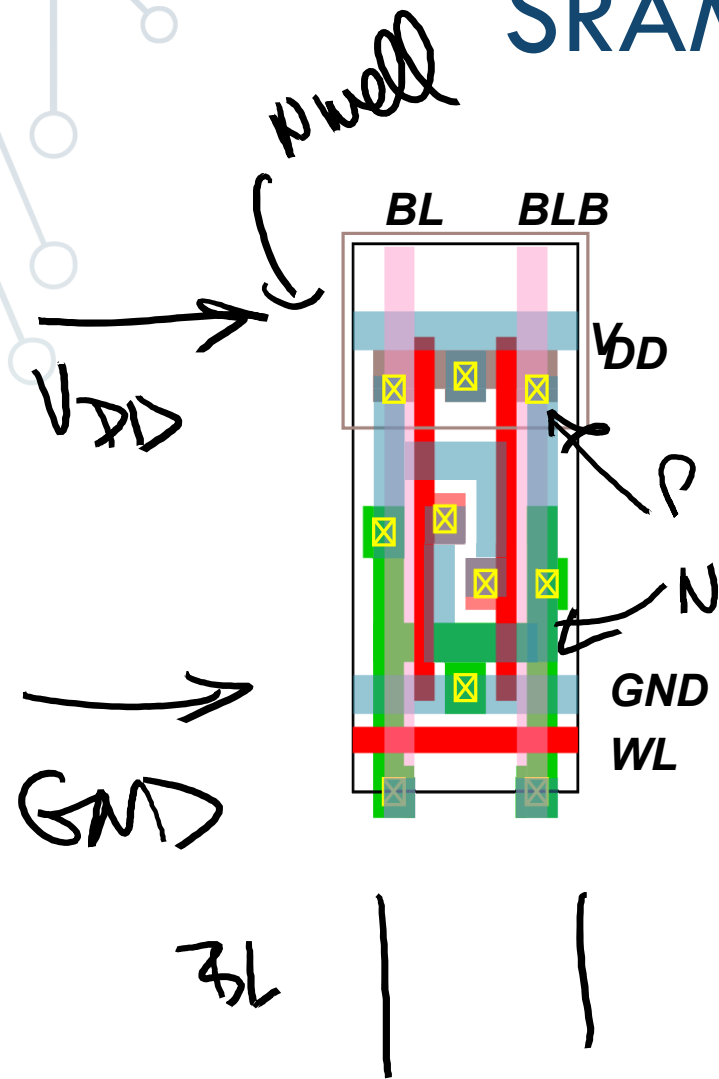
3. Memory

3.A SRAM Basics and Trends

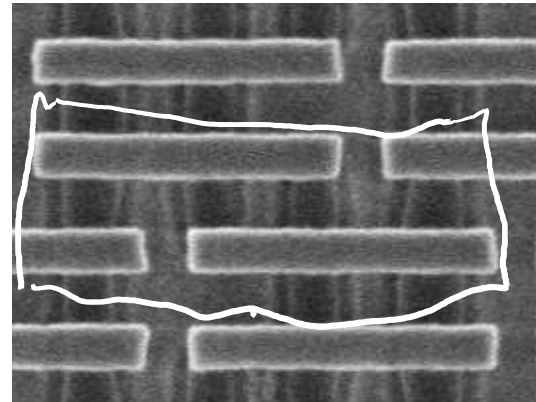
6-T SRAM Cell



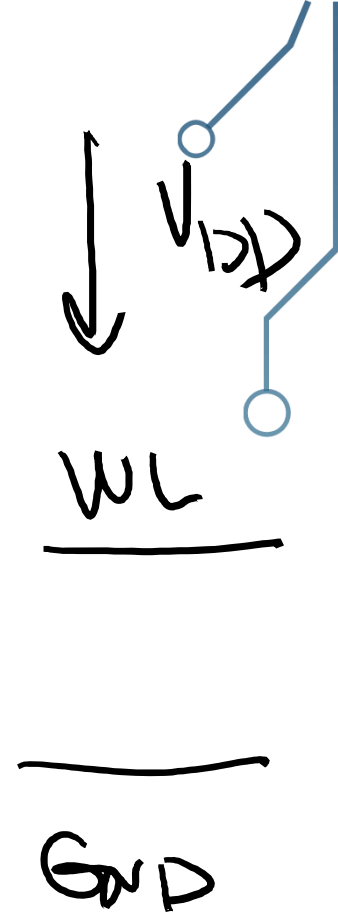
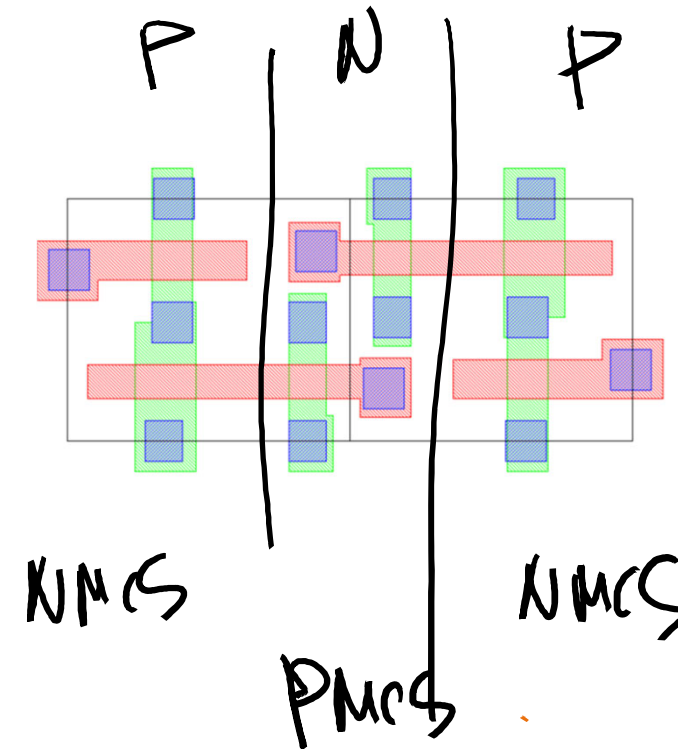
SRAM Cell Design Trends



Cell in 90nm
($1\mu\text{m}^2$)



Cell in 32nm
($0.171\mu\text{m}^2$)

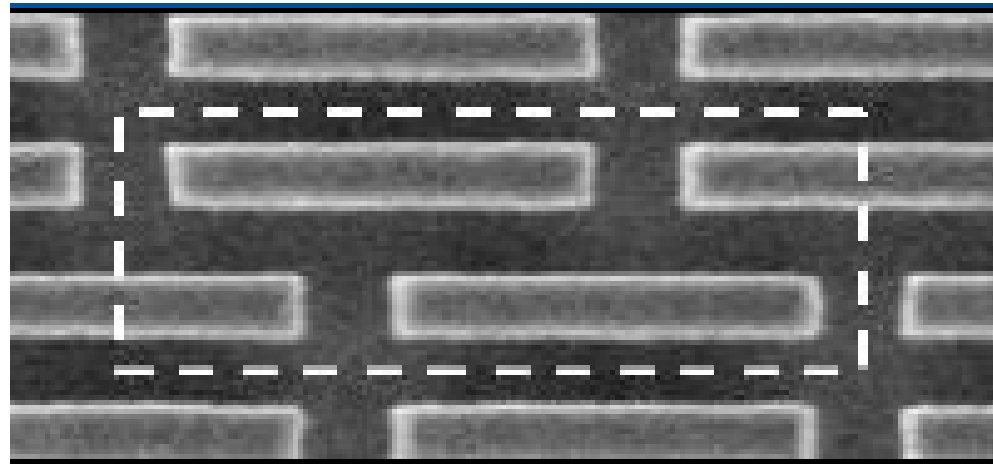


• Key enabling technology:

STI

• Impact:

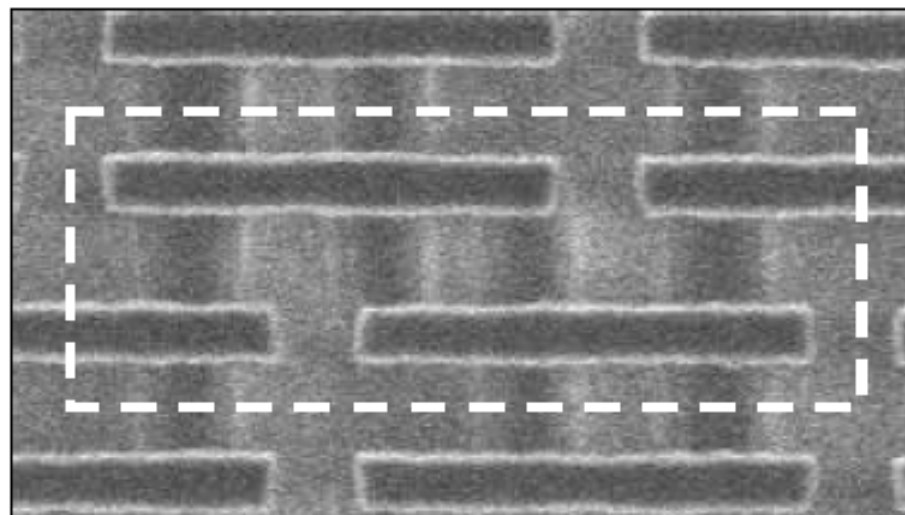
SRAM Cell Trends (22nm)



0.092 μm^2 cell in 22nm from Intel (IDF'09)

A little analysis by using a ruler:

- Aspect ratio 2.9
- Height $\sim 178\text{nm}$, Width $\sim 518\text{nm}$
- Gate $\sim 45\text{nm}$ (L_g is smaller)



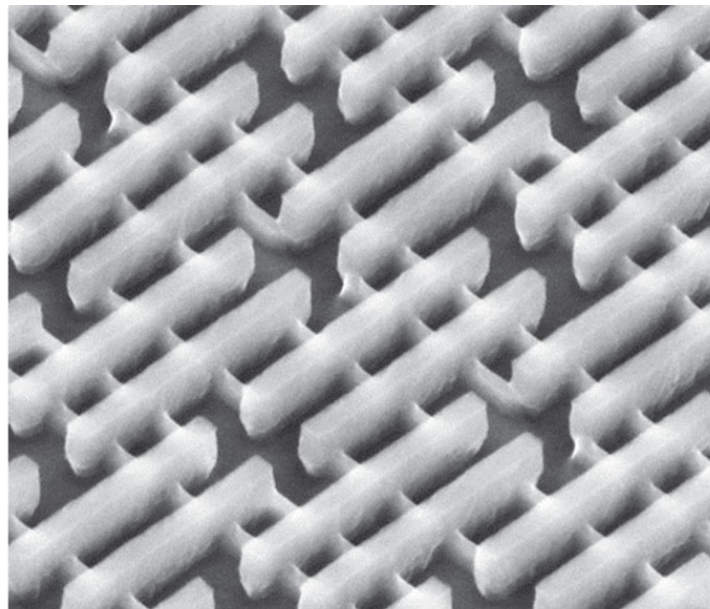
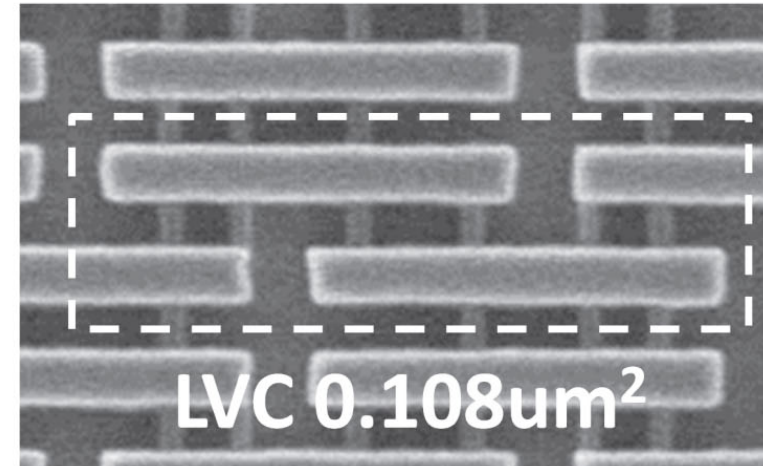
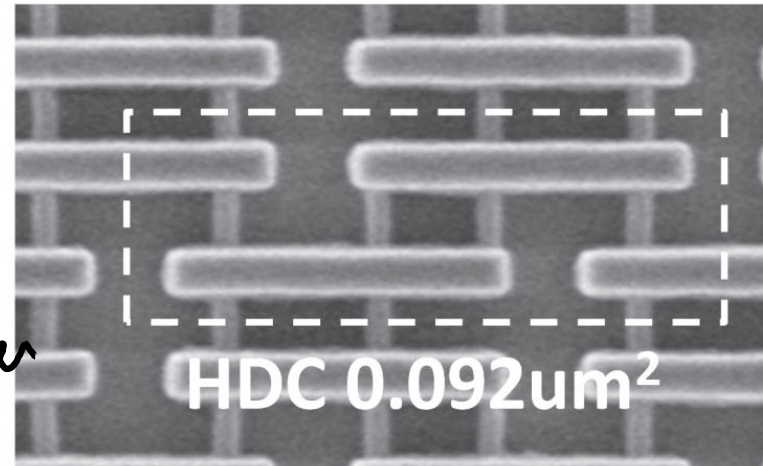
0.346 μm^2 cell in 45nm from Intel (IEDM'07)

22nm SRAM – Discrete Widths

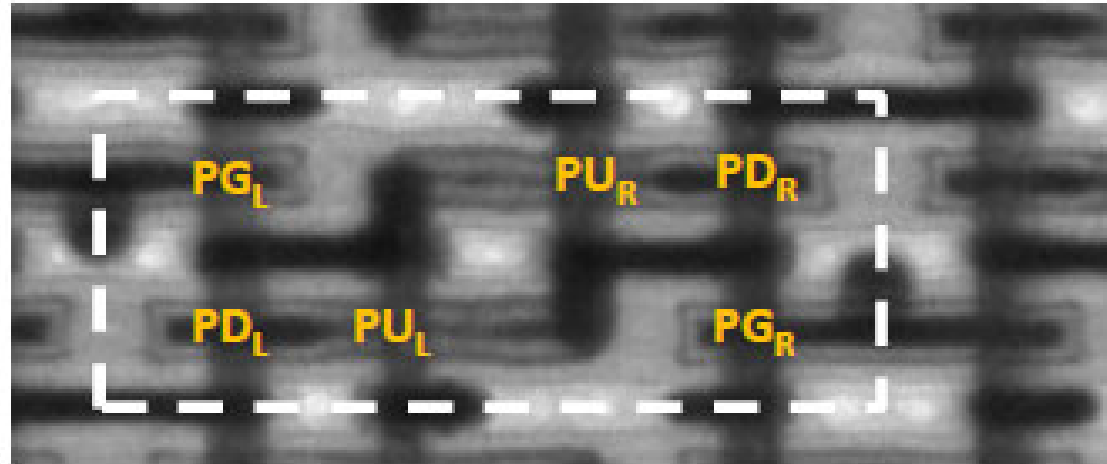
- FinFET cell design



*2ct
in production*



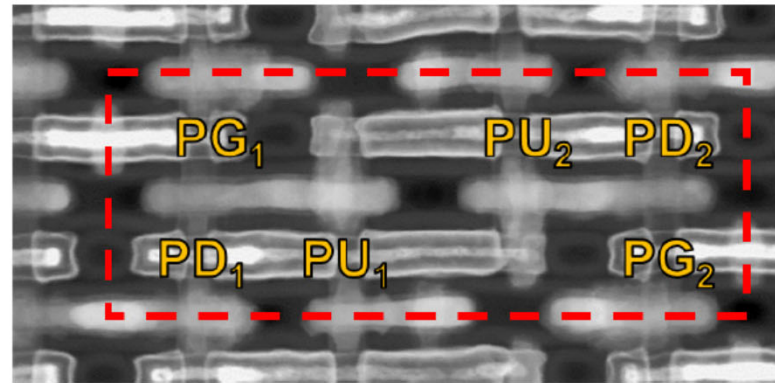
14nm SRAM



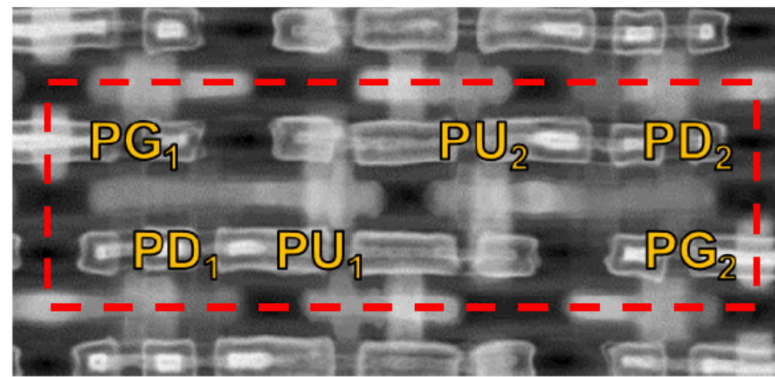
- Aspect ratio ~ 2.5
- Cell area = $0.05\mu\text{m}^2$
 - Height = 140nm (2 gate p)
 - Width = 350nm
 - $L_g \sim 32\text{nm}$

10nm SRAM

HDC
0.0312 μm^2



LVC
0.0367 μm^2



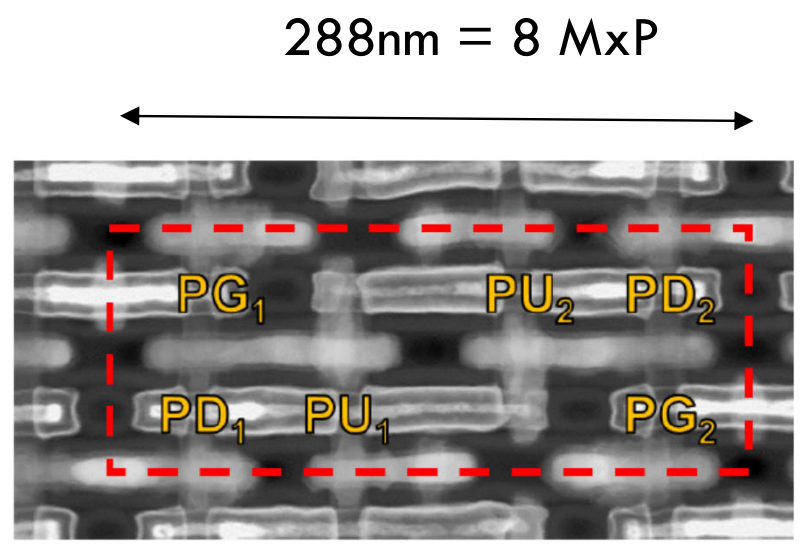
not in production.

- HDC 1:1:1
- LVC 1:1:2

Guo, ISSCC'18

10nm SRAM + Ruler

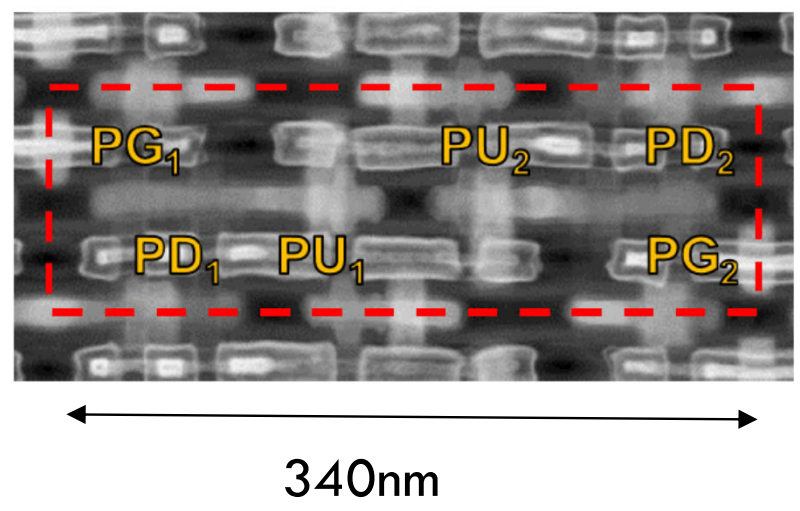
HDC
0.0312 μm^2



2CPP = 108nm

Lg ~ 20nm

LVC
0.0367 μm^2



Next Lecture

- SRAM read and write