EE241B : Advanced Digital Circuits
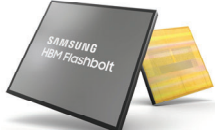
Lecture 13 – SRAM

Borivoje Nikolić

March 4, 2020, EE Times

HBM Flourishes, But HMC Lives. While high bandwidth memory (HBM) is flourishing, hybrid memory cube (HMC) is finding life in applications that didn't exist when it was first conceived.

Announcements

- Assignment 2 due on Friday
  - Quiz 2 on Tuesday, March 10
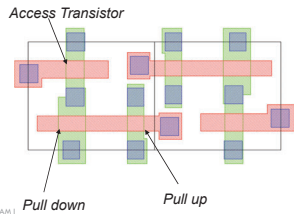- Please send me links to your project web pages
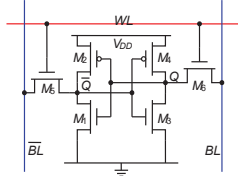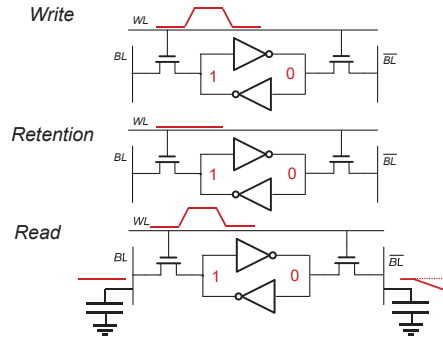

Outline

- Module 4
  - SRAM margins

---

4. Memory
   4.B SRAM Static Retention Margin

SRAM Cell/Array

- Hold (retention) stability
- Read stability
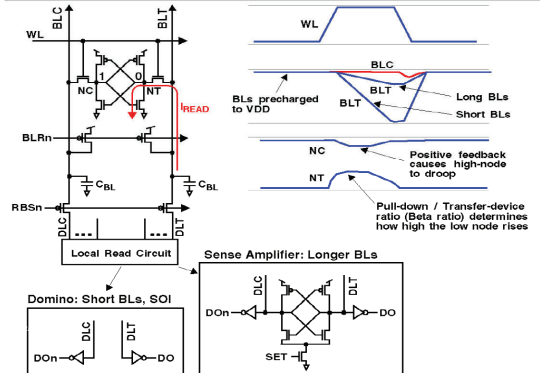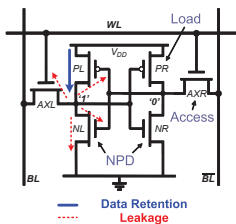- Write stability
- Read access time

Access Transistor

Pull down   Pull up

SRAM Operation

Write

Retention

Read

6T-SRAM Array Basics – Write Operation

BLT discharged to GND by Write Driver

High-node discharged through series stacked NFET devices. NFET effective device strength must overcome cell pull-up.

"Weak" 1 written through source-follower NFET x-fer device
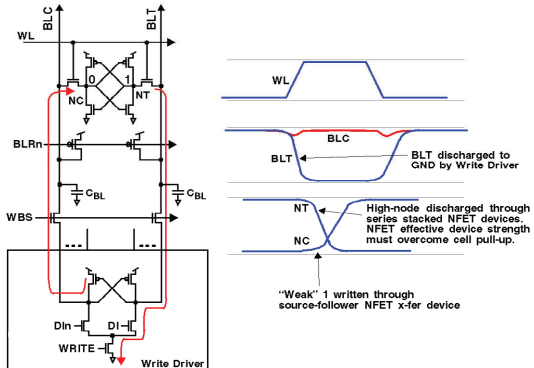
6T-SRAM Array Basics – Read Operation

BLs precharged to VDD

Long BLs
Short BLs

Positive feedback causes high-node to droop

Pull-down / Transfer-device ratio (Beta ratio) determines how high the low node rises

Local Read Circuit

Sense Amplifier: Longer BLs

Domino: Short BLs, SOI

SRAM Design – Hold (Retention) Stability

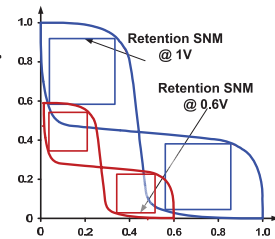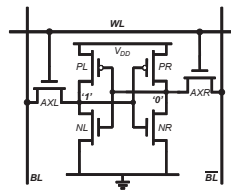
- Data Retention
- Leakage

Static Noise Margin (SNM)

> Scaling trend:
>> Increased gate leakage + degraded I_{ON}/I_{OFF} ratio
>> Lower V_{DD} during standby
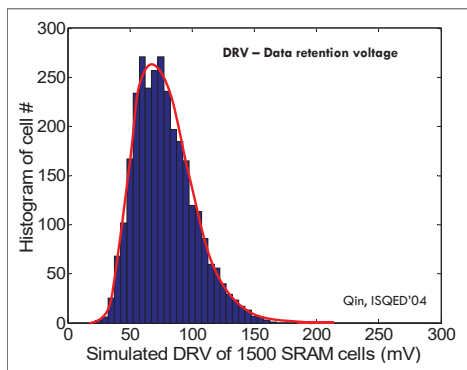> PMOS load devices must compensate for leakage

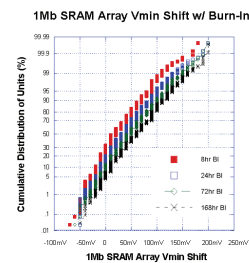## Retention Stability

- Would like to reduce supply in standby

Retention SNM @ 1V

Retention SNM @ 0.6V

Monte-Carlo Simulation of DRV Distribution

DRV – Data retention voltage

Qin, ISQED'04

Vmin Distribution

- Aggregate minimum operating voltage
- Digital test under supply sweep

1Mb SRAM Array Vmin Shift w/ Burn-In

1Mb SRAM Array Vmin Shift

M Ball, IEDM'06

4.C Static Read/Write Margins

Read Stability – Static Noise Margin (SNM)

Read SNM

90nm simulation
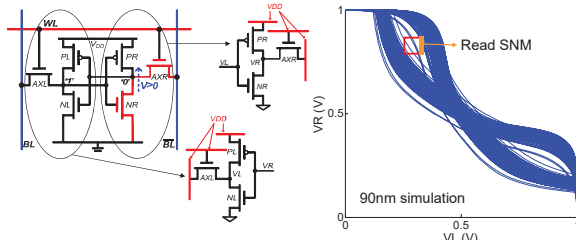
- Read SNM is the contention between the two sides of the cell under read stress.
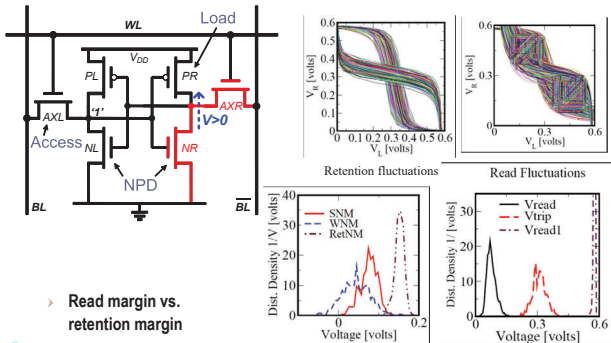
$$\Delta V_{Th} \propto \frac{1}{C_{ox}\sqrt{WL}}$$

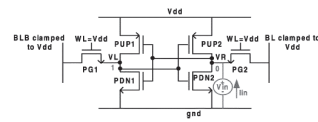Due to RDF

E. Seevinck, JSSC 1987

Read SNM - Measurements

Retention fluctuations

Read Fluctuations

SNM
WNM
RetNM

Vread
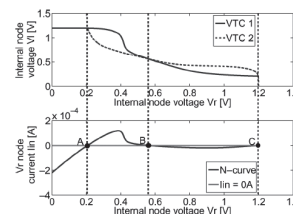Vtrip
Vread1

> Read margin vs. retention margin

Bhavnagarwala, IEDM'05

Read Stability – N-Curve

- A, B, and C correspond to the two stable points A and C and the meta-stable point B of the SNM curve

- When points A and B coincide, the cell is at the edge of stability and a destructive read can occur
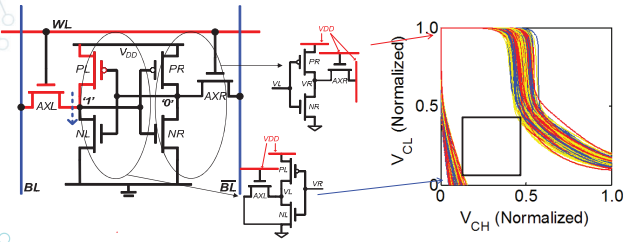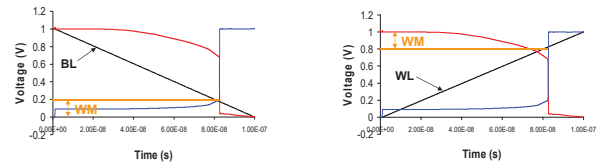
Grossar, JSSC'06

Write Stability – Write Noise Margin (WNM)

- Writeability is becoming harder with scaling
- Optimizing read stability and writeability at the same time is difficult

A. Bhavnagarwala, *IEDM* 2005
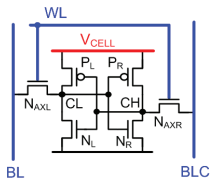

Writeability – BL/WL Write Margins

- Highest BL voltage under which write is possible when BLC is kept precharged

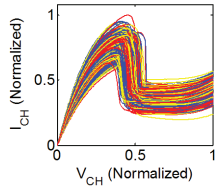- Difference between VDD and lowest WL voltage under which write is possible
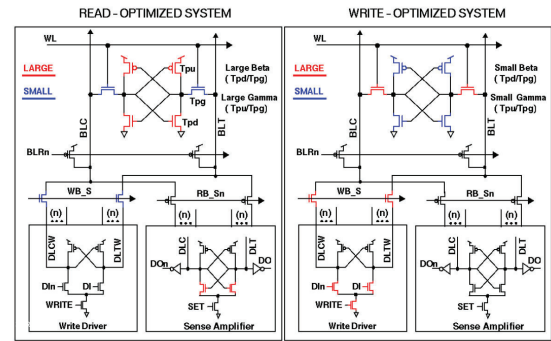

Write Stability – Write Current (N-Curve)

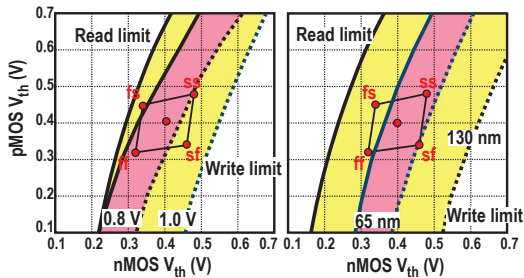- Minimum current into the storage node

C. Wann et al, *IEEE VLSI-TSA* 2005

The Conflict Between Read and Write

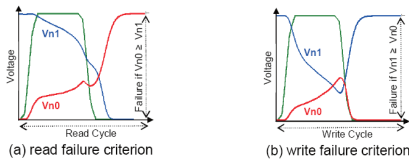## V_{Th} Window

- Assuming global spread

Yamaoka, ISSCC'05

4.D Dynamic Margins

6-T SRAM Static/Dynamic Stability

(a) read failure criterion

(b) write failure criterion
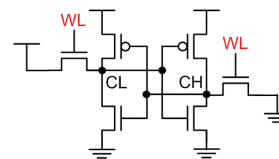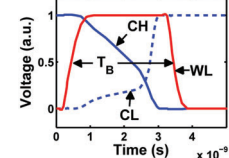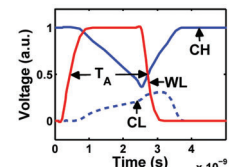
- Read Margin
  - SNM: pessimistic
- Write Margin
  - WNM: optimistic
- Introduction to dynamic margins
  - Three failure modes: read stability, writeability and read access time

---

Dynamic Write Stability

- $T_A < T_{write} < T_B$
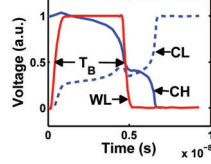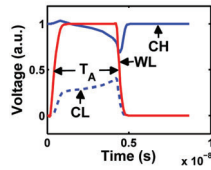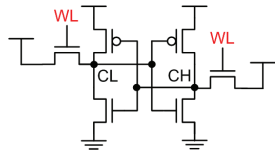- T_{write} = dynamic write stability
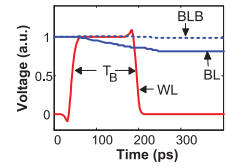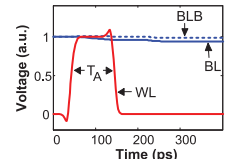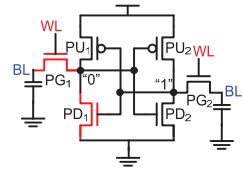- Static margins are optimistic

Khalil, TVLSI'08

Dynamic Read Stability

- $T_A < T_{read} < T_B$
- T_{read} = dynamic read stability
- Static margins are pessimistic
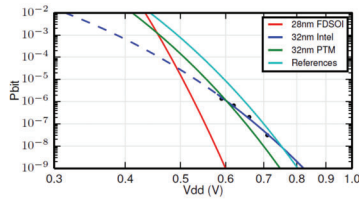
Khalil, TVLSI '08

Dynamic Read Access

- $T_A < T_{access} < T_B$
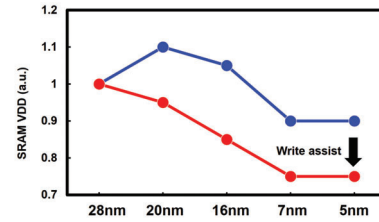- PD_1 and PG_1 are critical

Khalil, TVLSI '08

SRAM Overall Vmin

- Both read and write
- Some contradicting data

SRAM Vmin Scaling Trend

➢ SRAM voltage often higher than logic

- J. Chang, ISSCC'20

Next Lecture

- Peripheral circuits
- SRAM assist techniques
- Alternatives to 6T SRAM