Announcements
* Assignment 2 due on Friday
* Quiz 2 on Tuesday, March 10
* Please send me links to your project web pages

March 4, 2020, EE Times
HBM Flourishes, But HMC Lives. While high-bandwidth memory (HBM) is flourishing, hybrid memory cube (HMC) is finding life in applications that didn’t exist when it was first conceived.

Outline
* Module 4
  * SRAM margins

SRAM Cell/Array
* Hold (retention) stability
* Read stability
* Write stability
* Read access time

SRAM Operation

4. Memory
4B SRAM Static Retention Margin

6T-SRAM Array Basics – Write Operation

6T-SRAM Array Basics – Read Operation

H. Pilo, IEDM 2006
SRAM Design – Hold (Retention) Stability

- Scaling trend:
  - Increased gate leakage + degraded $I_{ON}/I_{OFF}$ ratio
  - Lower $V_{DD}$ during standby
  - PMOS load devices must compensate for leakage

Retention Stability

- Would like to reduce supply in standby

Monte-Carlo Simulation of DRV Distribution

- DRV – Data retention voltage
- Histogram of cell #
- Simulated DRV of 1500 SRAM cells (mV)
- DRV – Data retention voltage

Vmin Distribution

- Aggregate minimum operating voltage
- Digital test under supply sweep

Read Stability – Static Noise Margin (SNM)

- Read SNM is the contention between the two sides of the cell under read stress.
- $\Delta V_{SNM} \propto \frac{1}{C_{\mu \sqrt{WL}}}$
- Due to RDF

4.C Static Read/Write Margins

Read SNM - Measurements

- Read margin vs. retention margin

Read Stability – N-Curve

- A, B, and C correspond to the two stable points A and C and the meta-stable point B of the SNM curve
- When points A and B coincide, the cell is at the edge of stability and a destructive read can occur
Writeability is becoming harder with scaling  
Optimizing read stability and writeability at the same time is difficult

Write Stability – Write Noise Margin (WNM)

- Writeability is becoming harder with scaling  
- Optimizing read stability and writeability at the same time is difficult

Writeability – BL/WL Write Margins

- Highest BL voltage under which write is possible when BLC is kept precharged
- Difference between VDD and lowest WL voltage under which write is possible

Write Stability – Write Current (N-Curve)

- Minimum current into the storage node

V_T Window

- Assuming global spread

4D Dynamic Margins

6-T SRAM Static/Dynamic Stability

- Read Margin
  - SRAM: pessimistic
- Write Margin
  - WNM: optimistic
- Introduction to dynamic margins
- Three failure modes: read stability, writeability and read access time

Dynamic Write Stability

- \( T_A < T_{\text{write}} < T_B \)
- \( T_{\text{write}} = \) dynamic write stability
- Static margins are optimistic

Yamaoka, ISSCC'05

Xahil, TVLSI'08
**Dynamic Read Stability**

- $T_A < T_{\text{read}} < T_B$
- $T_{\text{read}} = \text{dynamic read stability}$
- Static margins are pessimistic

Khalil, TVLSI '08

---

**Dynamic Read Access**

- $T_A < T_{\text{access}} < T_B$
- $PD_1$ and $PG_1$ are critical

Khalil, TVLSI '08

---

**SRAM Overall Vmin**

- Both read and write
- Some contradicting data

---

**SRAM Vmin Scaling Trend**

- SRAM voltage often higher than logic

J. Chang, ISSCC '20

---

**Next Lecture**

- Peripheral circuits
- SRAM assist techniques
- Alternatives to 6T SRAM