# EE241B : Advanced Digital Circuits

## Lecture 14 – SRAM 2

Borivoje Nikolić


**March 4, 2020, AnandTech**

**El Capitan Supercomputer Detailed:** AMD CPUs & GPUs to drive 2 Exaflops of compute.

Back in August, the United States Department of Energy and Cray announced plans for a third United States exascale supercomputer, El Capitan. Scheduled to be installed in Lawrence Livermore National Laboratory (LLNL) in early 2023.

# Announcements

- Quiz 2 on Thursday
- Please send me links to your project web pages
- Assignment 3 due next week
- Project midterm reports due next week

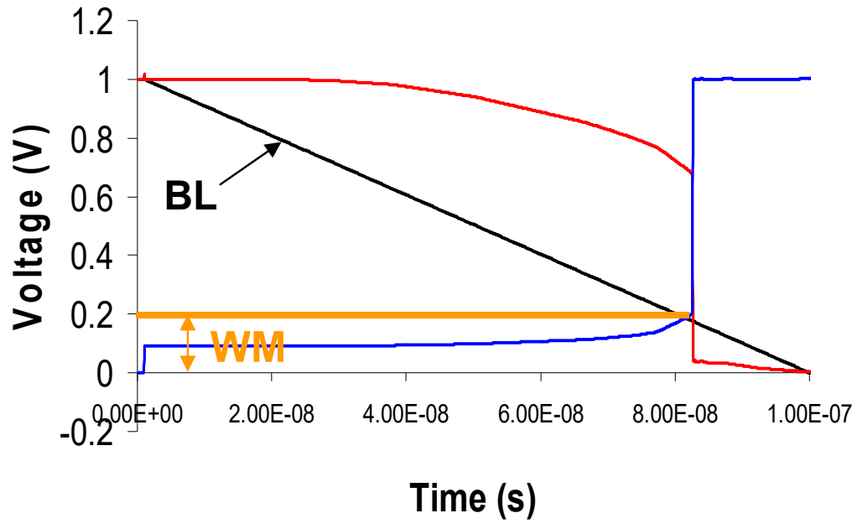
# Midterm report

# Outline

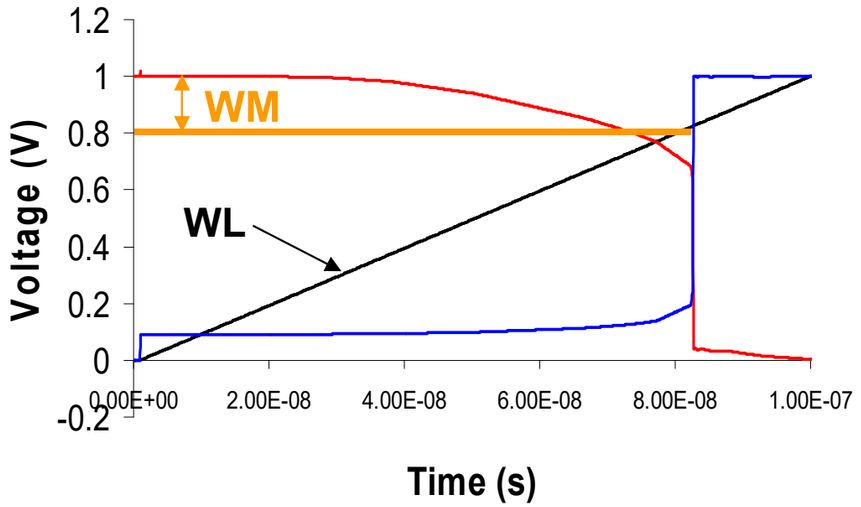
- Module 4
  - SRAM dynamic margins
  - Assist techniques

# 4.C Static Read/Write Margins

# Writeability – BL/WL Write Margins

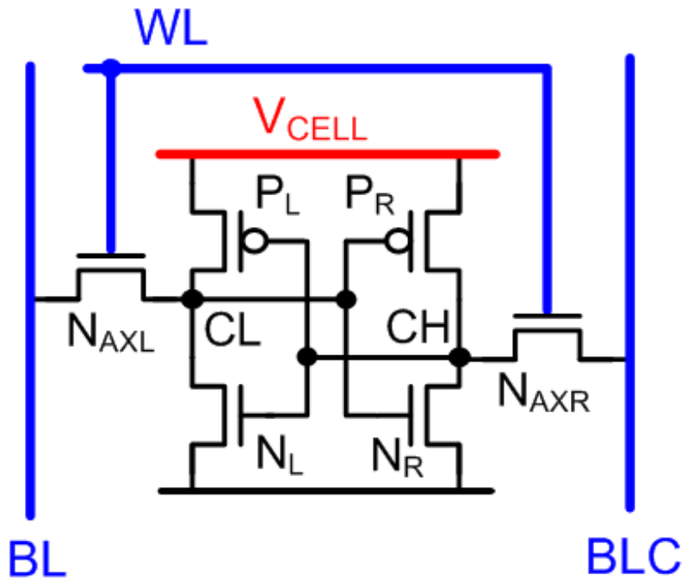



- Highest BL voltage under which write is possible when BLC is kept precharged

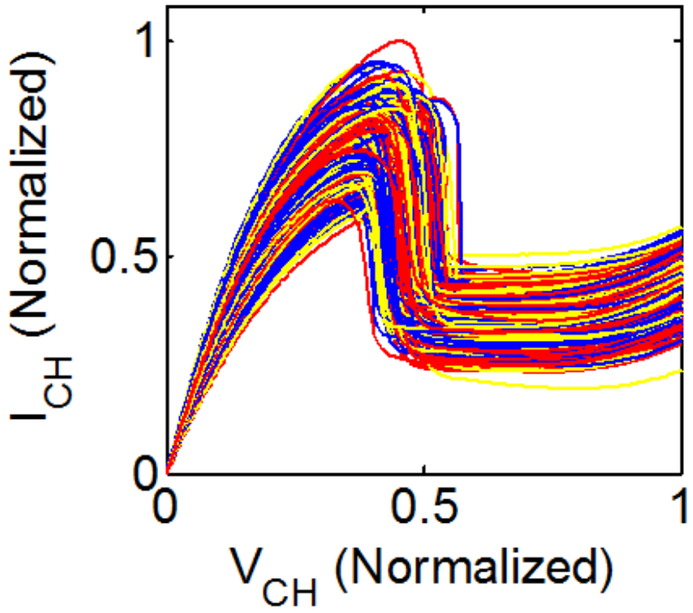



- Difference between VDD and lowest WL voltage under which write is possible

# Write Stability – Write Current (N-Curve)

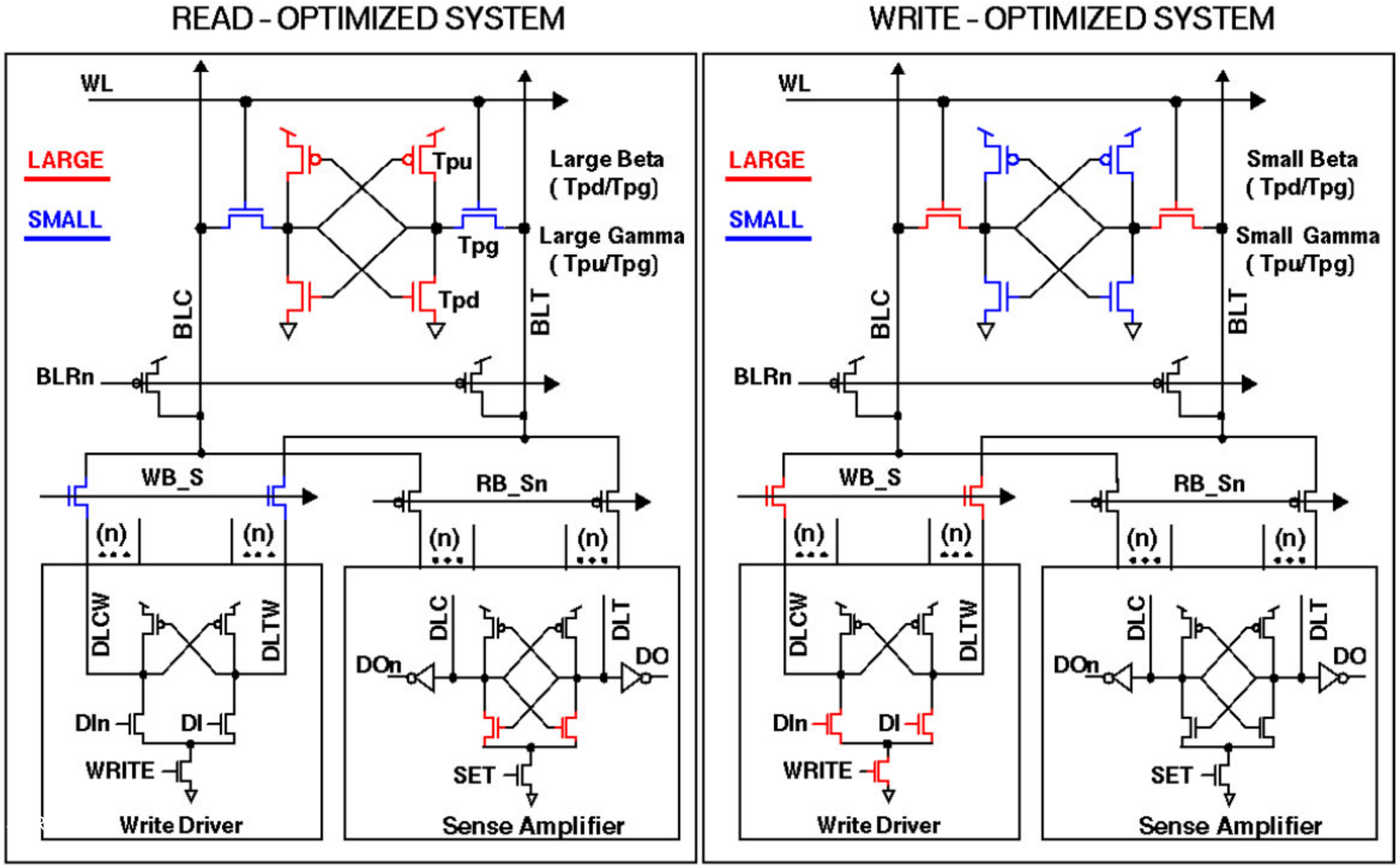



- Minimum current into the storage node



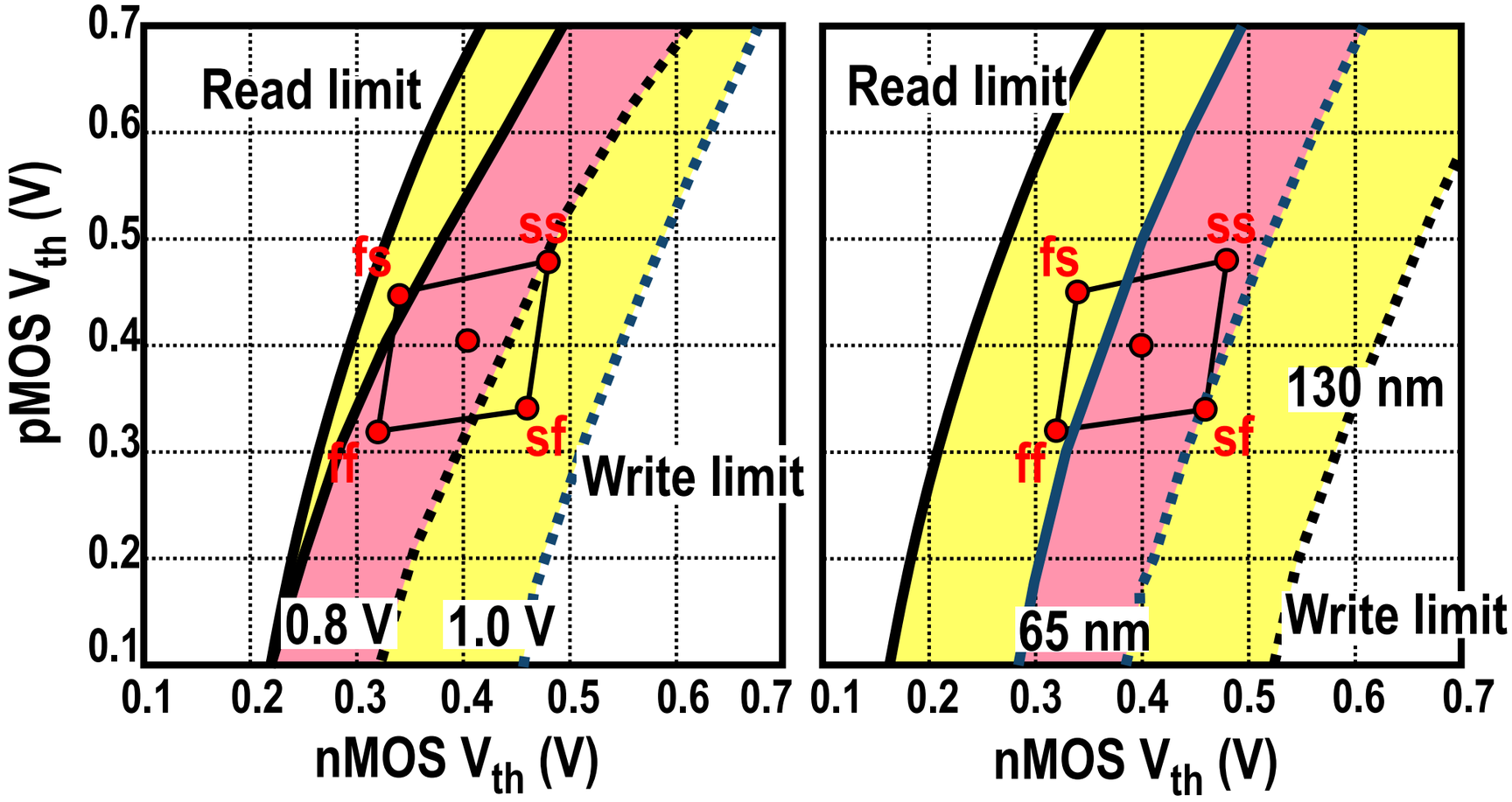

C. Wann et al, *IEEE VLSI-TSA* 2005

# The Conflict Between Read and Write



# $V_{Th}$ Window

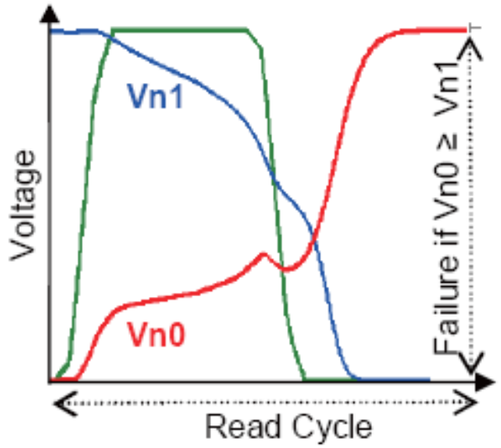
- Assuming global spread



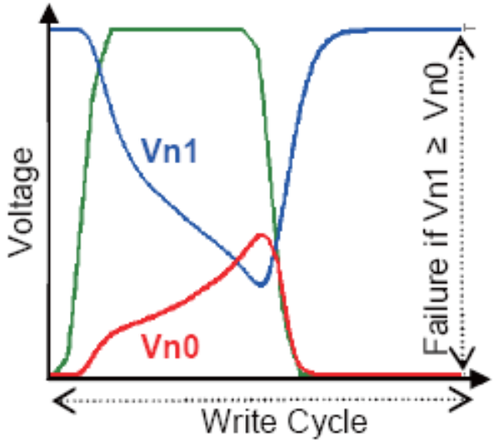

Yamaoka, ISSCC'05

# 4.D Dynamic Margins

# 6-T SRAM Static/Dynamic Stability



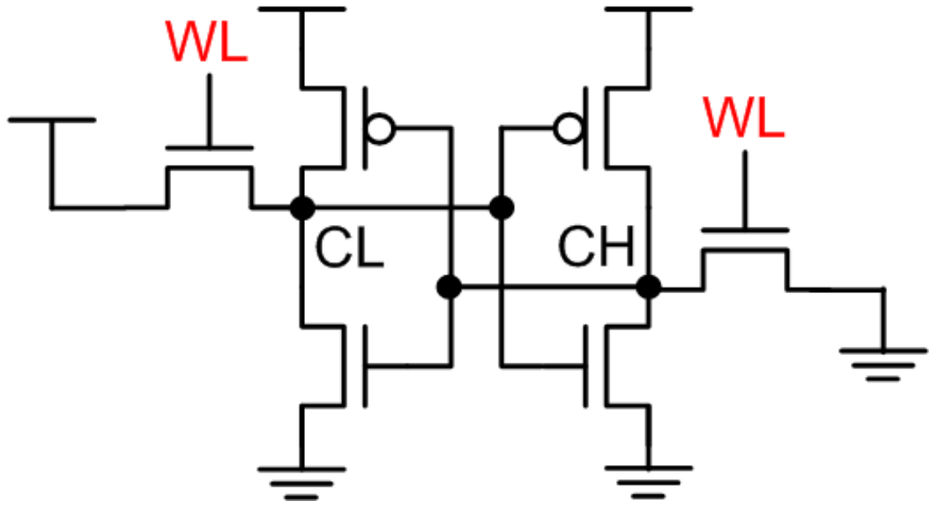
(a) read failure criterion

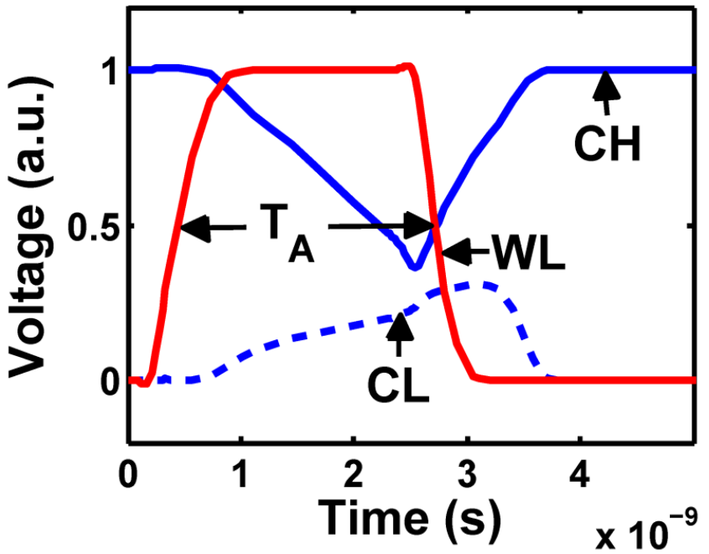


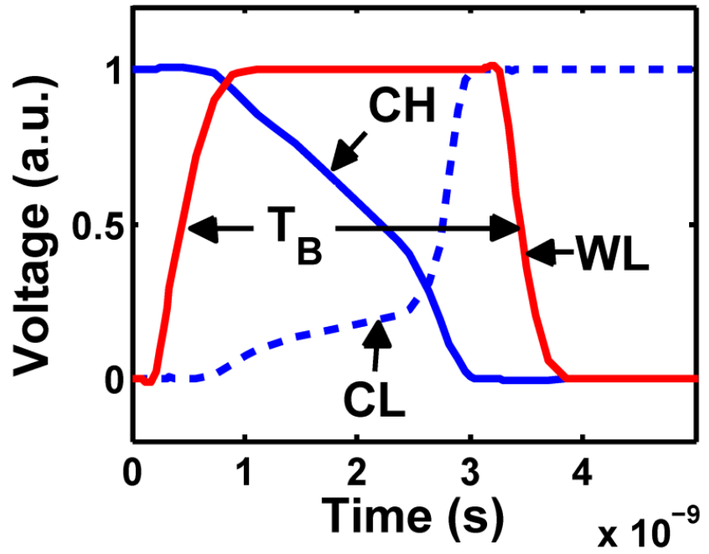
(b) write failure criterion

- Read Margin
  - SNM: pessimistic
- Write Margin
  - WNM: optimistic
- Introduction to dynamic margins
  - Three failure modes: read stability, writeability and read access time

# Dynamic Write Stability



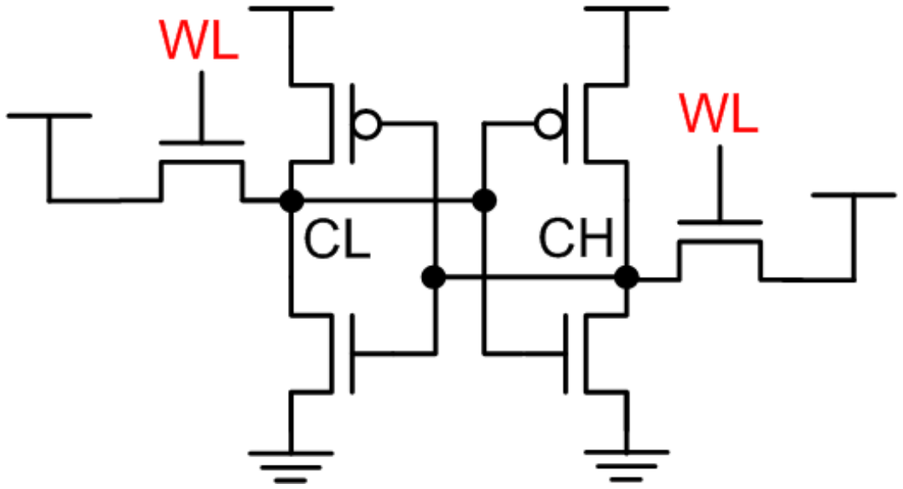



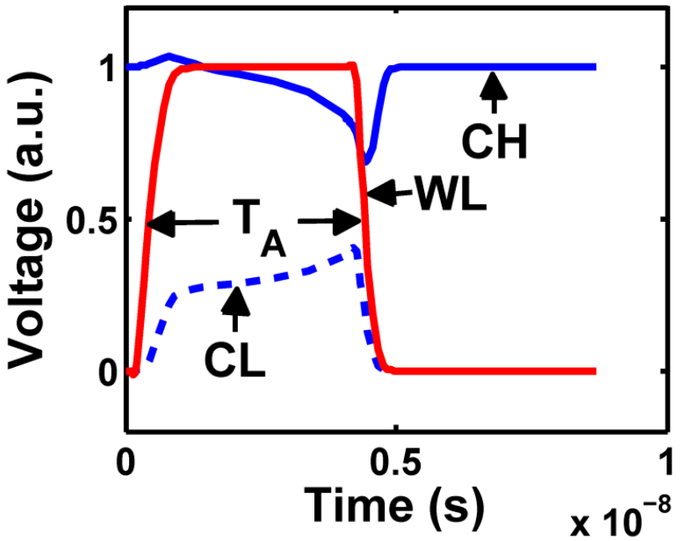



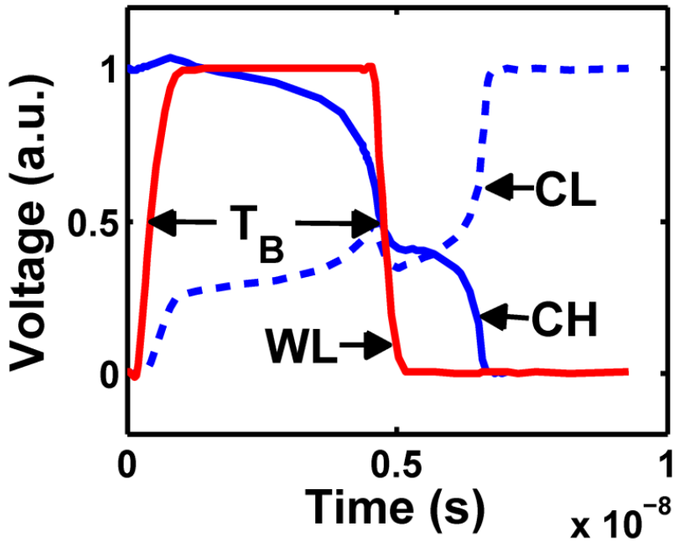

- $T_A < T_{write} < T_B$
- $T_{write}$= dynamic write stability
- Static margins are optimistic

Khalil, TVLSI'08

# Dynamic Read Stability



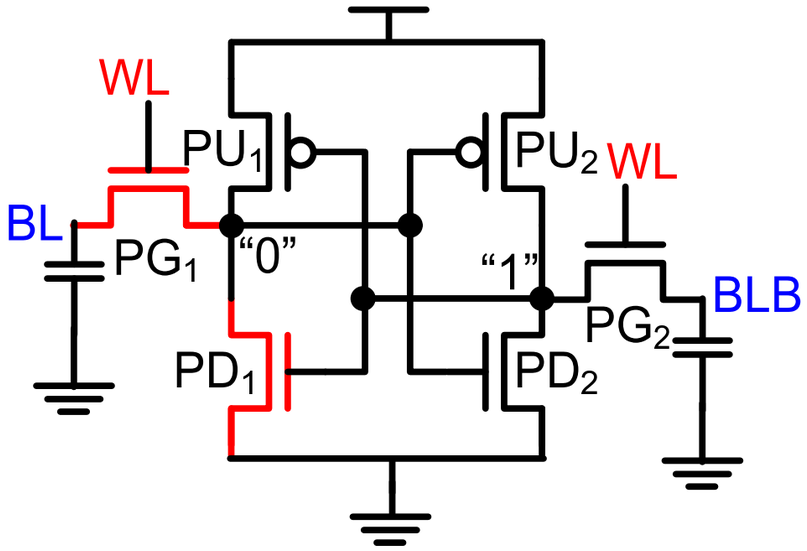



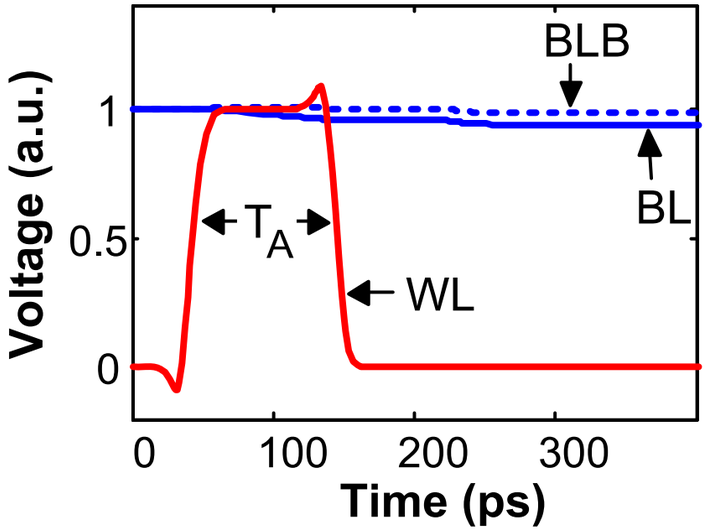



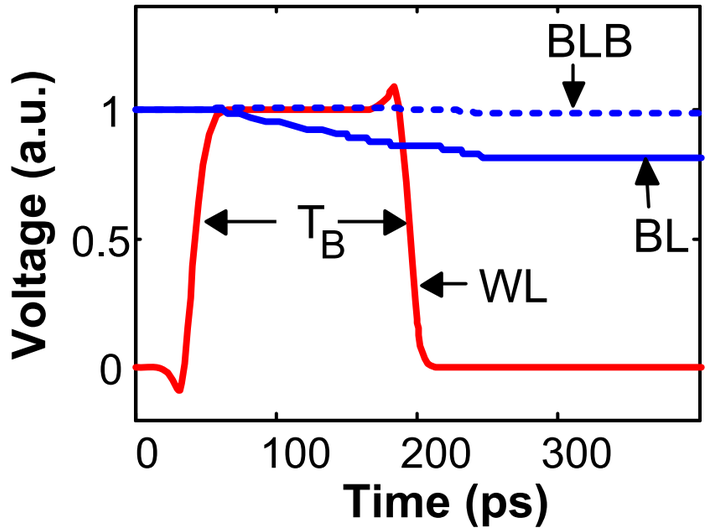

- $T_A < T_{read} < T_B$
- $T_{read}$ = dynamic read stability
- Static margins are pessimistic

Khalil, TVLSI '08

# Dynamic Read Access



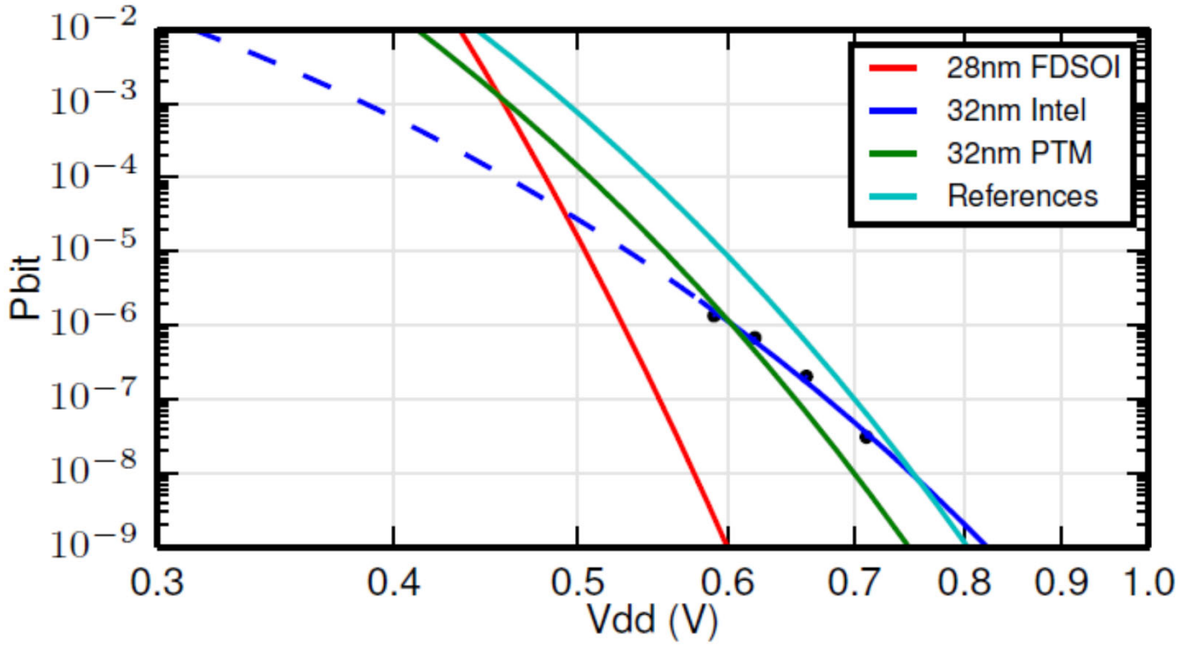




- $T_A < T_{access} < T_B$
- $PD_1$ and $PG_1$ are critical

Khalil, TVLSI '08

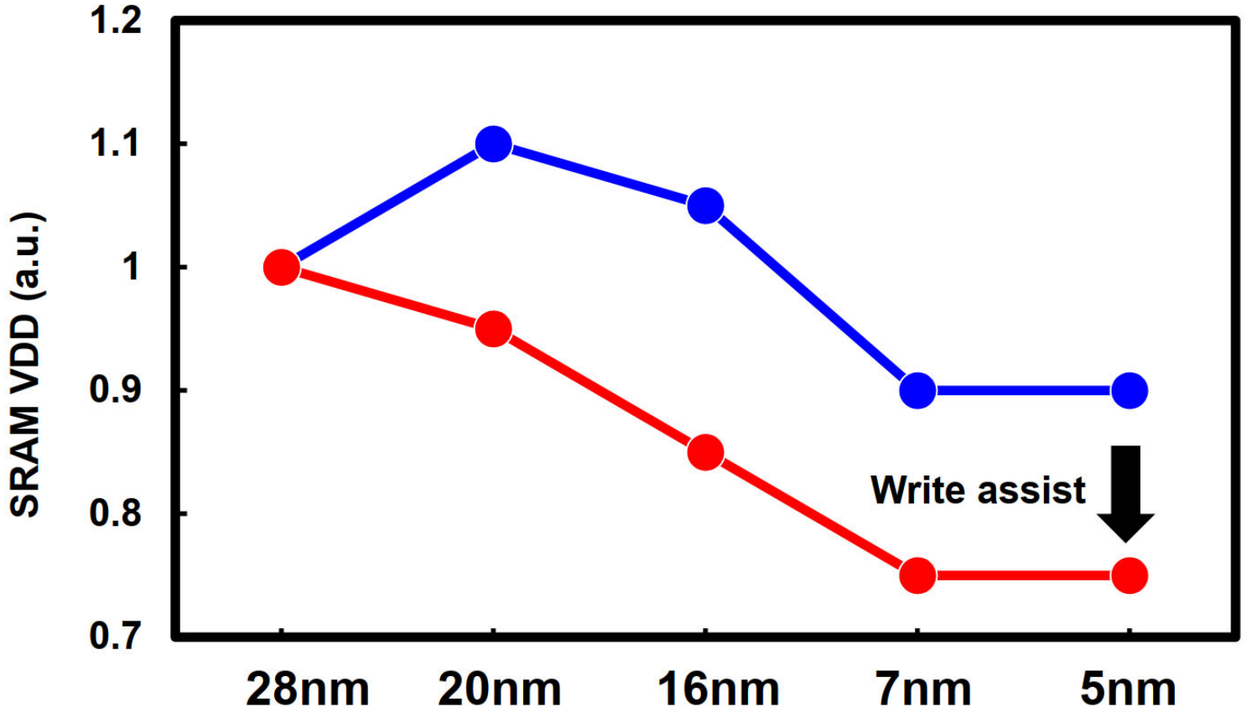
# SRAM Overall Vmin

- Both read and write
- Some contradicting data



# SRAM Vmin Scaling Trend

- SRAM voltage often higher than logic



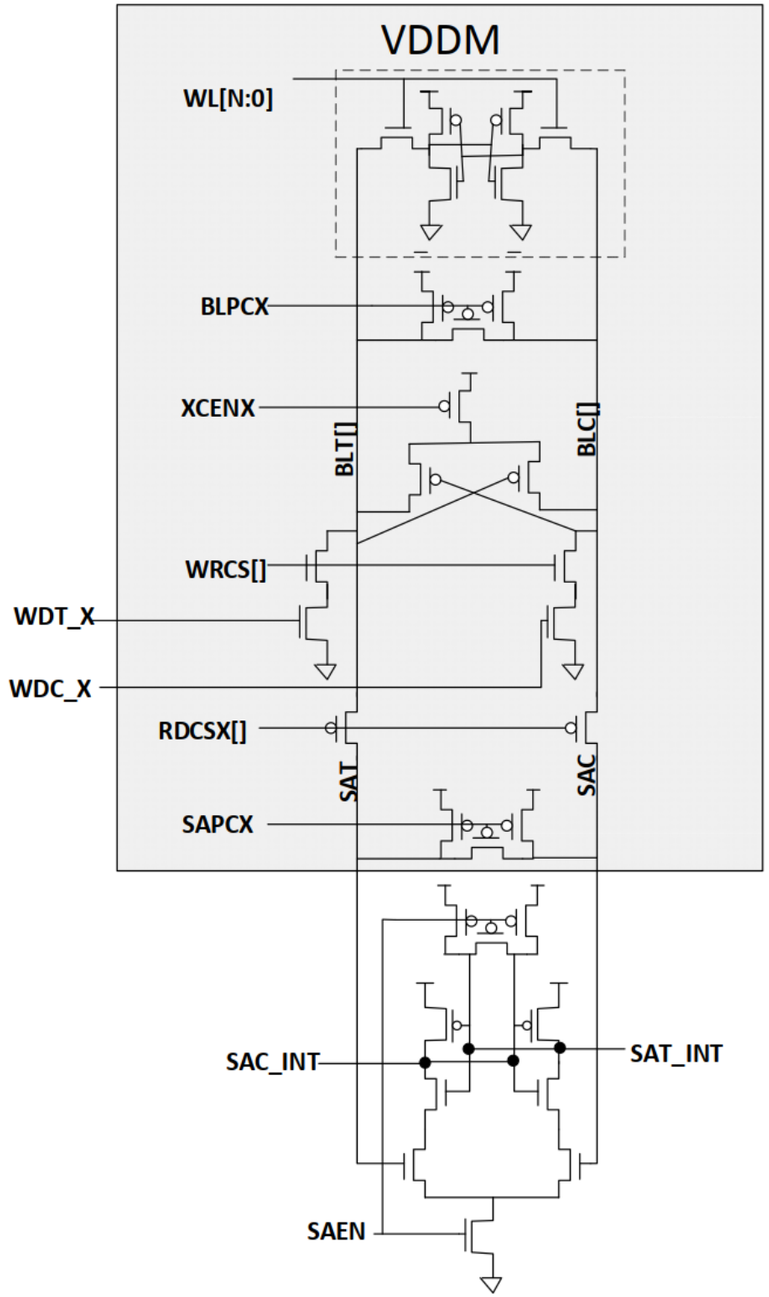

- J. Chang, ISSCC'20

# 4.E SRAM Peripheral Circuits

# Peripheral Circuits in SRAM

- Decoders (and pre-decoders)
- Column circuitry: read, write, multiplex, mask
- Write assist techniques
- Read assist techniques
- Redundancy
- BIST
- ECC

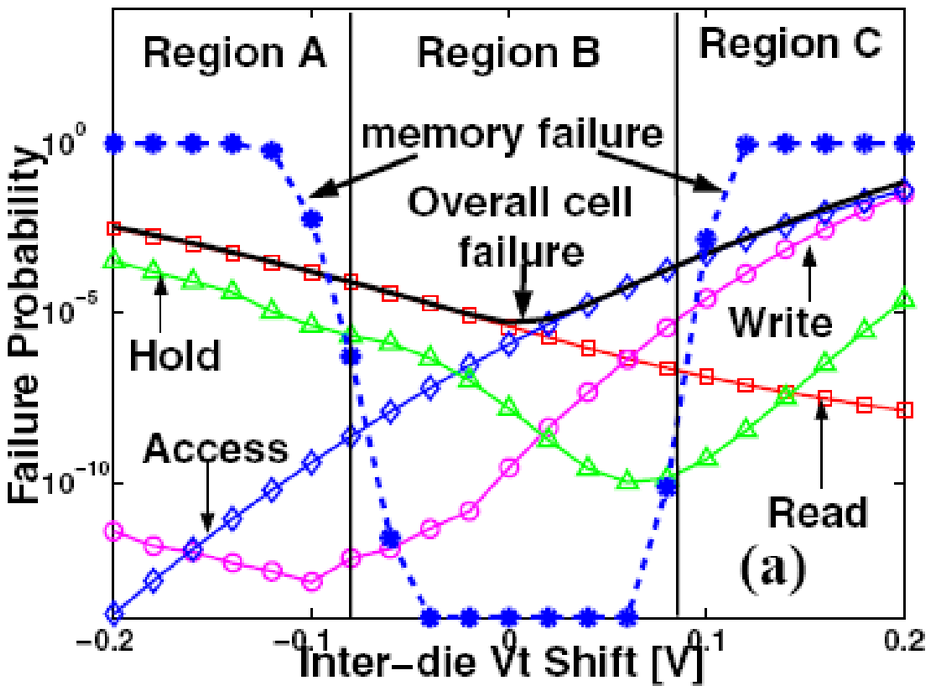
# SRAM Array

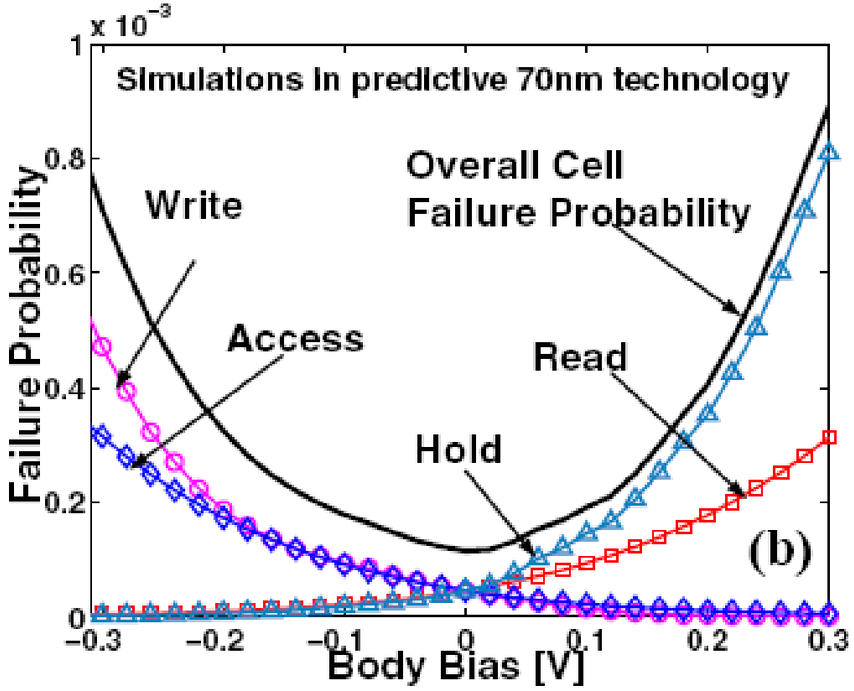



AMD Zen2
ISSCC'20

# Array Adjustments

**Array back bias, to compensate for systematic variations**



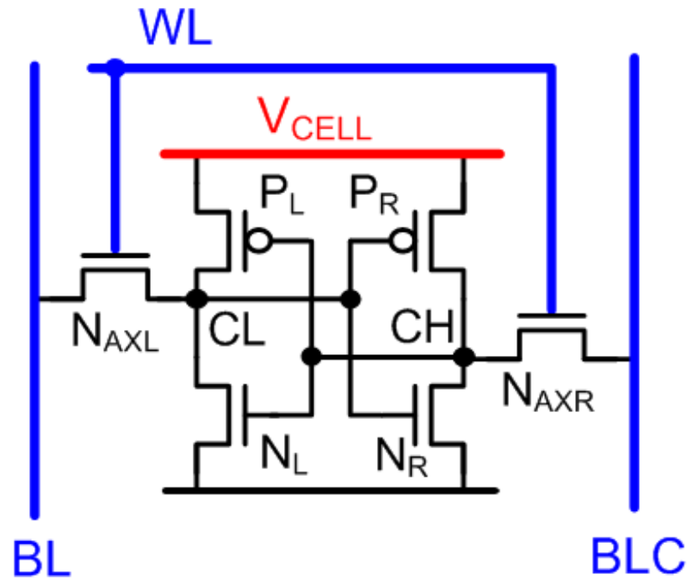

**May be useful in technologies with strong body effect**

S. Mukhopadhyay, *VLSI* 2006

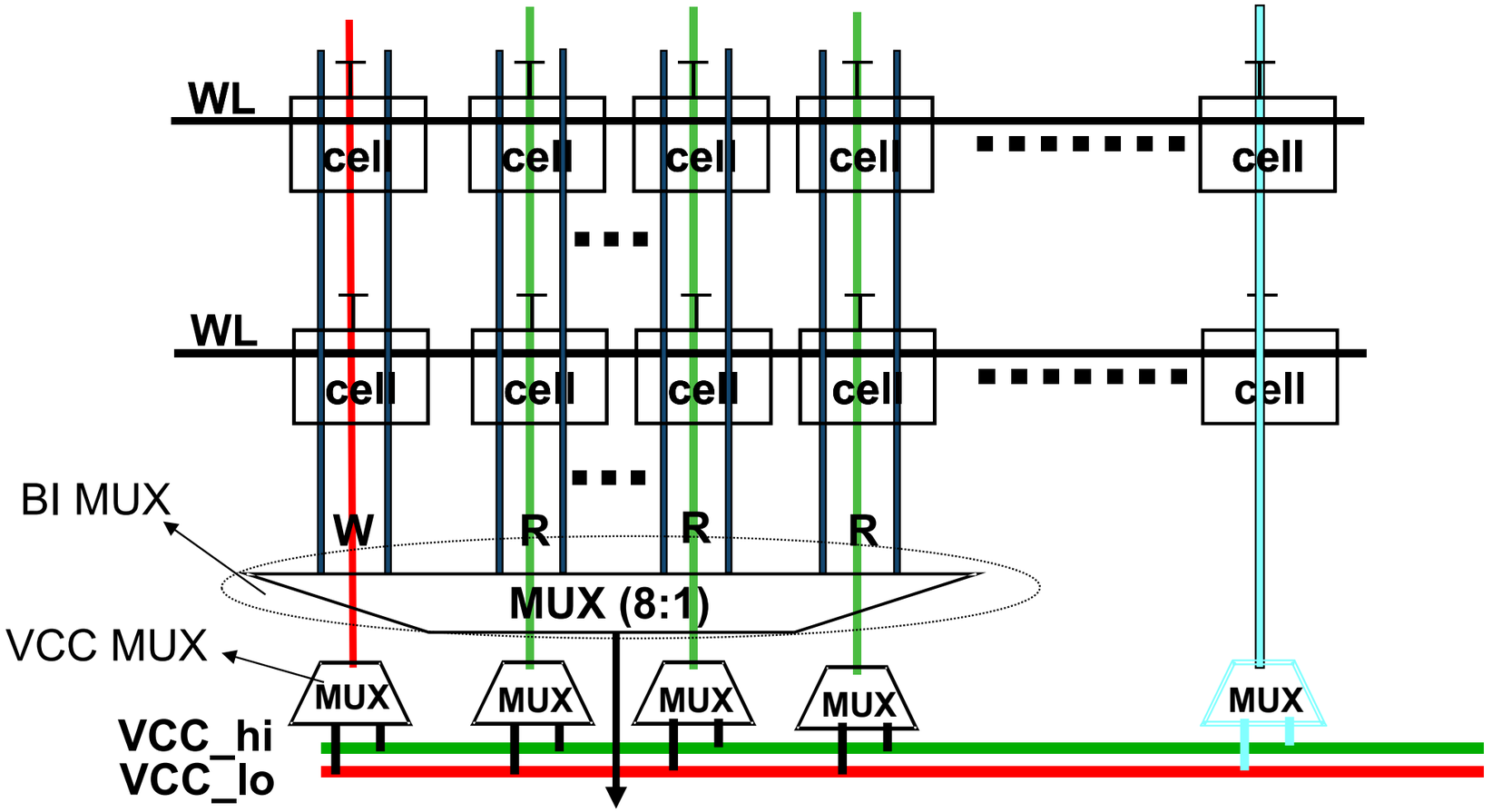
# 4.F SRAM Assist Circuits

# Basic Ideas

- Dynamically change voltages



# Dynamic $V_{DD}$ Implementation

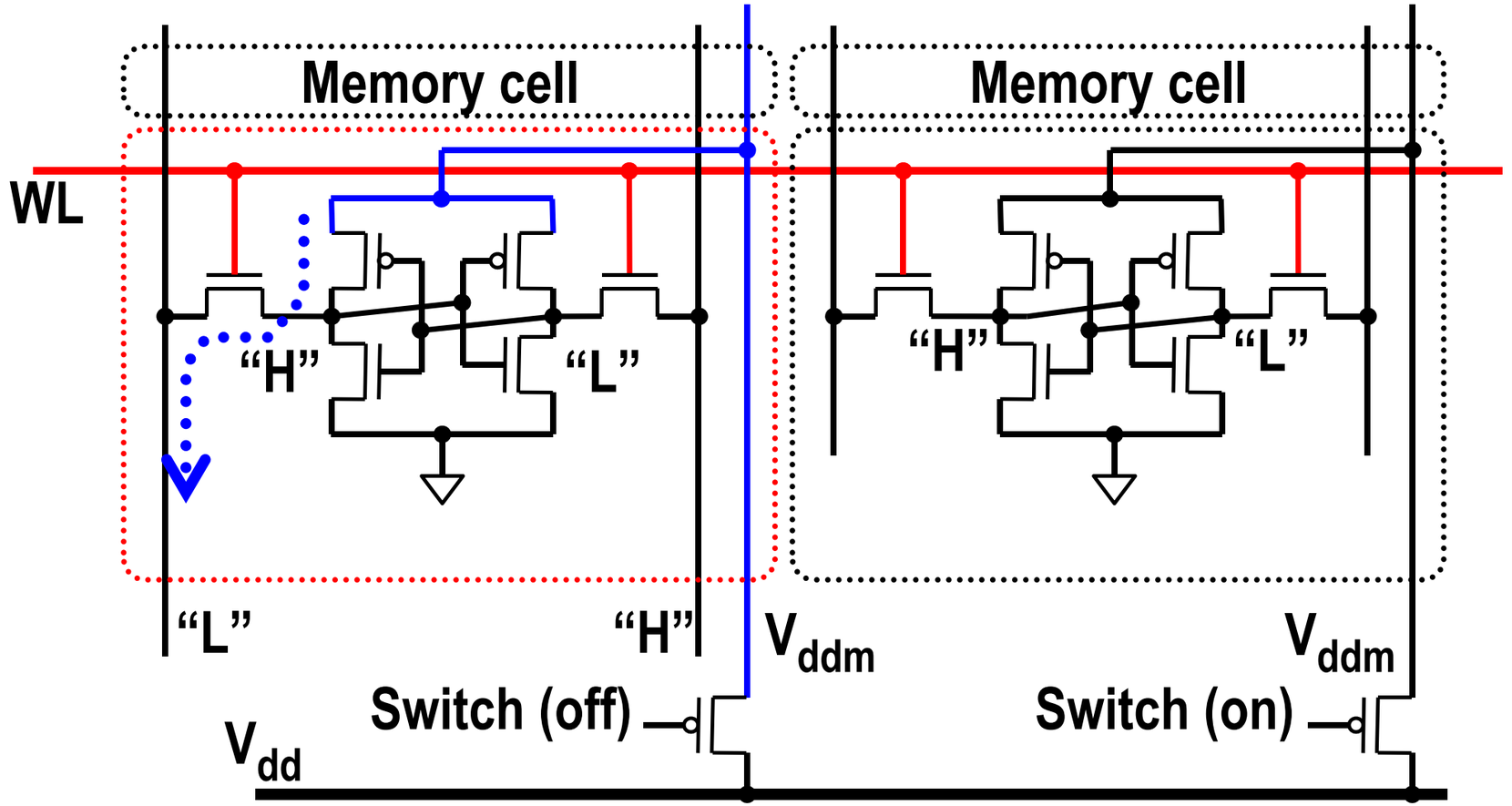



- VCC selection is along column direction to decouple the read & write

Zhang, ISSCC'05

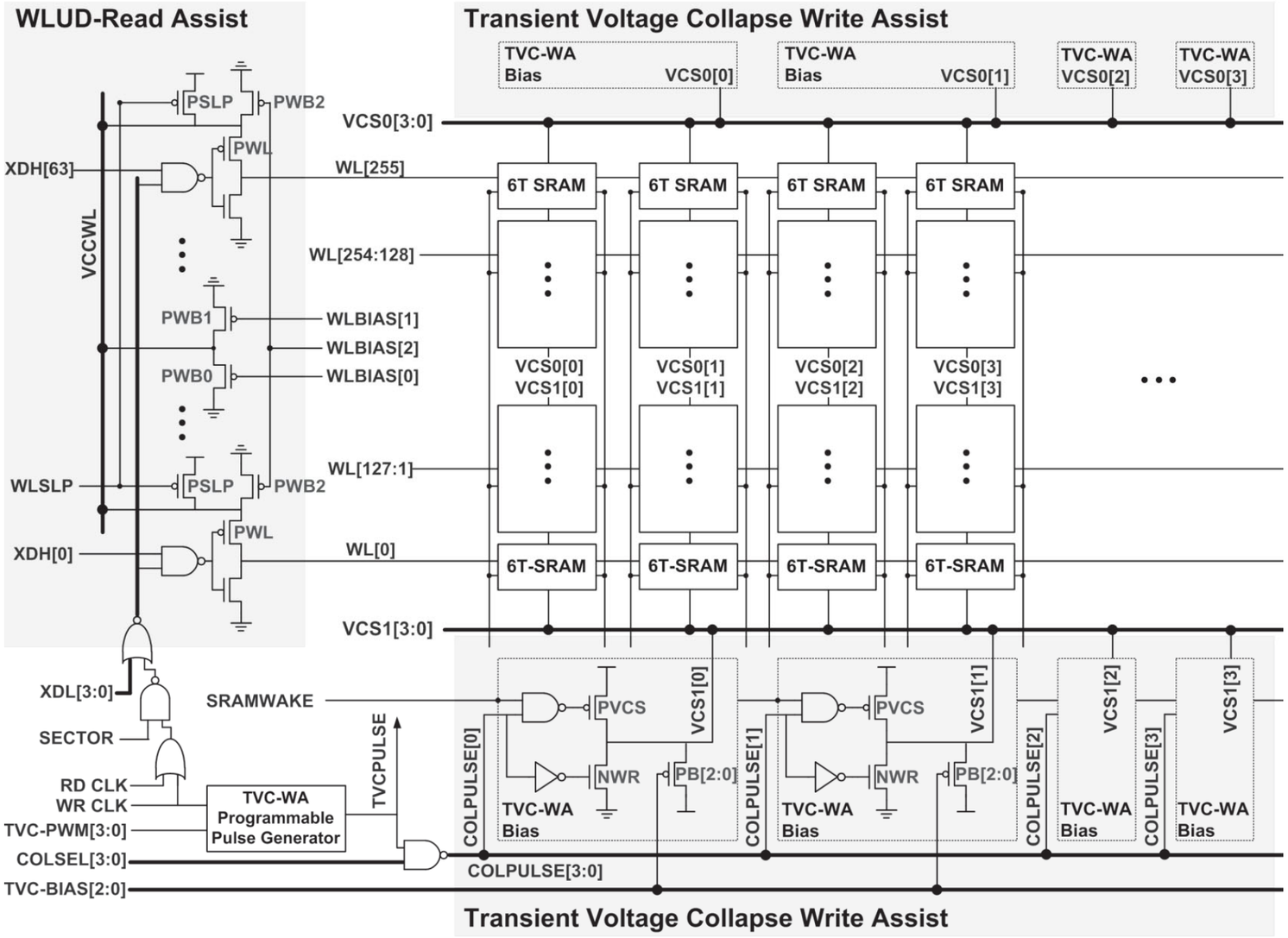
# Floating VDD Technique

- W/o second supply



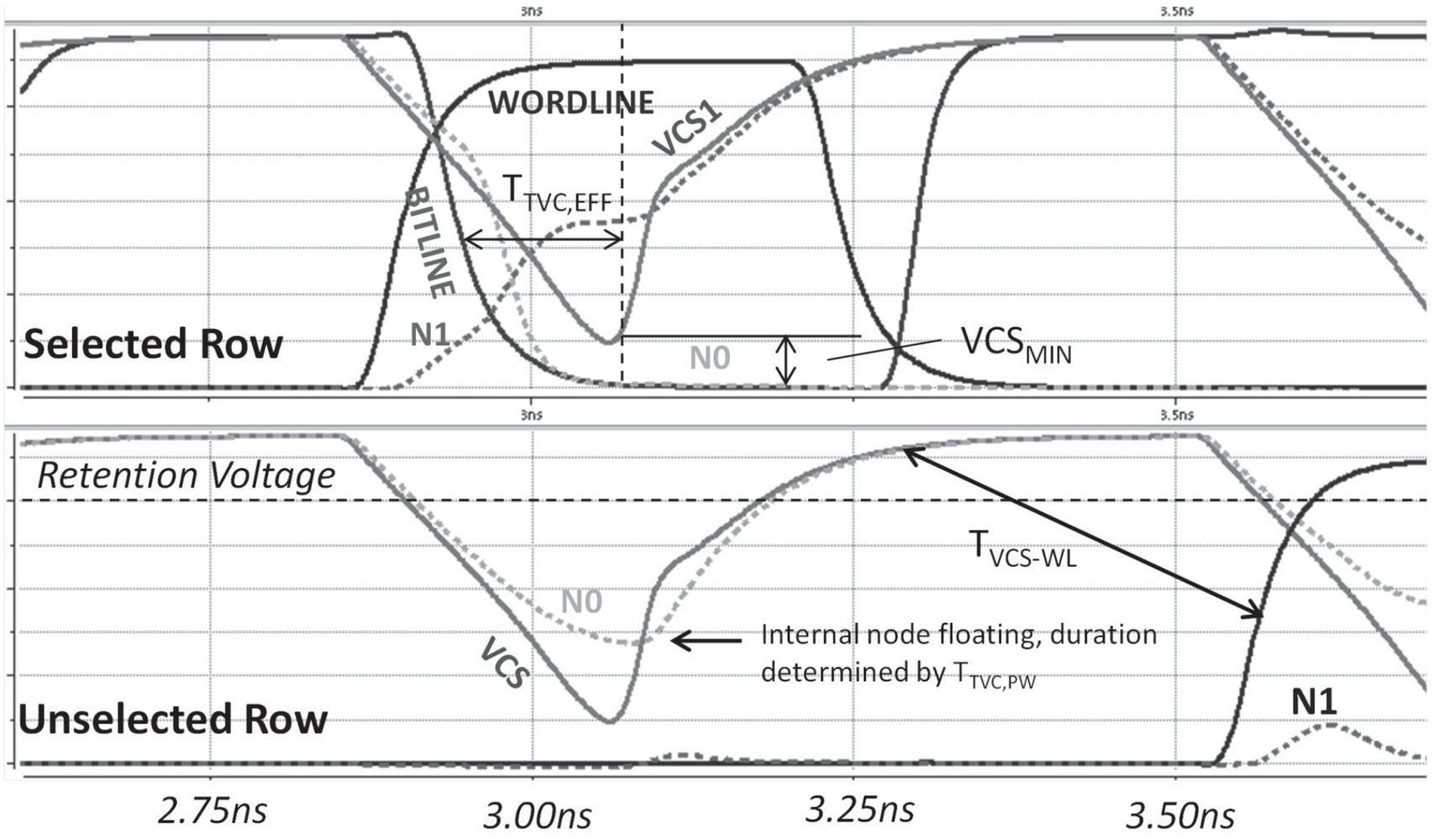

Yamaoka, ISSCC'04

# Collapsing $V_{DD}$ Technique



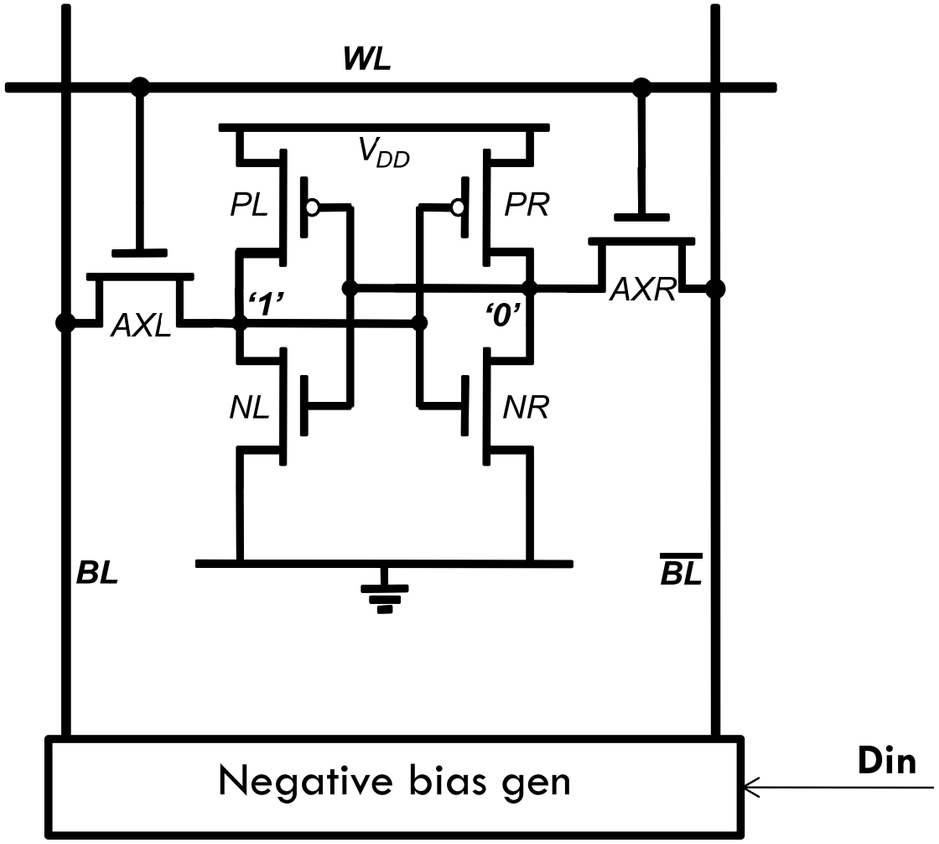

E. Karl, ISSCC'12

# Collapsing $V_{DD}$ Technique



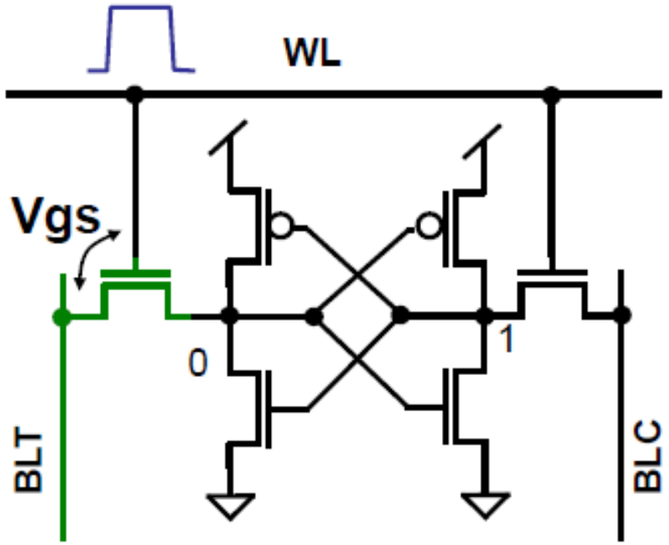

E. Karl, ISSCC'12

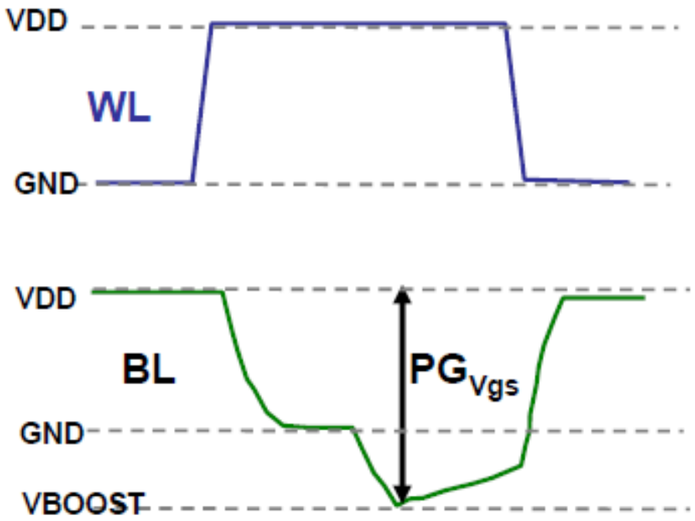
# Negative BL




Nii, VLSI'08

# Negative BL

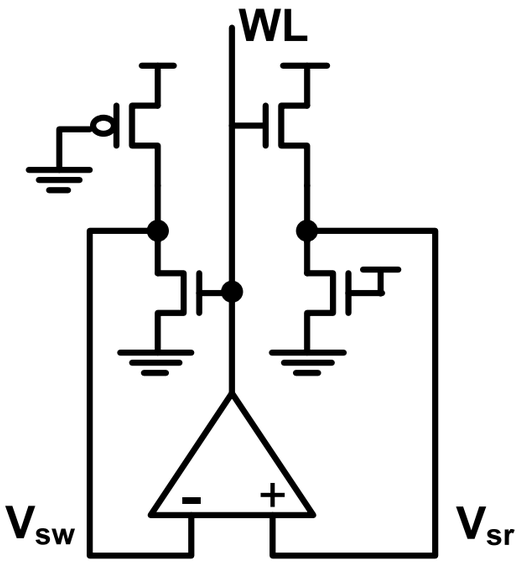


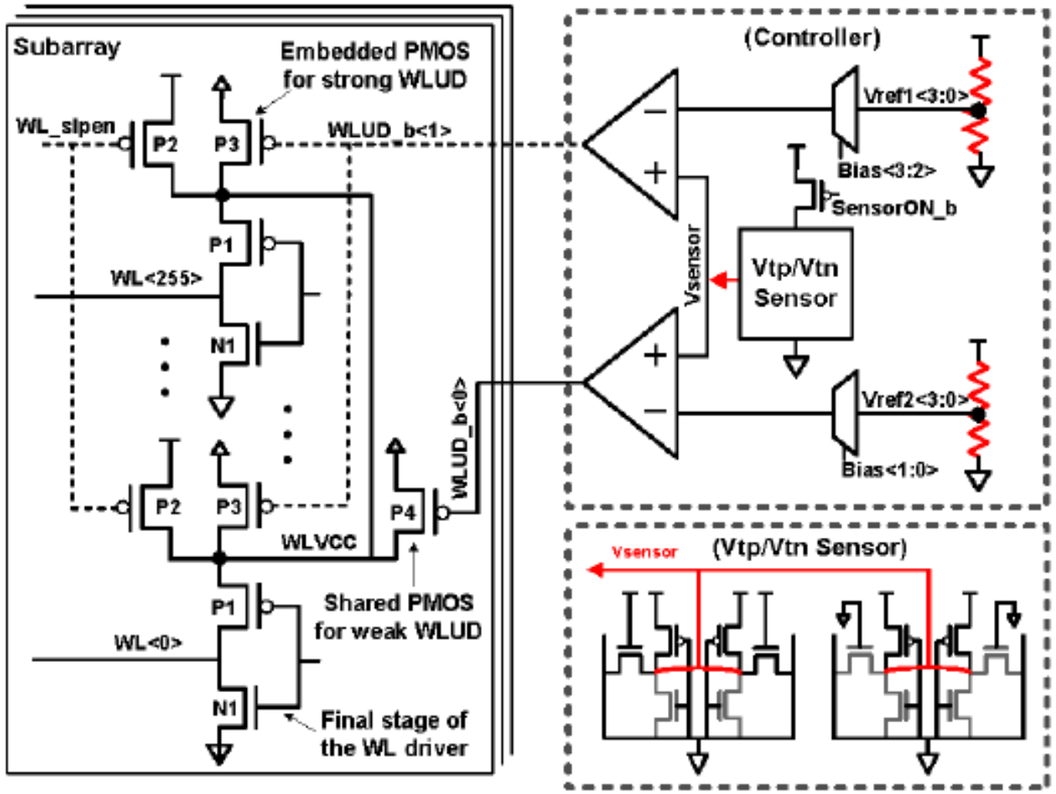

- Arsovski, ISSCC'11

# WL Underdrive

- Sensing appropriate WL voltage

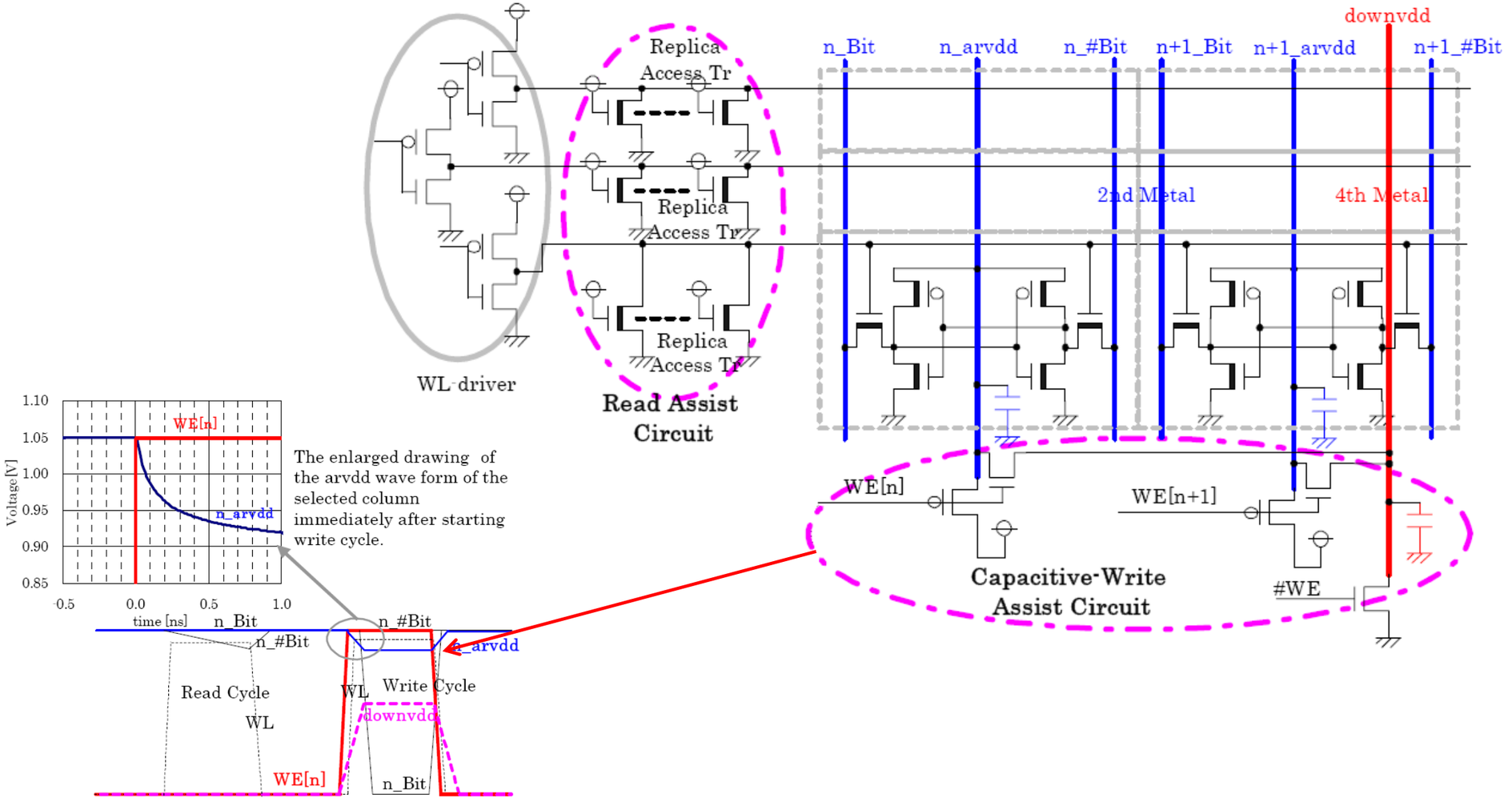



Carlson, CICC'08




Nho, ISSCC'10

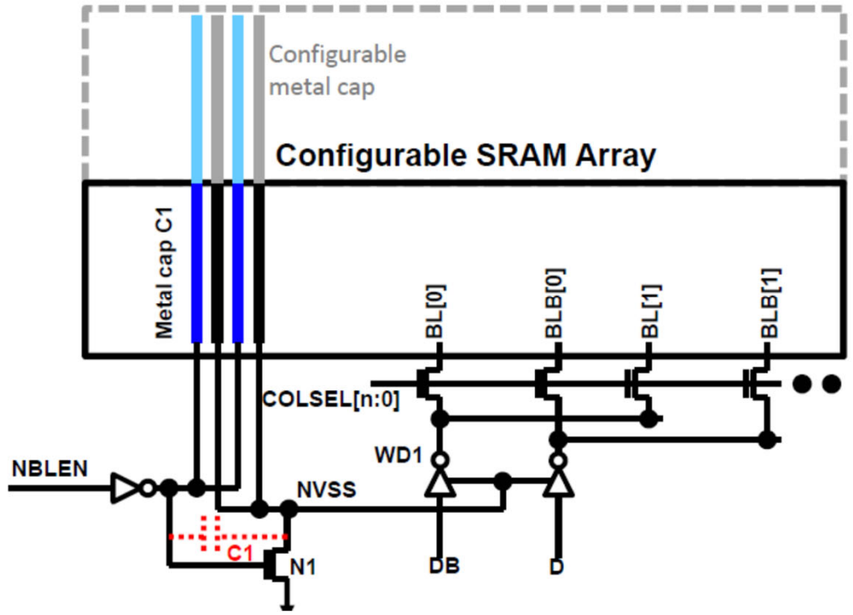
# Capacitive Write Assist + WL Underdrive



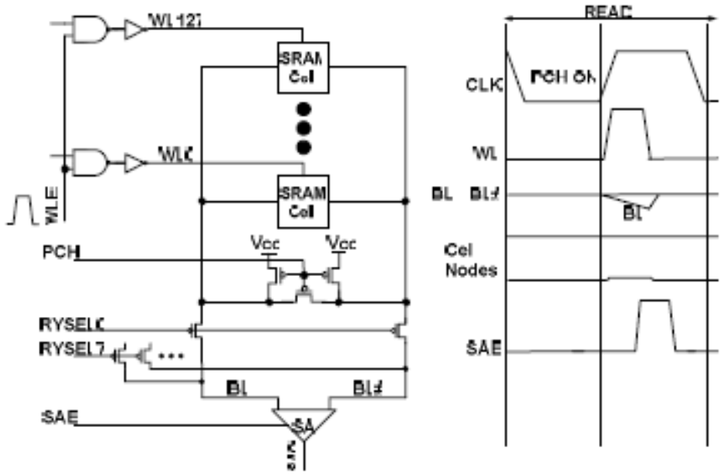

S. Ohbayashi, *VLSI* 2006

# Capacitive Write Assist (ISSCC'20)

- 5nm SRAM [J. Chang, ISSCC'20]



# Pulsed WL/BL



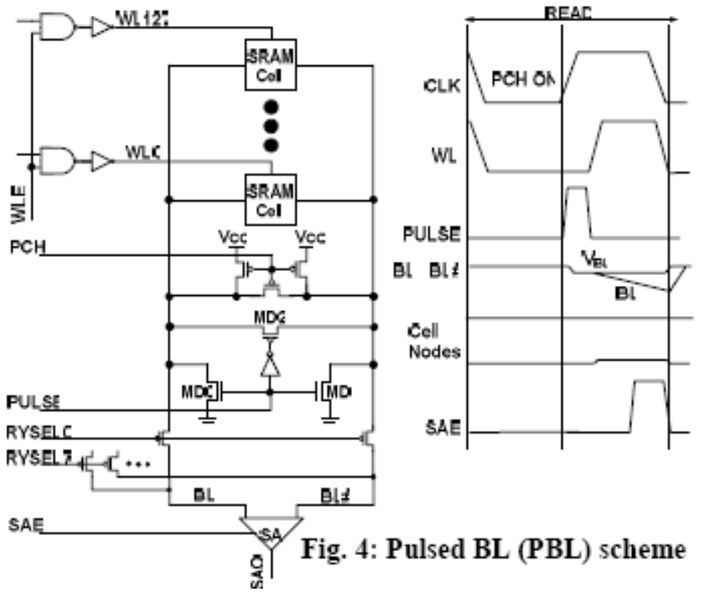



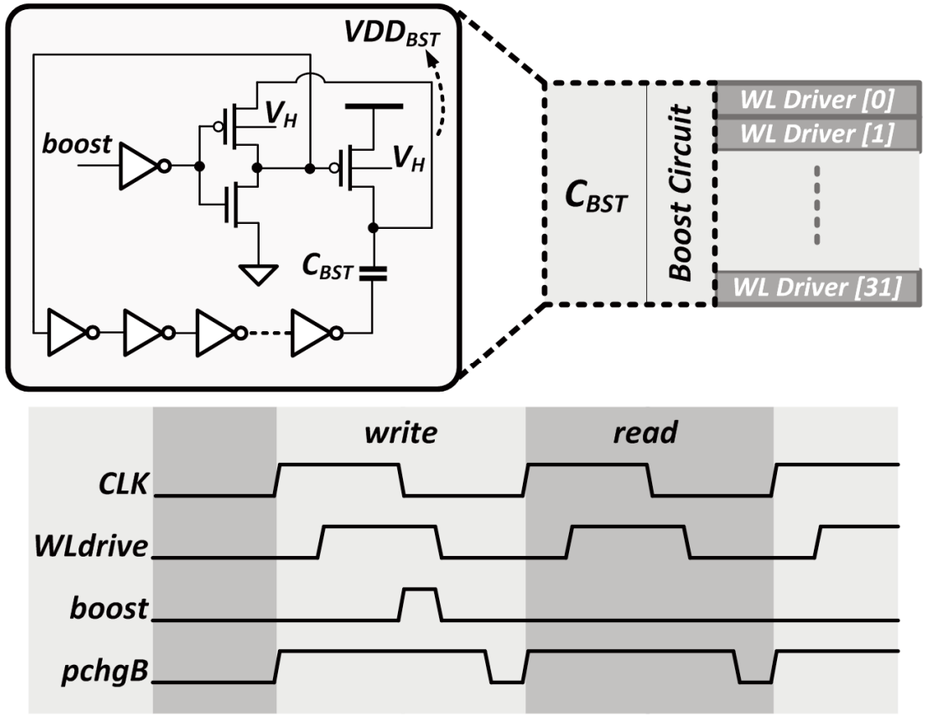

Fig. 4: Pulsed BL (PBL) scheme

M.Khellah, *VLSI* 2006

# Pulsing WL

Wordline pulse shape


Generating boost



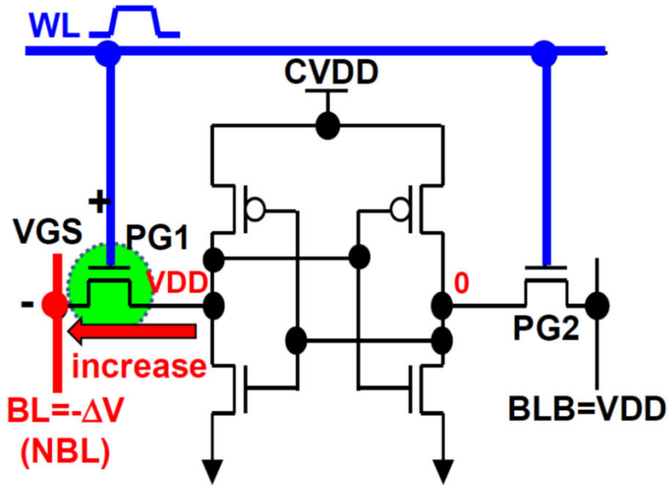

- Sinangil, ISSCC'2011

# ISSCC'17 – 7nm SRAM

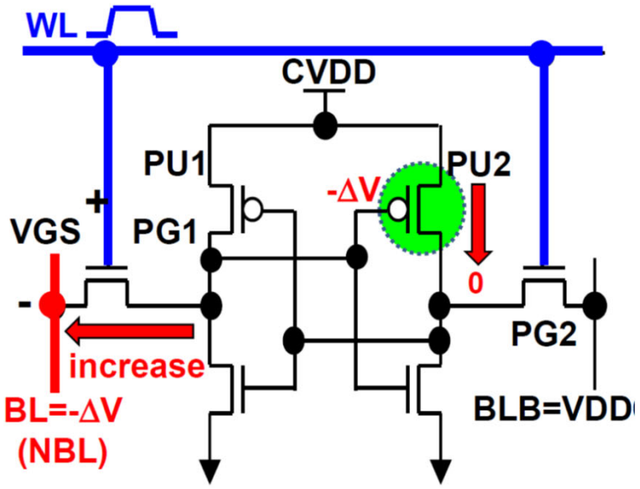
## Write Assist Techniques

- Negative Bit-Line (NBL):
  - increase PG1 and PU2 strength
- Improve both contention and recovery

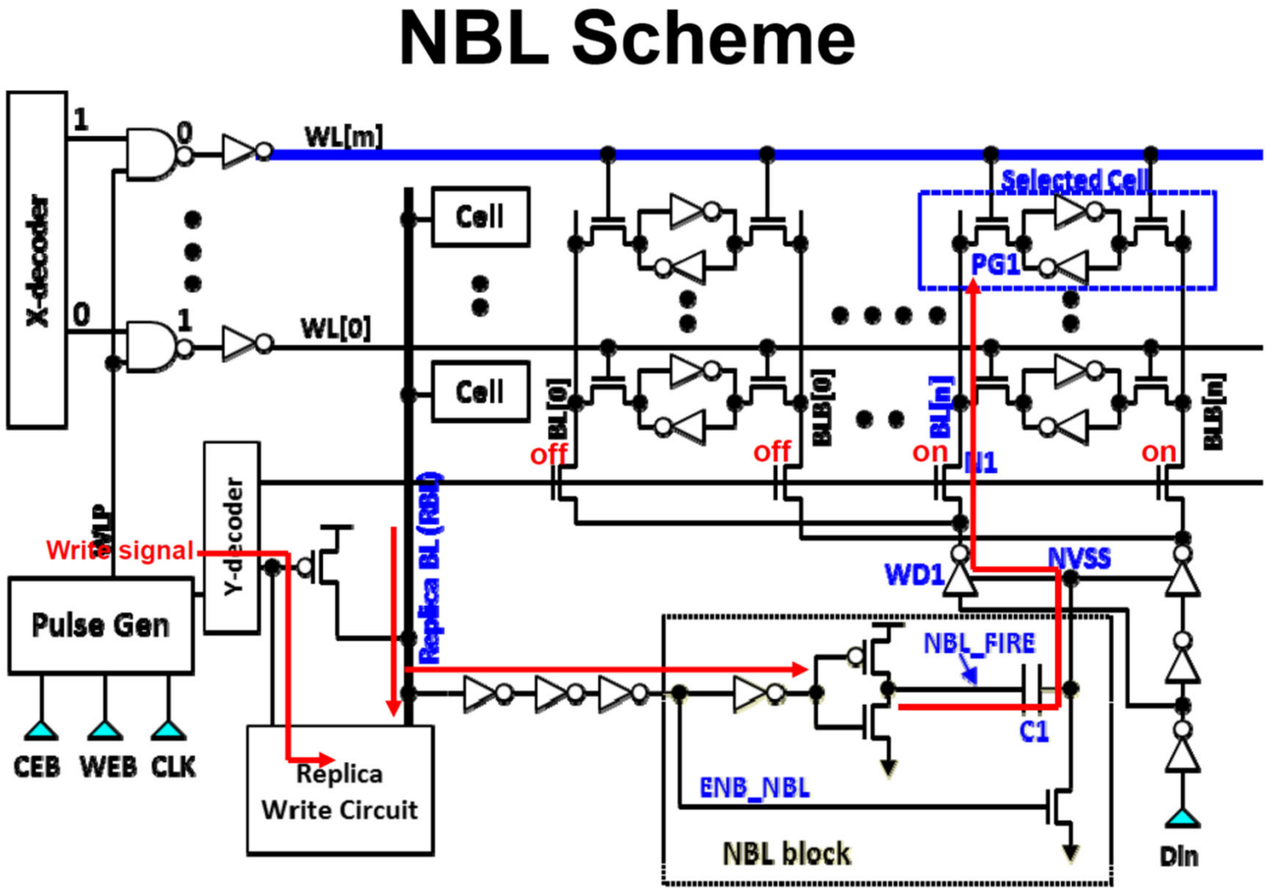
NBL: increase PG1 strength




NBL: increase PU2 strength

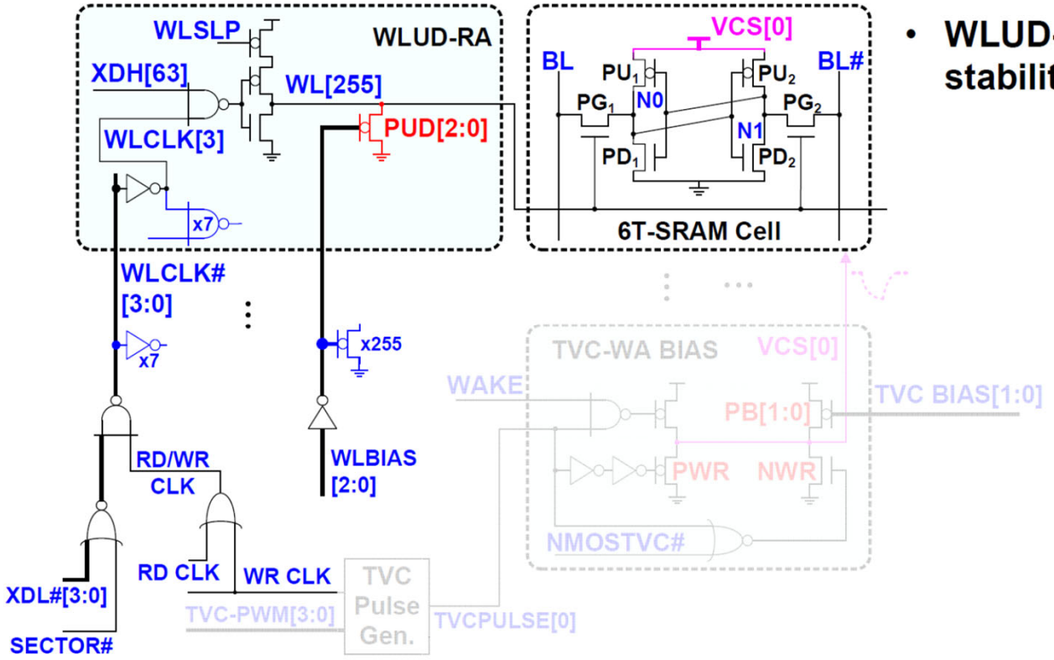


# ISSCC'17 – 7 nm SRAM



# ISSCC'18 - 10nm Read Assist

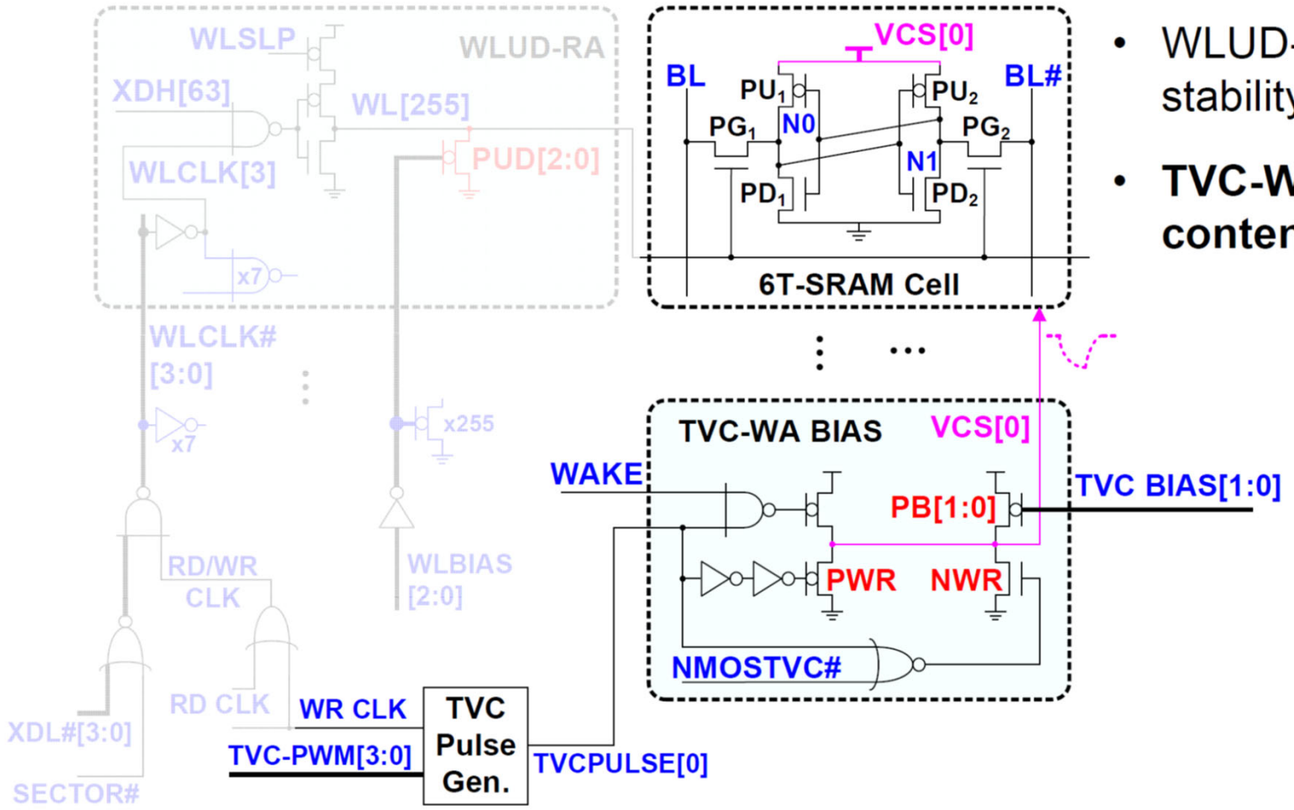
- Wordline underdrive




- **WLUD-RA for improved stability margin (1.5% area)**

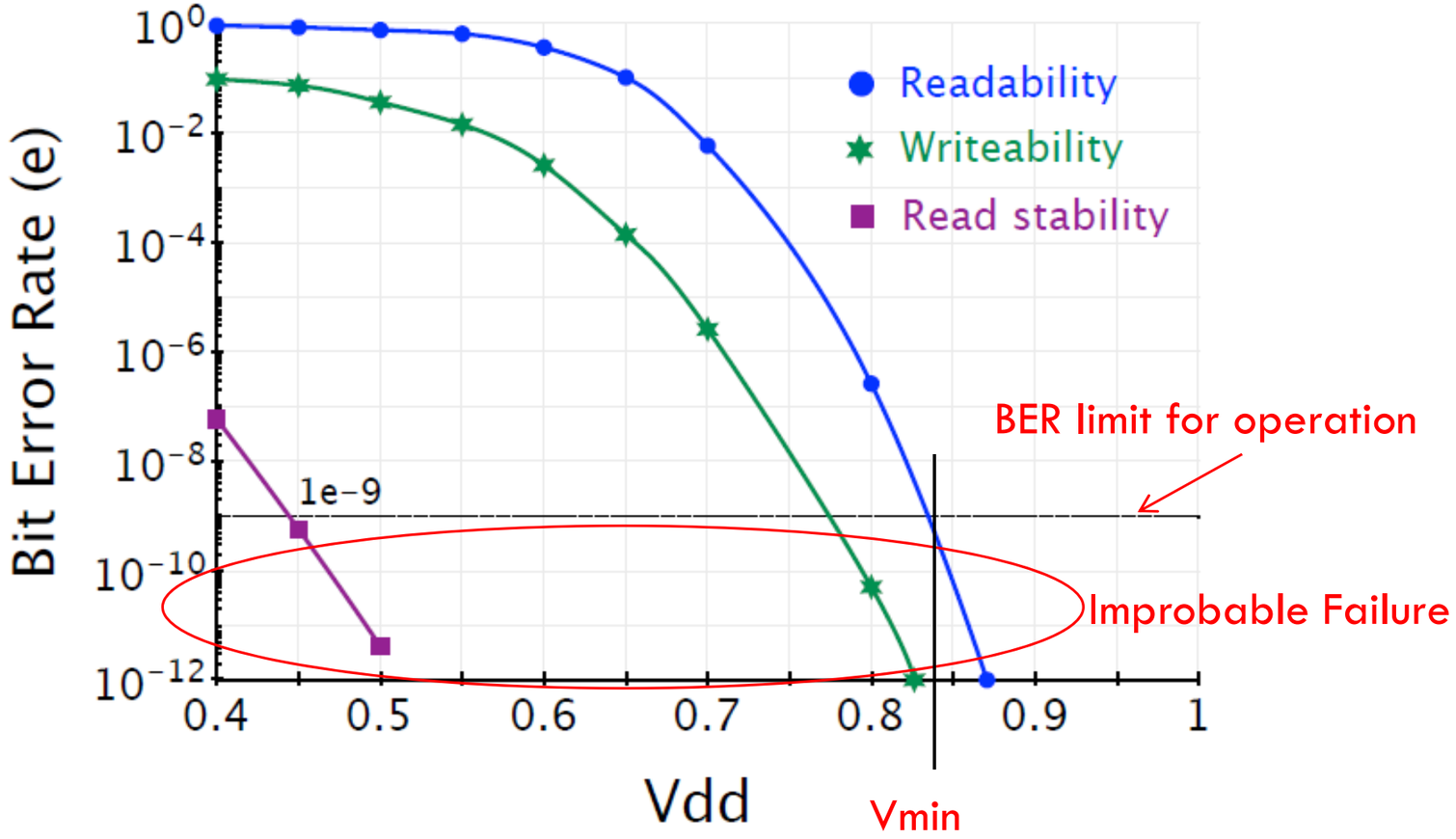
# ISSCC'18 - 10nm SRAM

- Transient voltage collapse



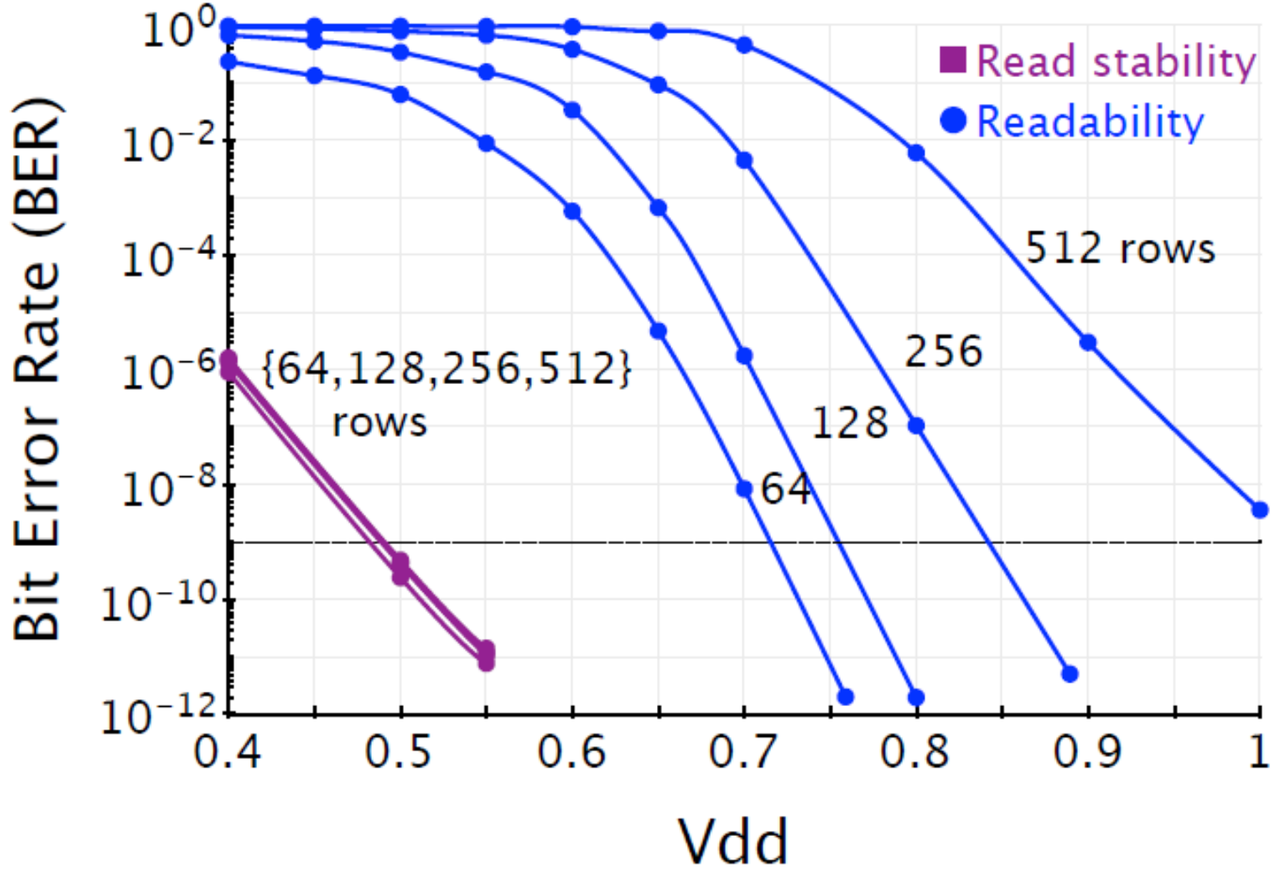

- WLUD-RA for improved stability margin (1.5% area)
- **TVC-WA to reduce PU:PG contention (3.3% area)**

# SRAM Failure Rates

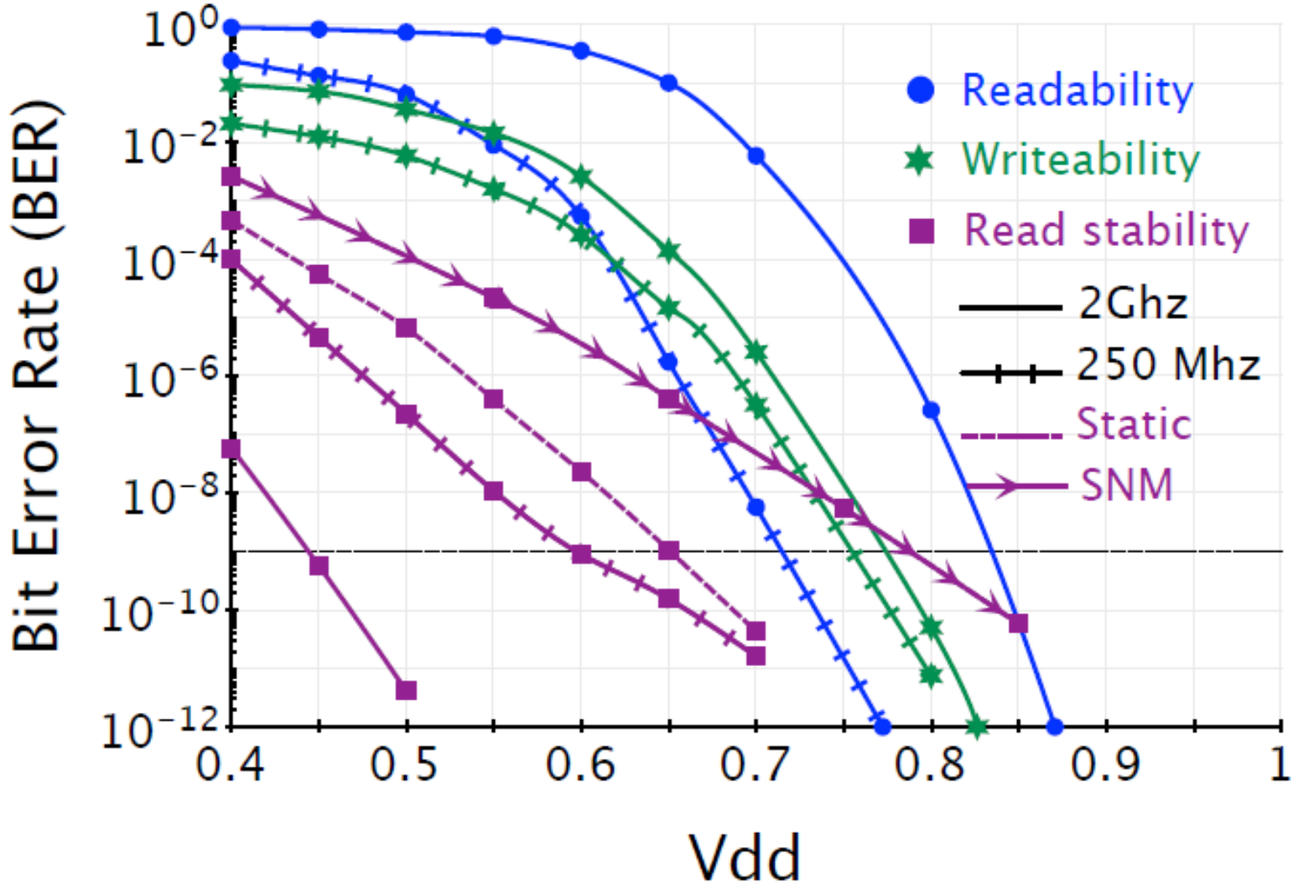



Readability, writeability, and read-stability failure rates for a 28nm 6T SRAM bitcell

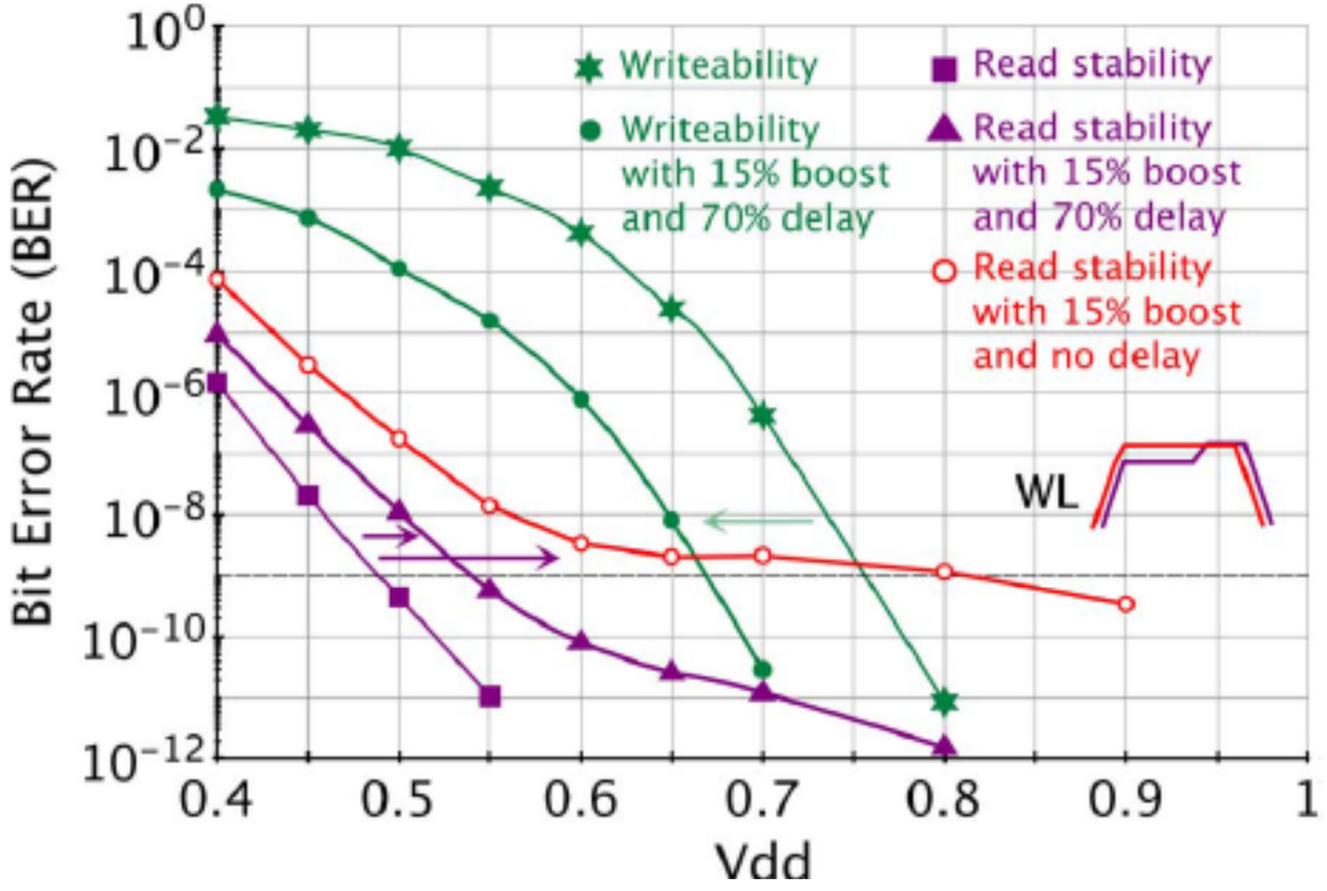
# Effect of bitline capacitance



# Effect of clock period



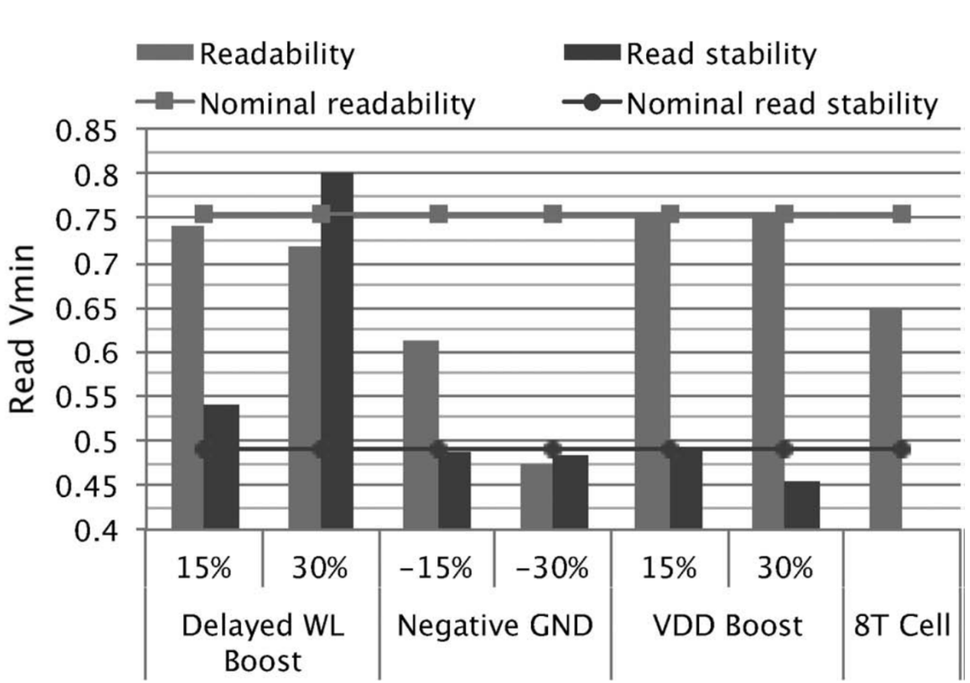
# Effect of Assist Techniques

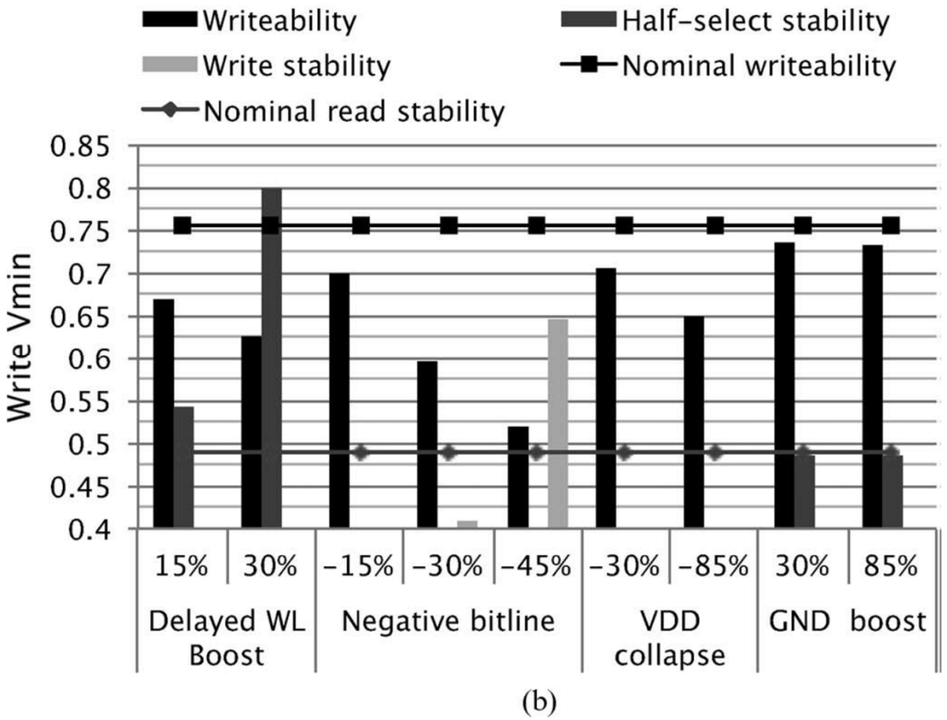



Zimmer, TCAS-I'12

# How Do They Stack Up?

- 28nm bulk CMOS

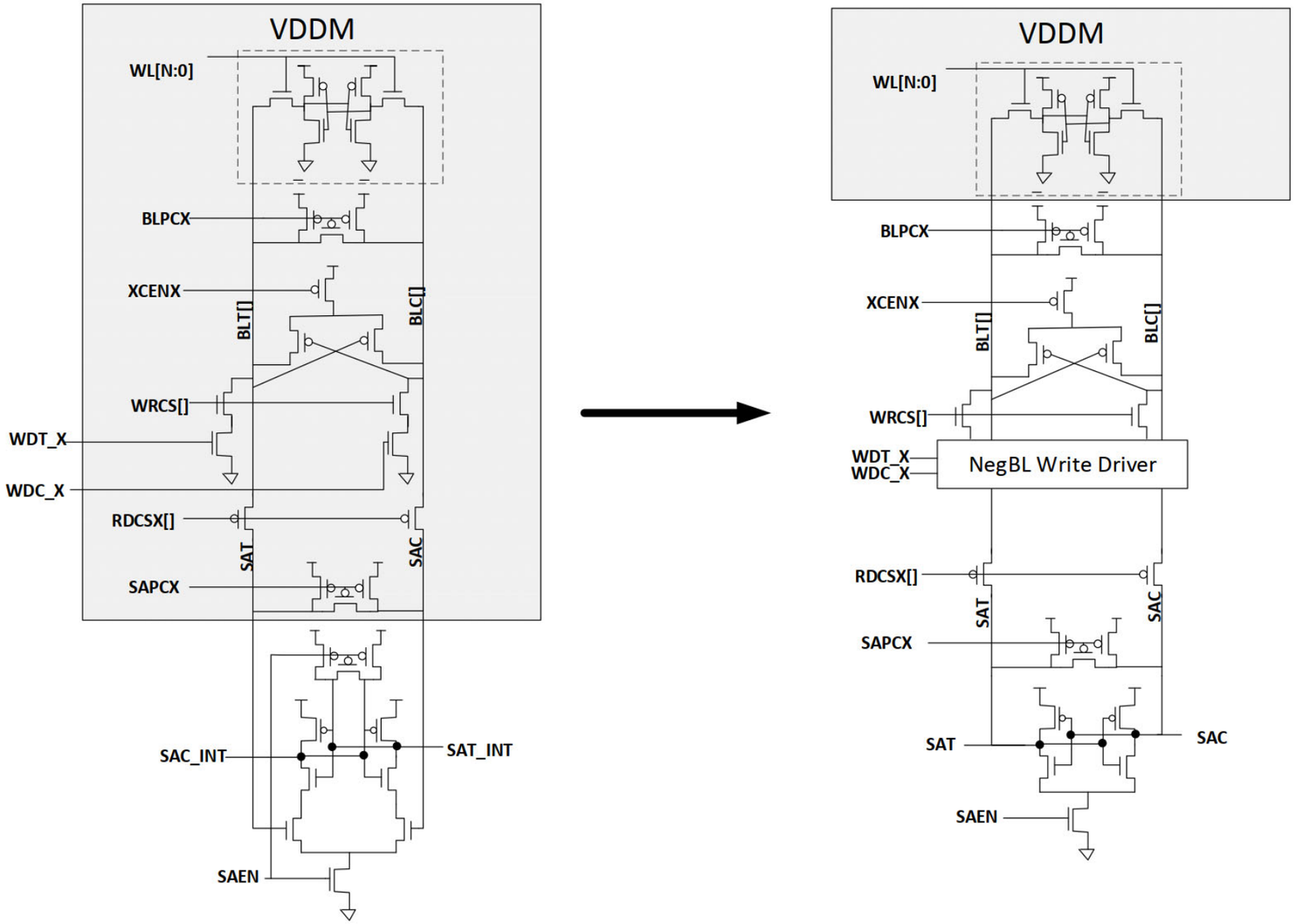



(b)

# SRAM In Practice

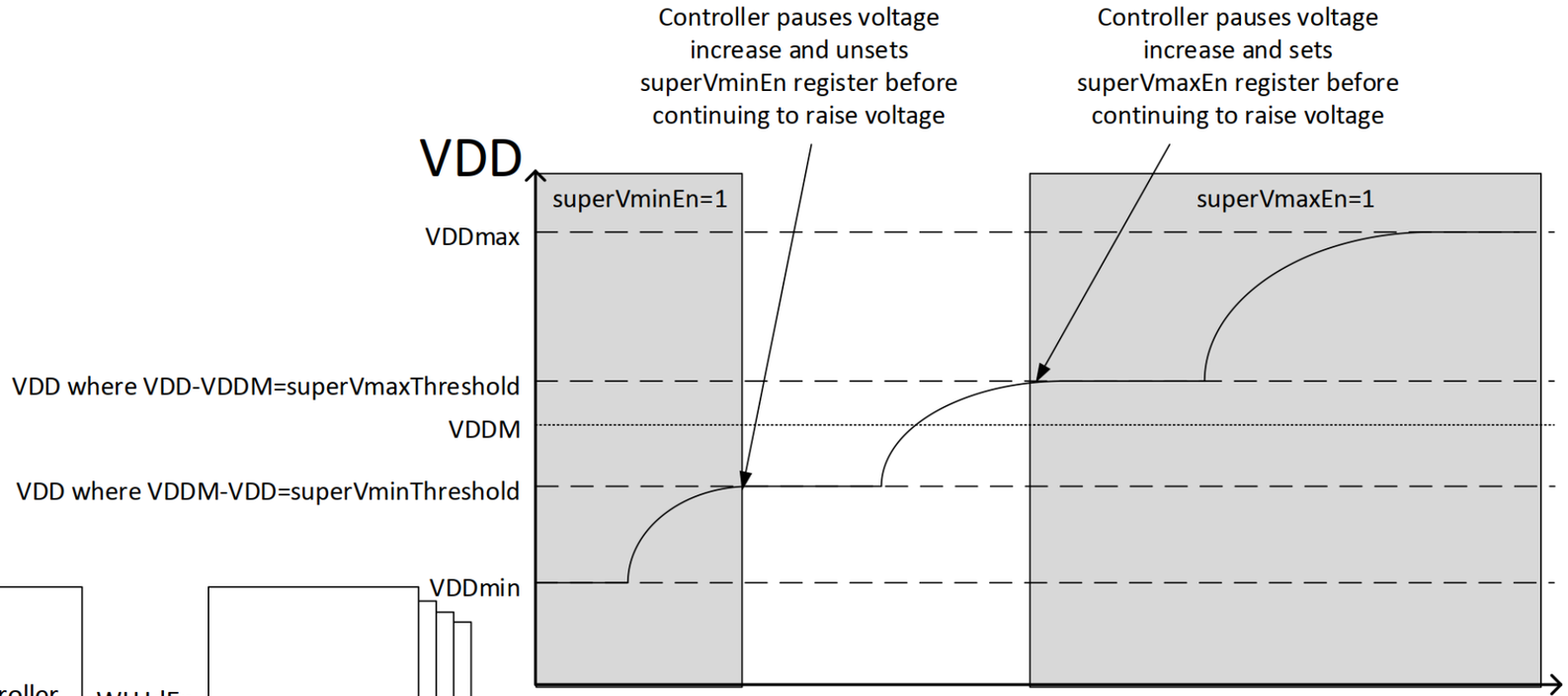
- 7nm AMD Zen2 (Singh, ISSCC'20)

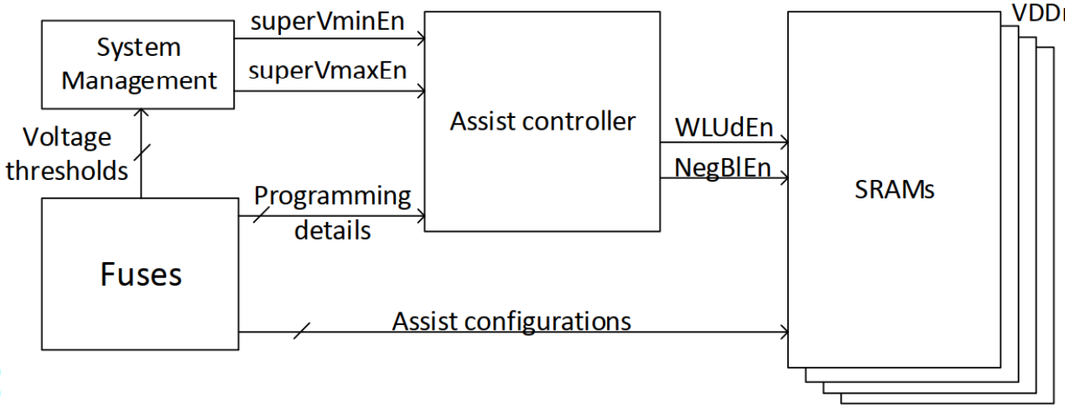


# SRAM In Practice

- 7nm AMD Zen2 (Singh, ISSCC'20)

  - Moving bitline precharge to VDD creates both bitcell stability and writeability challenges
  - High level of configurability allows for silicon flexibility



# Next Lecture

- More peripheral circuits
- ECC
- Alternatives to 6T SRAM