# EE241B : Advanced Digital Circuits

## Lecture 14 – SRAM 2

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**March 4, 2020, AnandTech**

**El Capitan Supercomputer Detailed:** AMD CPUs & GPUs to drive 2 Exaflops of compute.

Back in August, the United States Department of Energy and Cray announced plans for a third United States exascale supercomputer, El Capitan. Scheduled to be installed in Lawrence Livermore National Laboratory (LLNL) in early 2023.

# Announcements

- Quiz 2 on Thursday
- Please send me links to your project web pages
- Assignment 3 due next week
- Project midterm reports due next week

# Midterm report

Title (Meaningful)

Names

Abstract (5 sentences)

1. Subject area; Problem statement
2. Contrast; define state of the art
3. Key contribution
4. Basis for comparison
5. Summary of results

1. Introduction
2. Summarize the proposed techniques
3. Set up environment for comparison
4. Hypotheses to be tested / comparison of other people's results
5. Conclusion

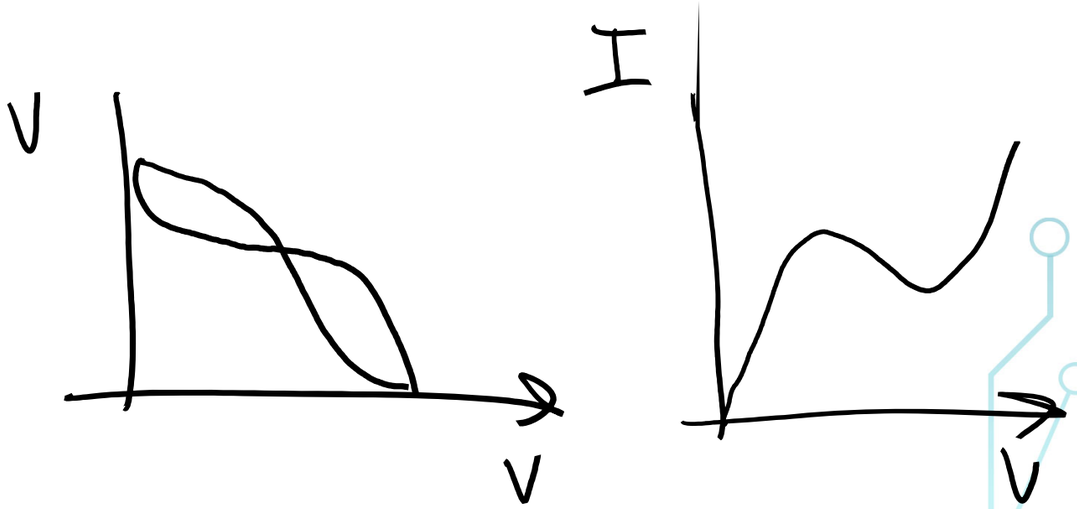
References

4-pages (2 column)

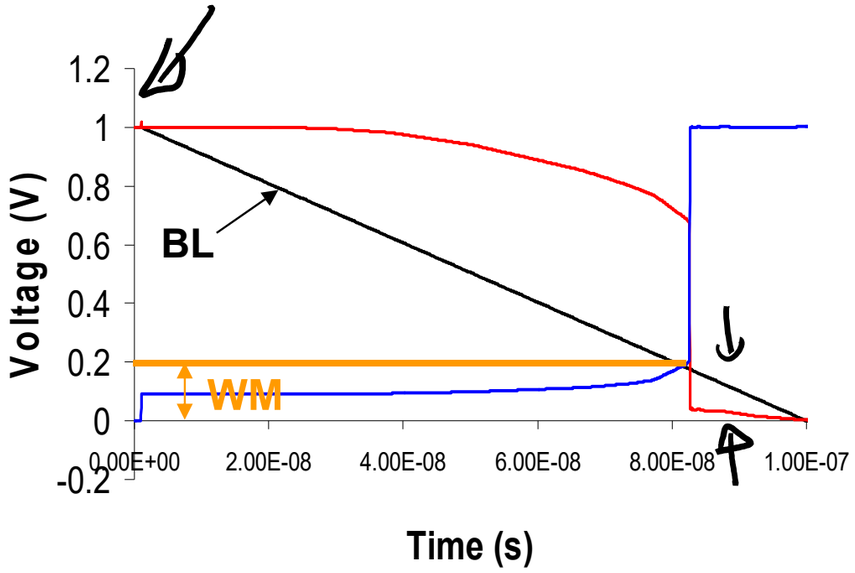
# Outline

- Module 4
  - SRAM dynamic margins
  - Assist techniques

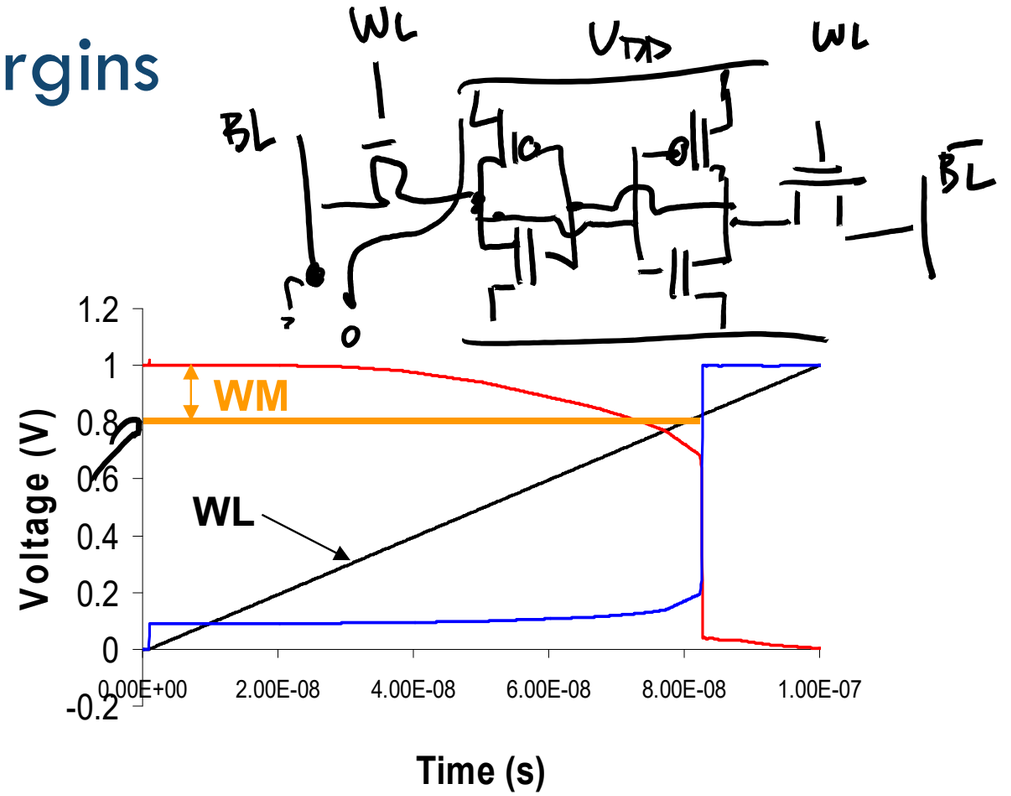
# 4.C Static Read/Write Margins



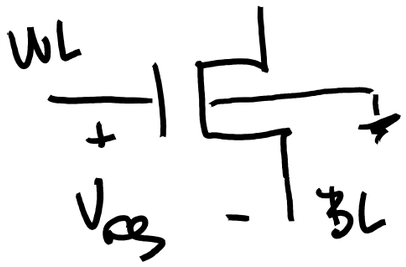
# Writeability – BL/WL Write Margins



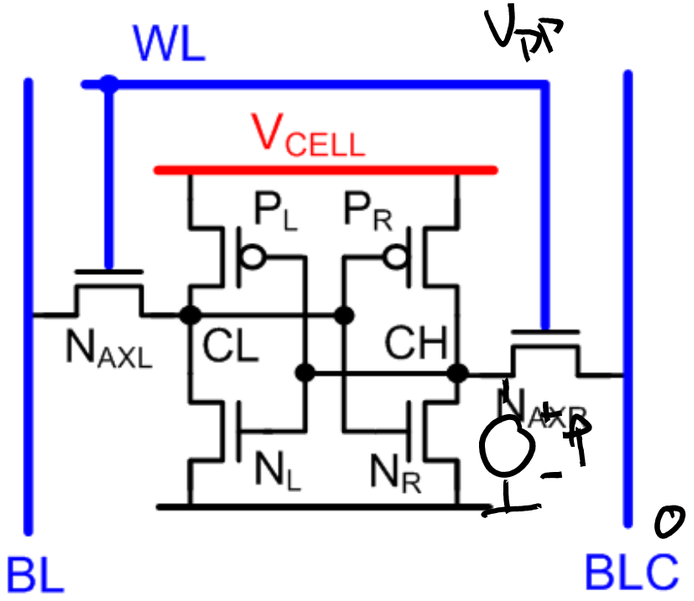

- Highest BL voltage under which write is possible when BLC is kept precharged



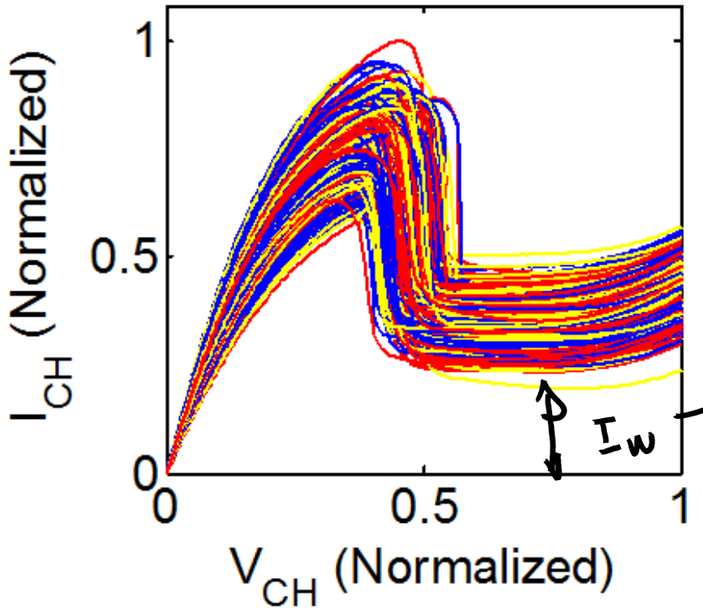

- Difference between VDD and lowest WL voltage under which write is possible

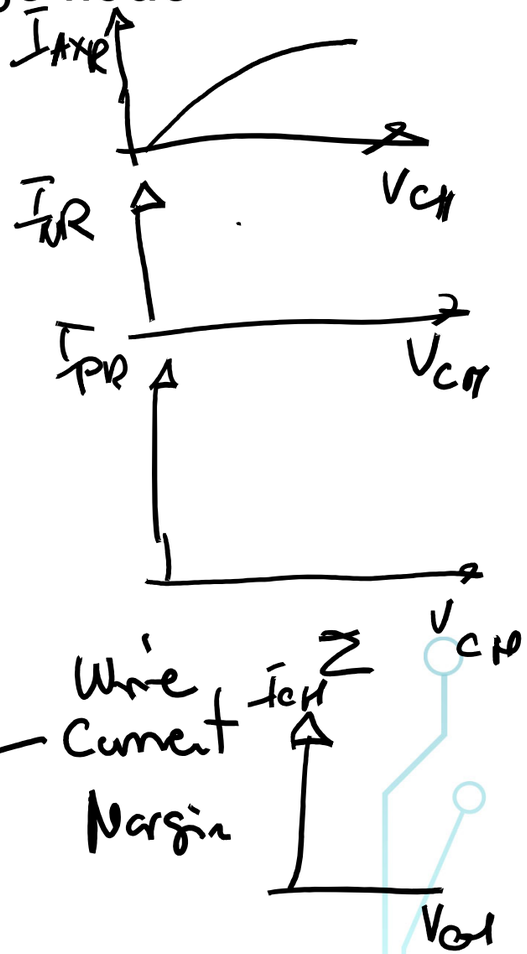


# Write Stability – Write Current (N-Curve)



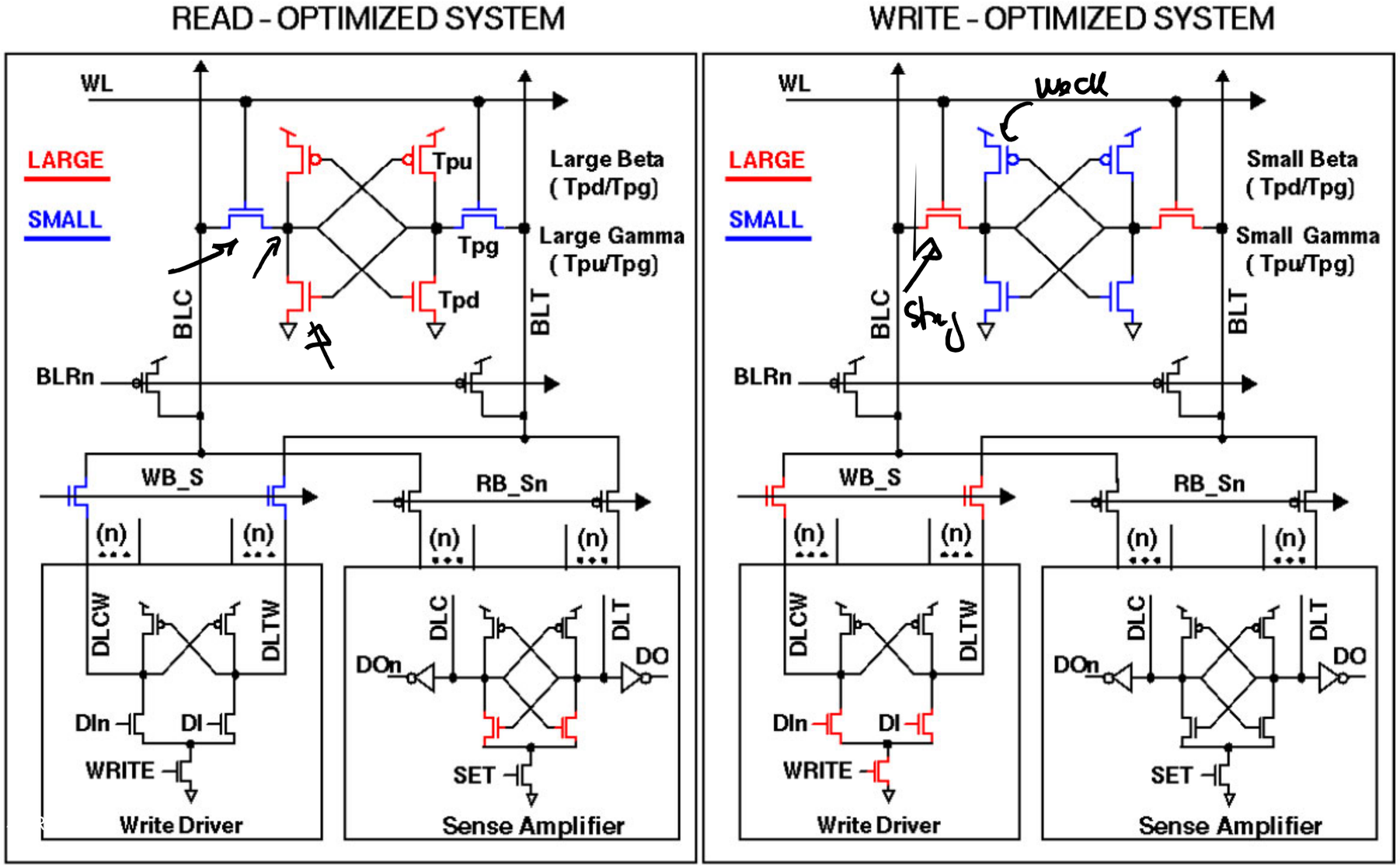

- Minimum current into the storage node



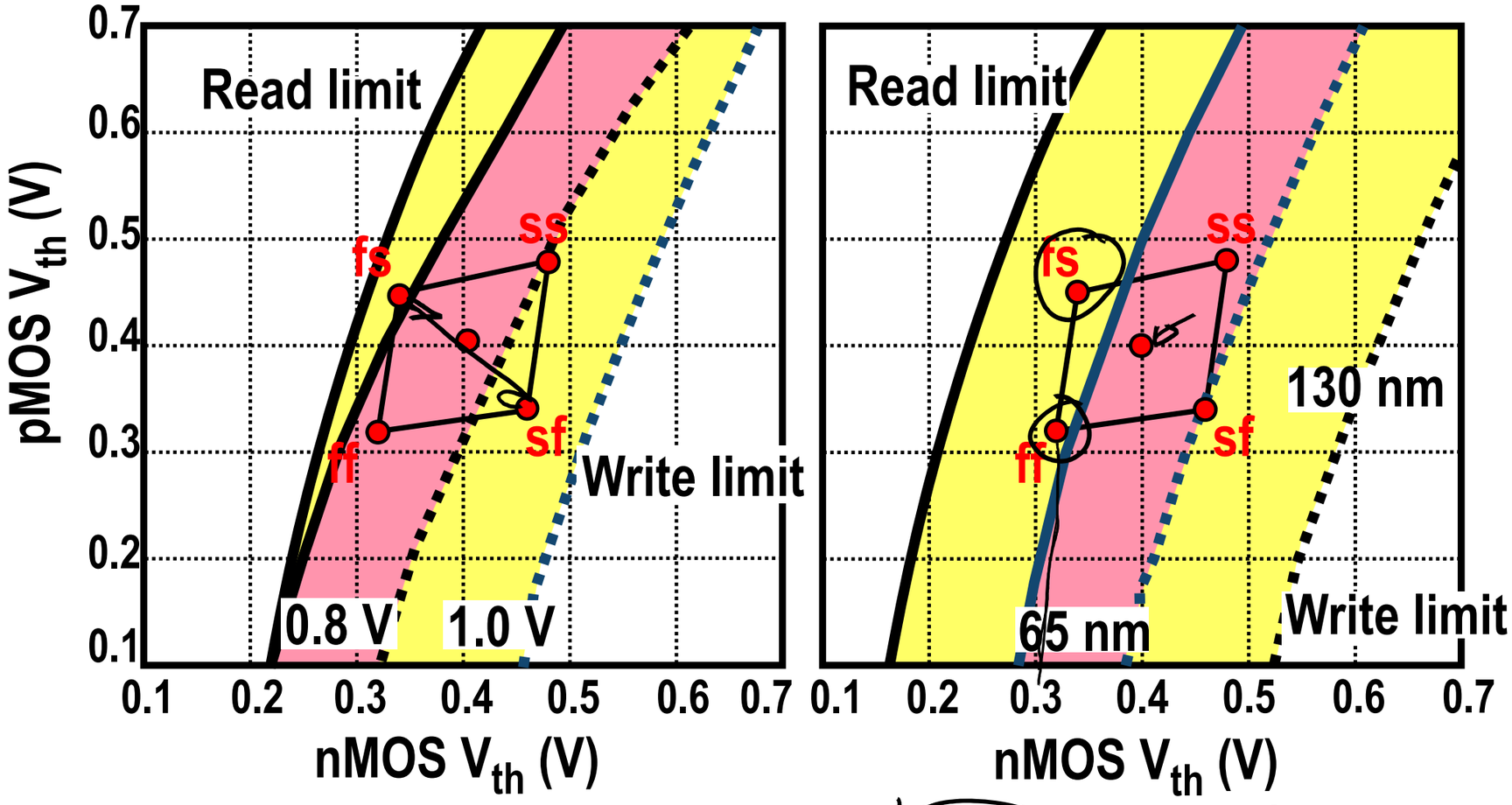

C. Wann et al, *IEEE VLSI-TSA* 2005

# The Conflict Between Read and Write



# $V_{Th}$ Window

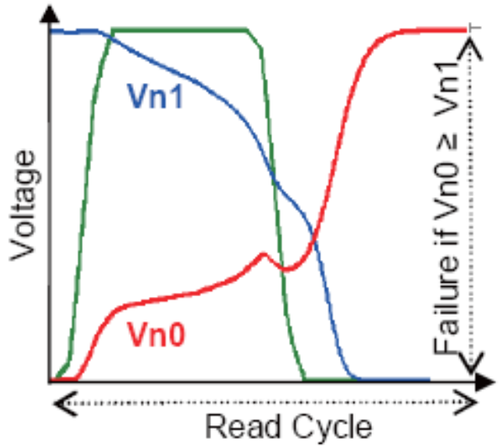
- Assuming global spread



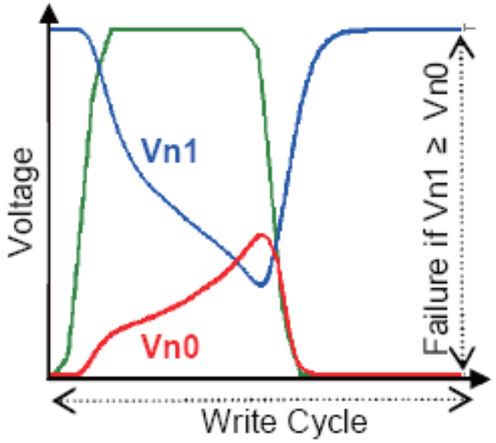

Yamaoka, ISSCC'05

# 4.D Dynamic Margins

# 6-T SRAM Static/Dynamic Stability



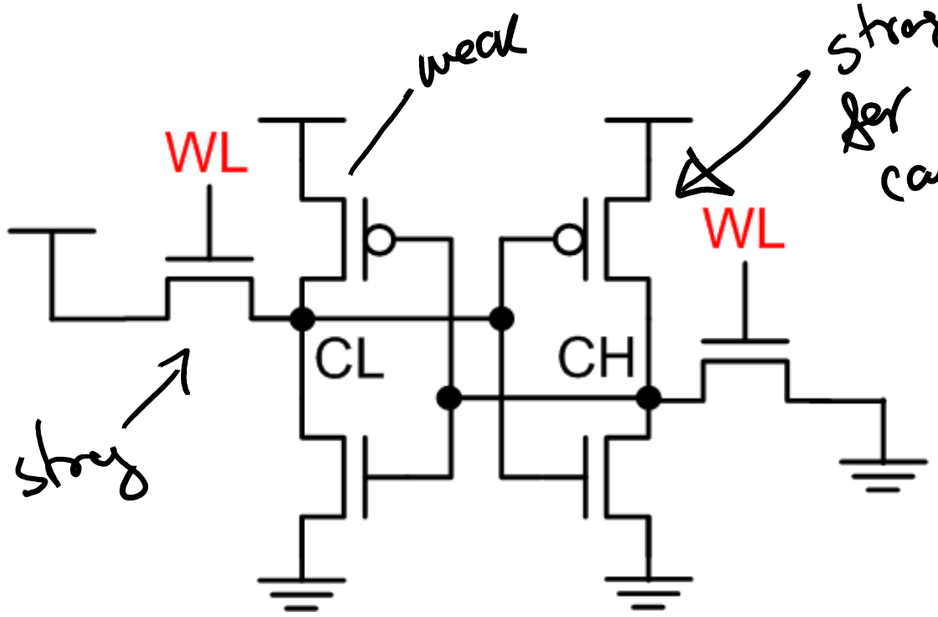
(a) read failure criterion

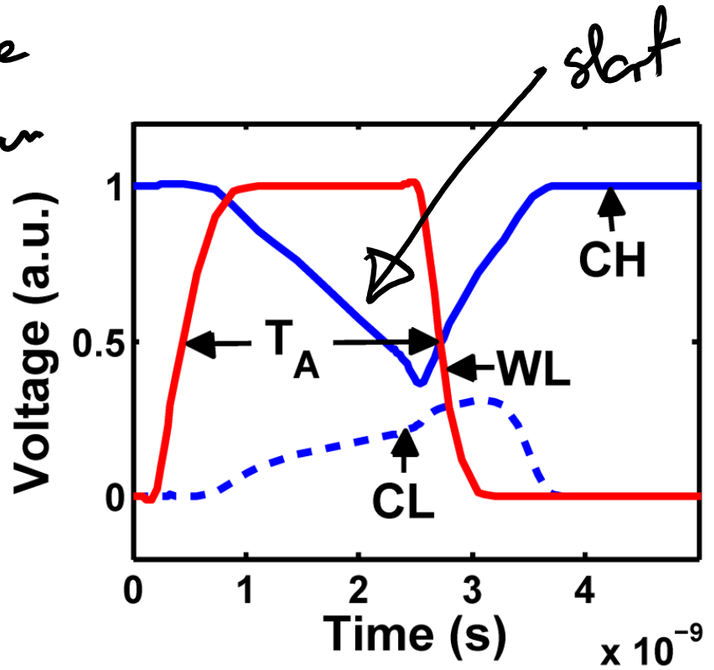


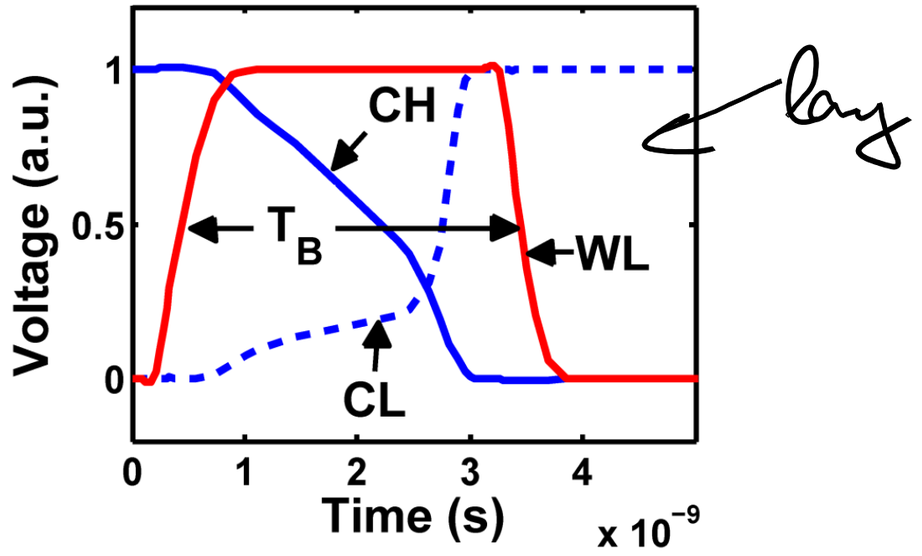
(b) write failure criterion

- Read Margin
  - SNM: pessimistic
- Write Margin
  - WNM: optimistic
- Introduction to dynamic margins
  - Three failure modes: read stability, writeability and read access time

# Dynamic Write Stability (Writability)



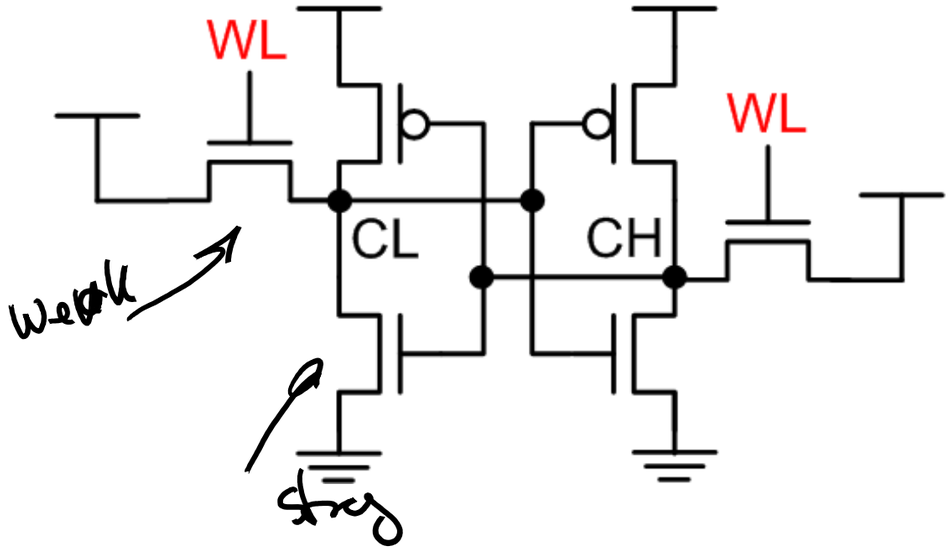



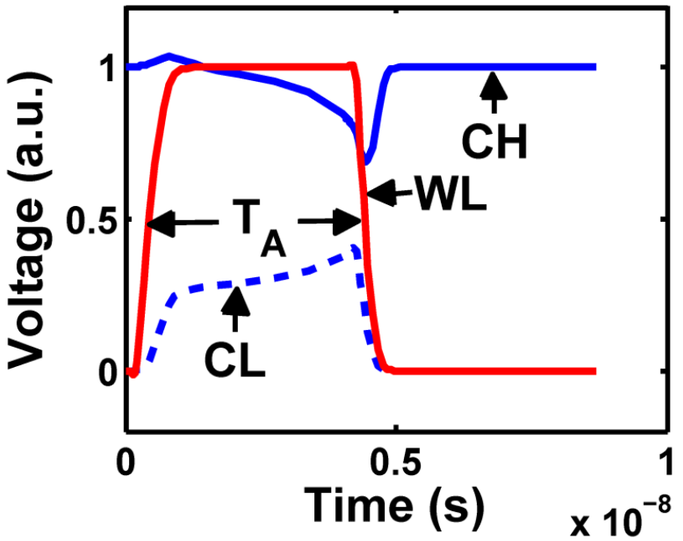



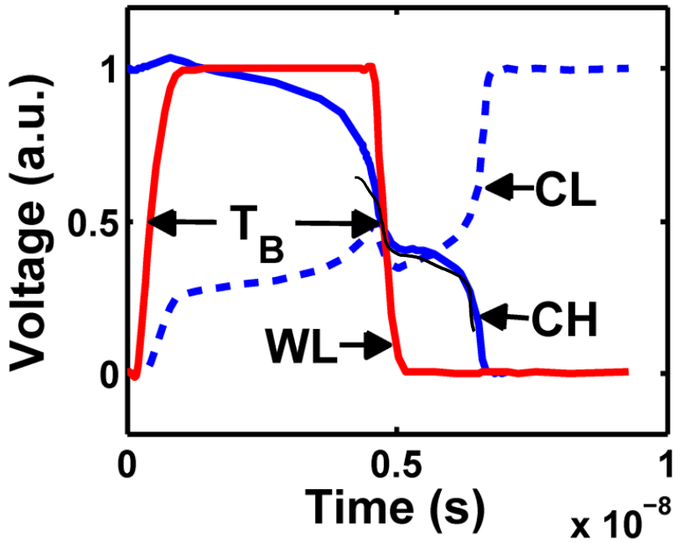

- $T_A < T_{write} < T_B$
- $T_{write}$ = dynamic write stability
- Static margins are optimistic

Khalil, TVLSI'08

# Dynamic Read Stability



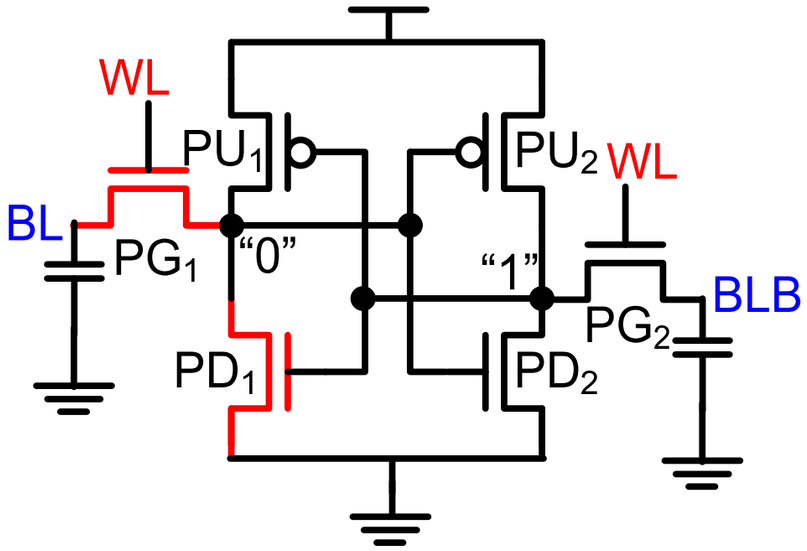



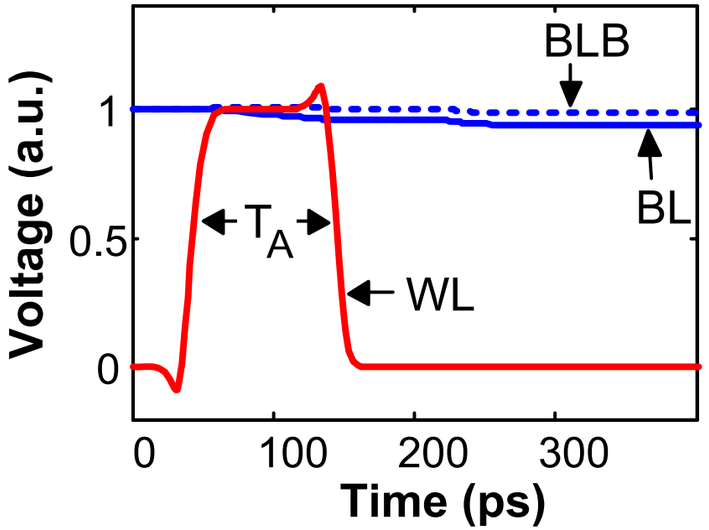




- $T_A < T_{read} < T_B$
- $T_{read}$ = dynamic read stability
- Static margins are pessimistic

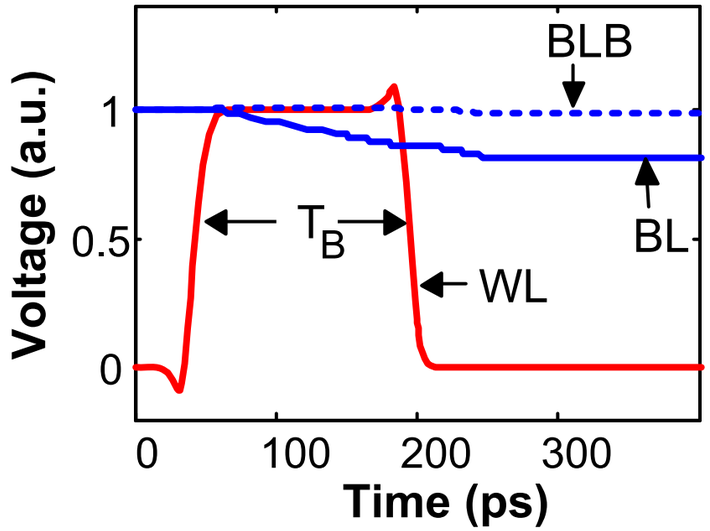
Khalil, TVLSI '08

# Dynamic Read Access




$\Delta V_{BL} < V_{OS}$



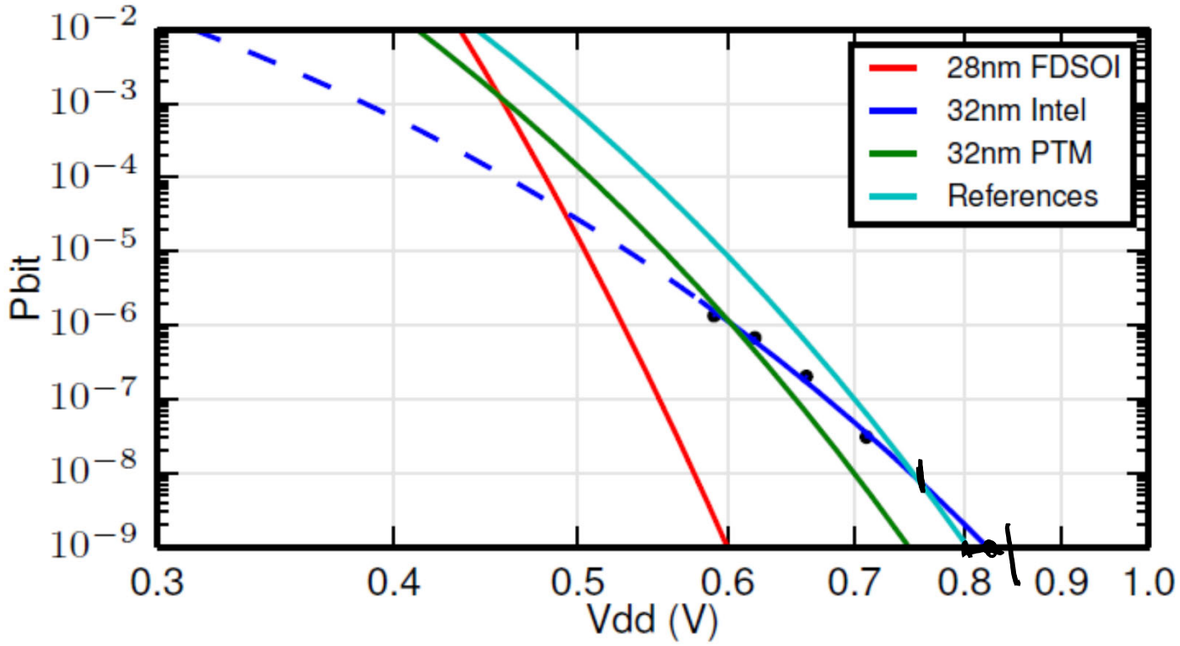

$> V_{OS}$

- $T_A < T_{access} < T_B$
- $PD_1$ and $PG_1$ are critical

Khalil, TVLSI '08

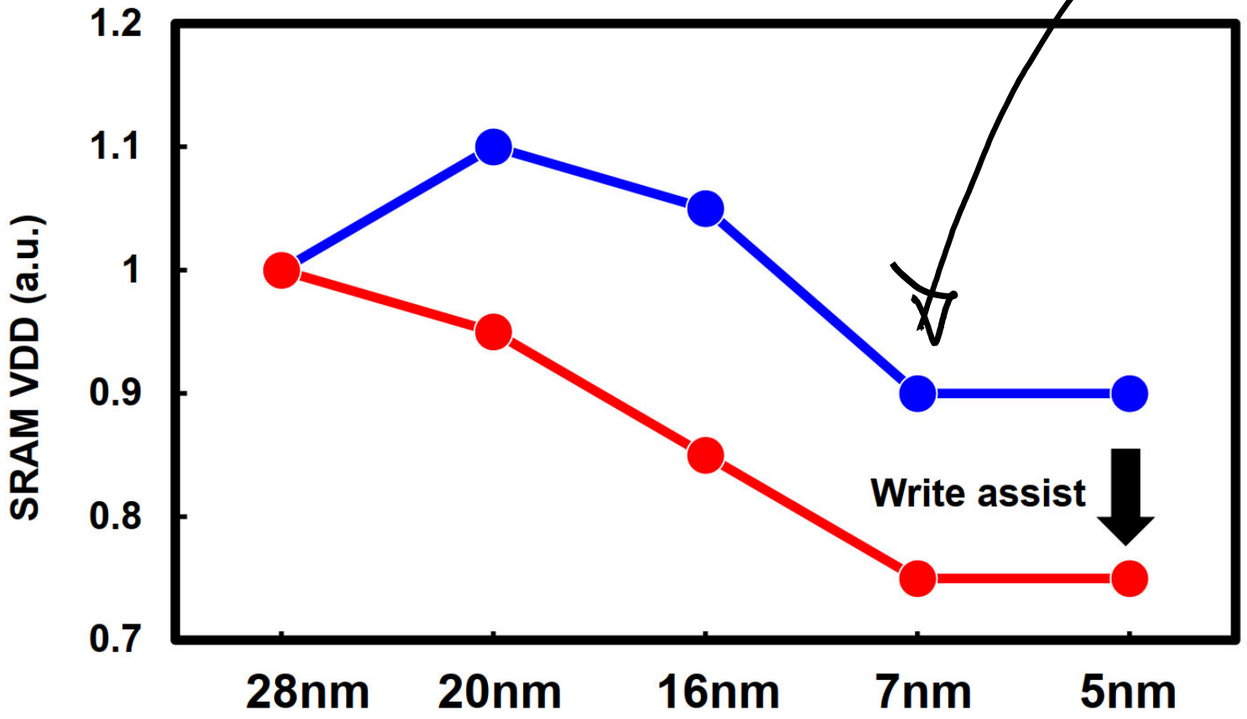
# SRAM Overall Vmin

- Both read and write
- Some contradicting data



# SRAM Vmin Scaling Trend

- SRAM voltage often higher than logic



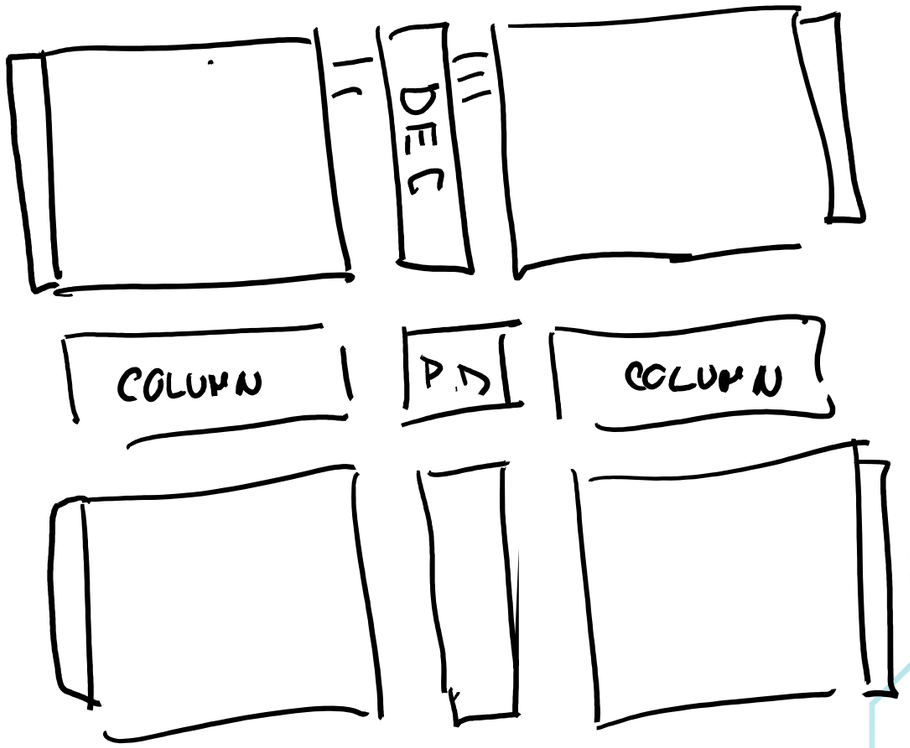

read stable but need write assist

- J. Chang, ISSCC'20

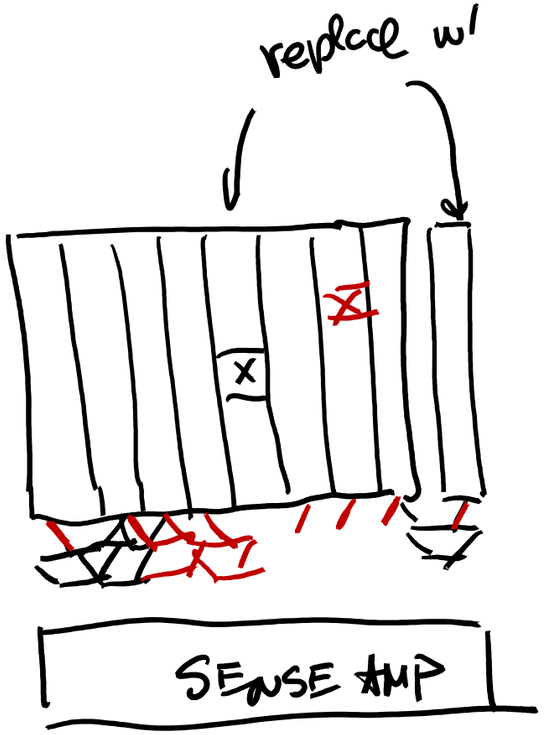
# 4.E SRAM Peripheral Circuits

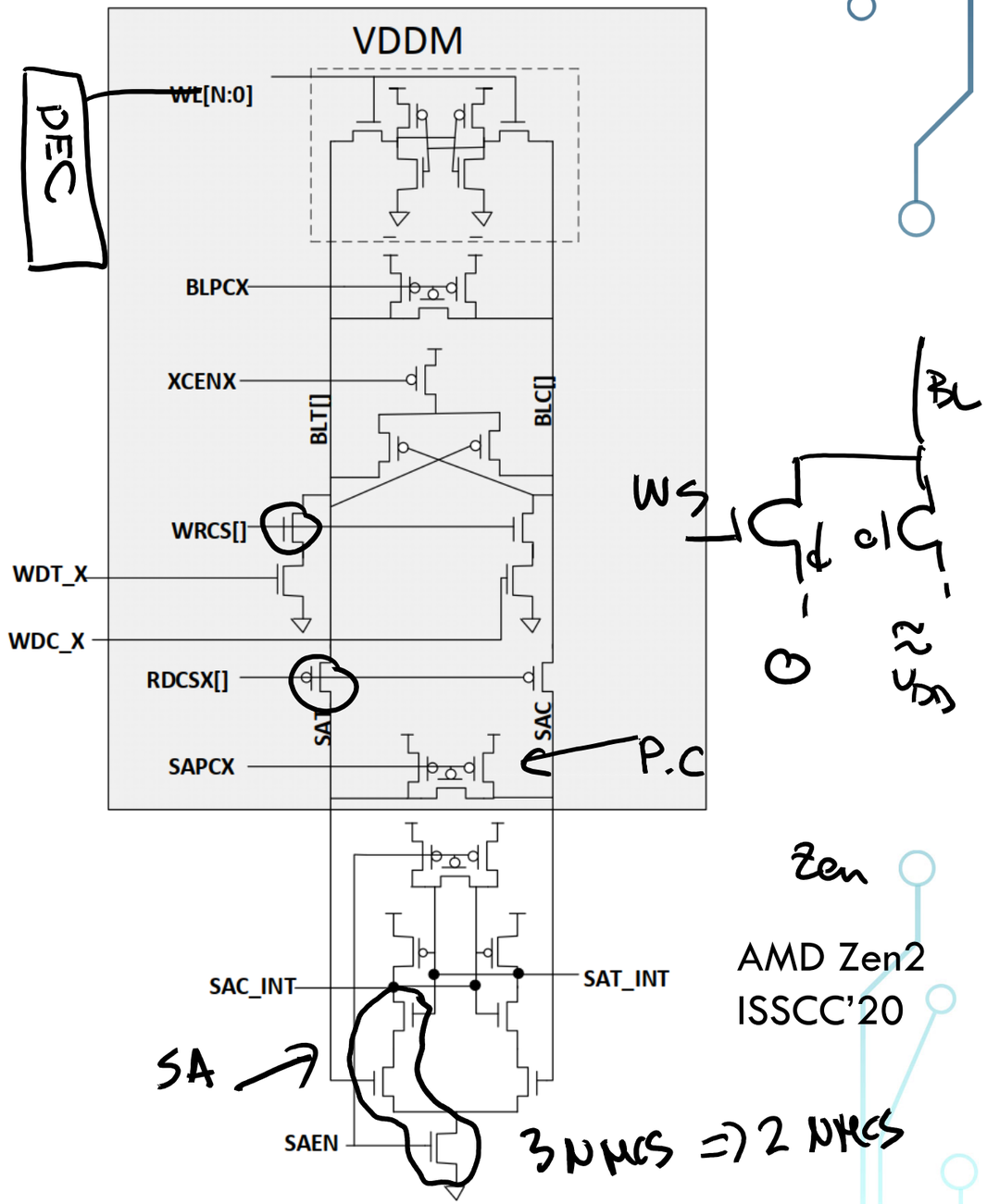
# Peripheral Circuits in SRAM

- Decoders (and pre-decoders)
- Column circuitry: read, write, multiplex, mask
- Write assist techniques
- Read assist techniques
- Redundancy
- BIST (Built-In Self-Test)
- ECC (Error correction)
- Power management



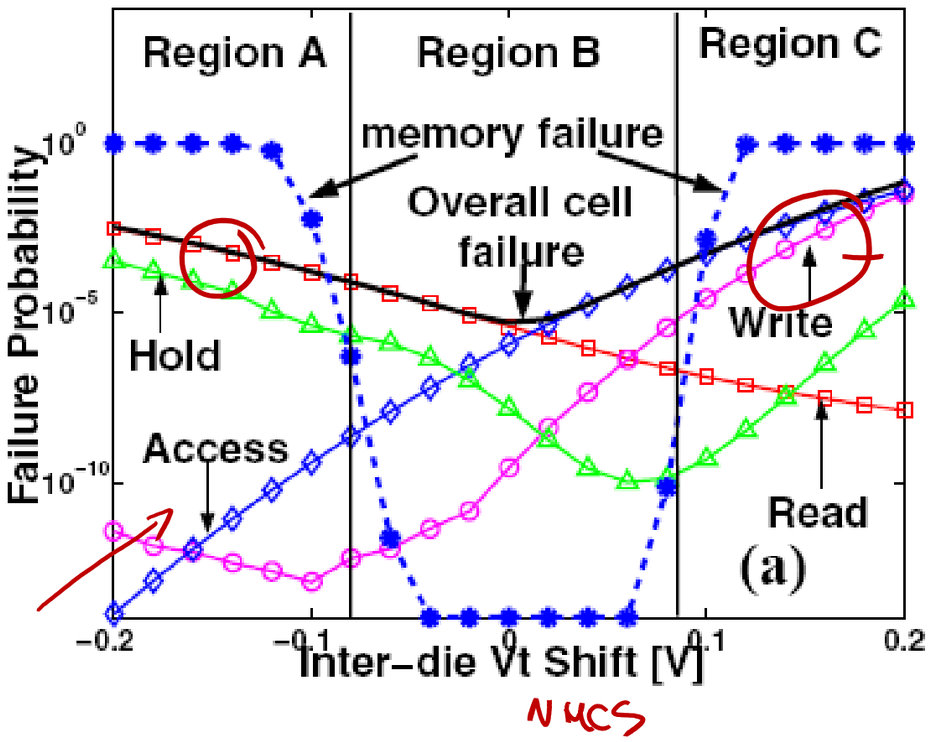
# SRAM Array

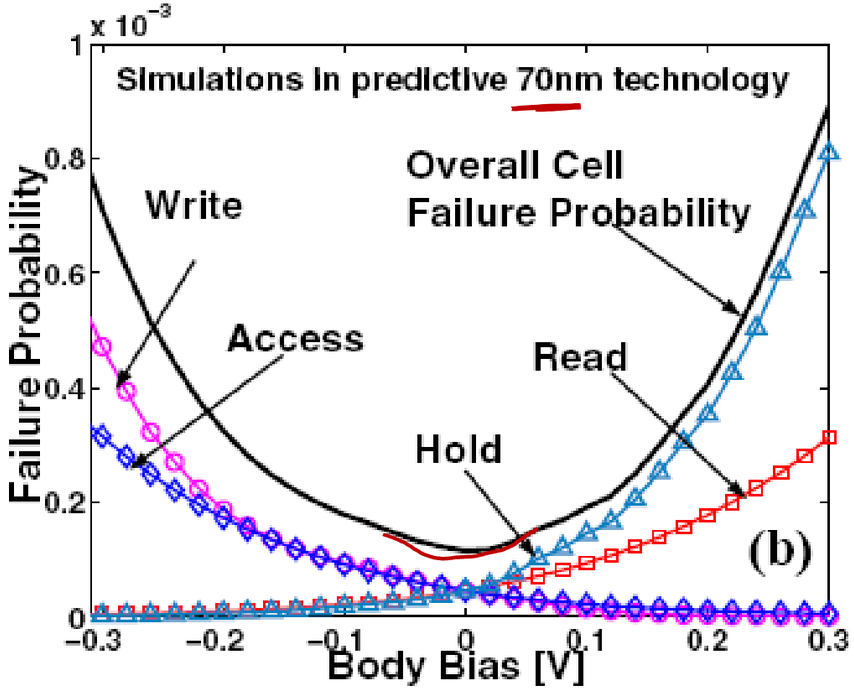

replace w/
SENSE AMP


VDDM
DEC
WL[N:0]
BLPCX
XCENX
BLT[]
BLC[]
WRCS[]
WDT_X
WDC_X
RDCSX[]
SAPCX
SAT
SAC
P.C
SAC_INT
SAT_INT
SA
SAEN
AMD Zen2
ISSCC'20
3 NMOS => 2 NMOS

# Array Adjustments

**Array back bias, to compensate for systematic variations**



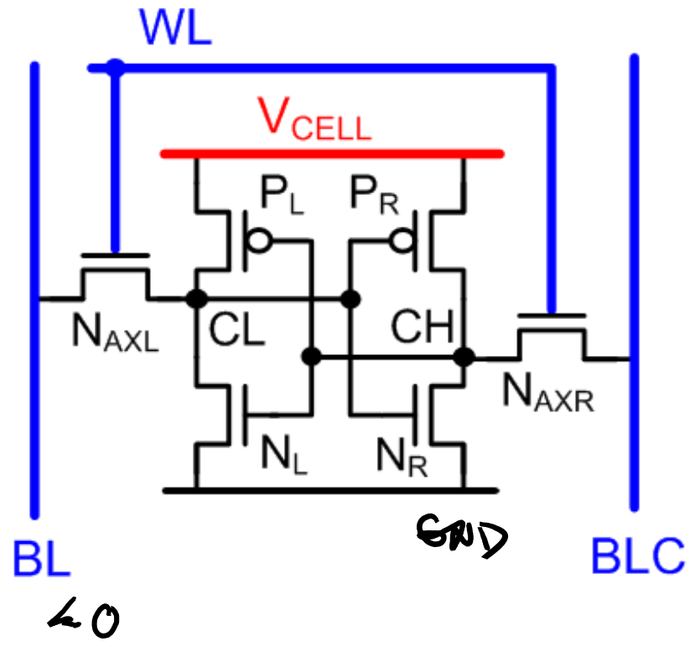

**May be useful in technologies with strong body effect**

S. Mukhopadhyay, *VLSI* 2006

# 4.F SRAM Assist Circuits

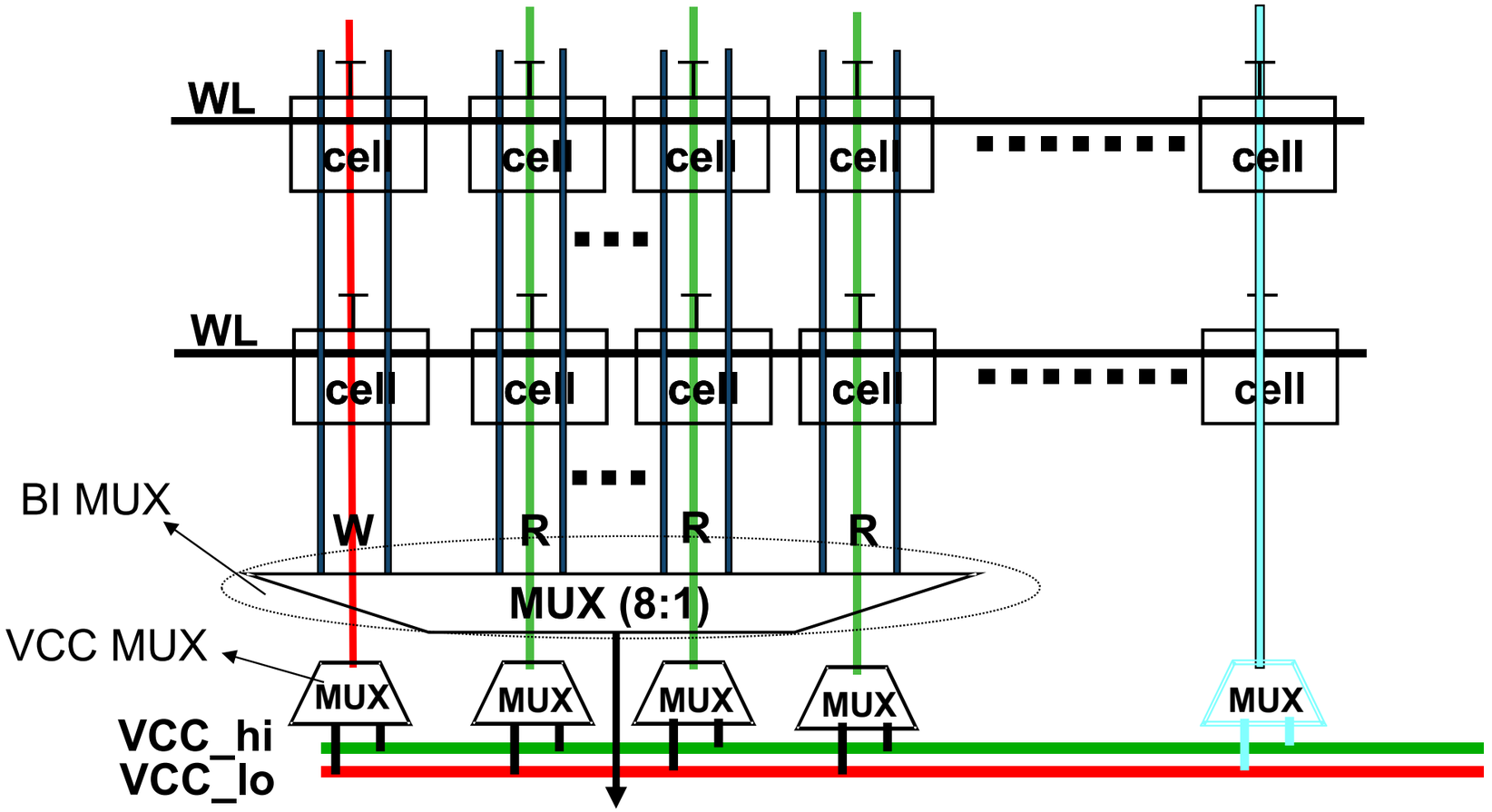
# Basic Ideas

- Dynamically change voltages




| | R/Col | Read | Write |
|---|---|---|---|
| WL | Row | $< V_{DD}$ | $> V_{DD}$ |
| BL | Col | $V_{DD}$ | $< GND$ |
| $V_{DD}$ ($V_{CELL}$) | Col | $V_{DD}$ | $< V_{DD}$ |
| GND | Row | $< 0$ | $0$ |

# Dynamic $V_{DD}$ Implementation




- VCC selection is along column direction to decouple the read & write

Zhang, ISSCC'05