EE241B : Advanced Digital Circuits

Lecture 15 – SRAM 3

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March 11, 2020, EE Times

Startup Ampere Attacks Intel's Strength: Startup Ampere Computing said it is shipping an Arm-based, 80-core processor, a chip it is positioning as the world's first "cloud-native" processor. Called the Altra, it was designed to process the workloads that are typically handled in the cloud, while also drawing significantly less power than the average CPU.

Announcements

- Quiz 2 today
- Project midterm reports due next Thursday (March 19)
- Assignment 3 due next week

- Reading - comprehensive (and optional)
  - Horiguchi, Itoh, *Nanoscale Memory Repair*, Springer, 2011.
  - Itoh, Horiguchi, Tanaka, *Ultra-Low Voltage Nano-Scale Memories*, Springer 2007.

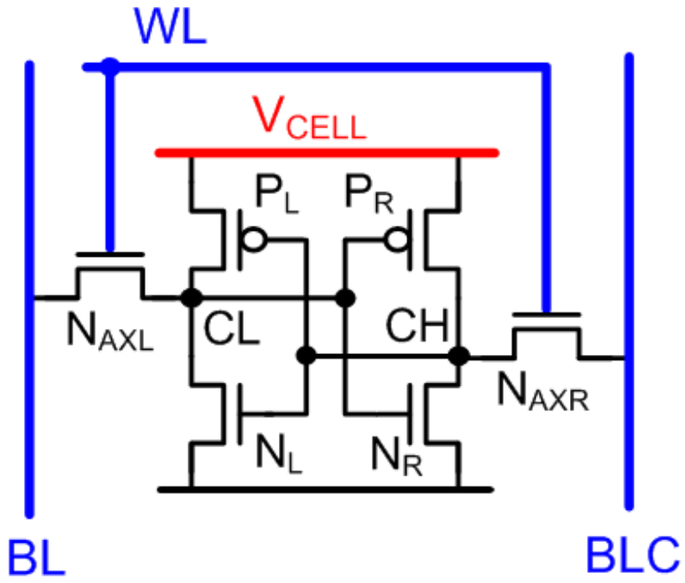
Outline

- Module 4
  - SRAM assist techniques
  - Sense amps

4.F SRAM Assist Circuits

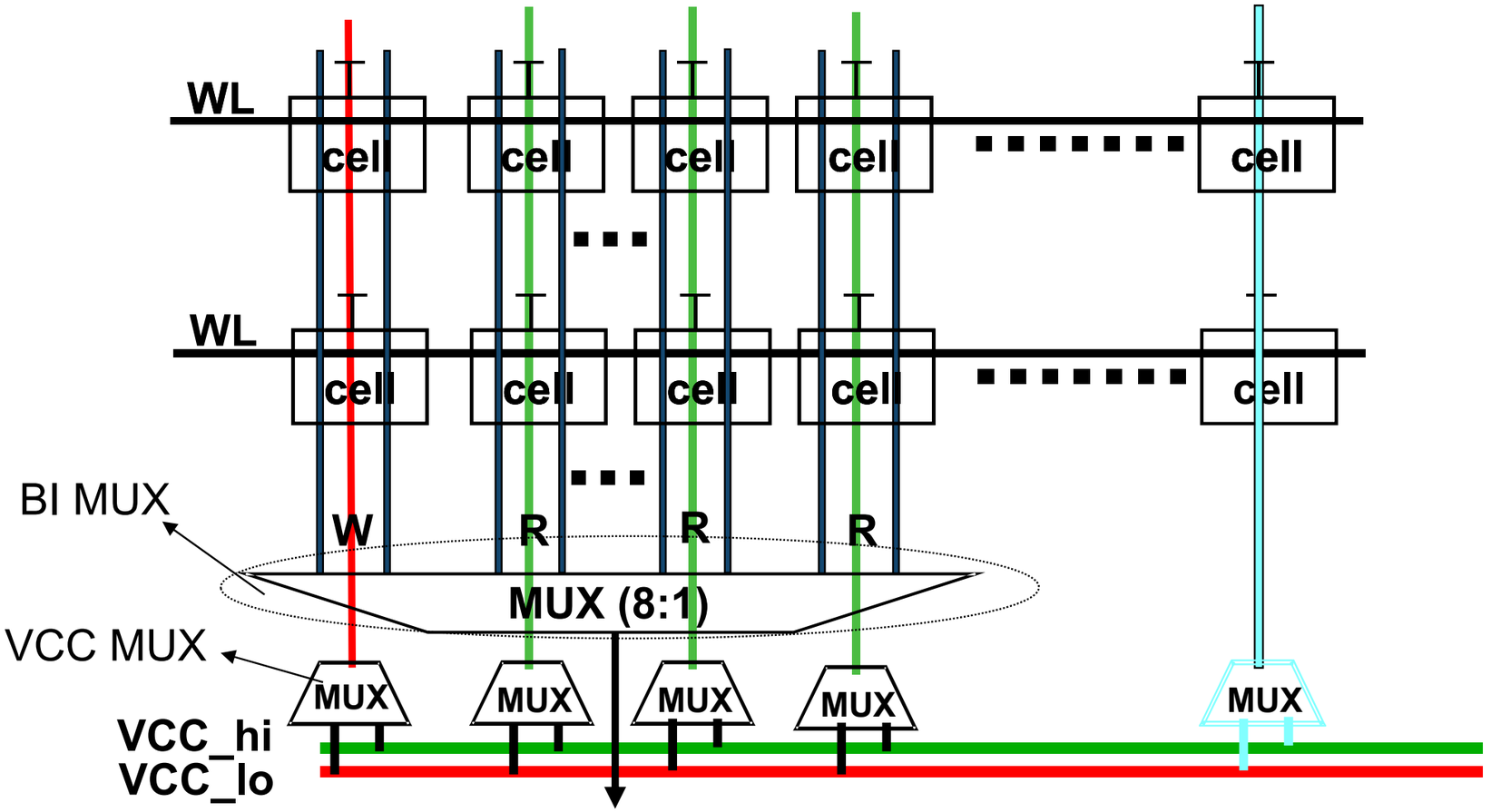
Basic Ideas

- Dynamically change voltages
- Negative BL helps with writing
- Lower VDD (V_{CELL}) helps with writing
- Higher WL helps with writing, lower hurts
- Lower WL helps with read, higher hurts



- Half-select condition: WL selected for write, but write operation is masked (BLs stay high)

Dynamic V_{DD} Implementation

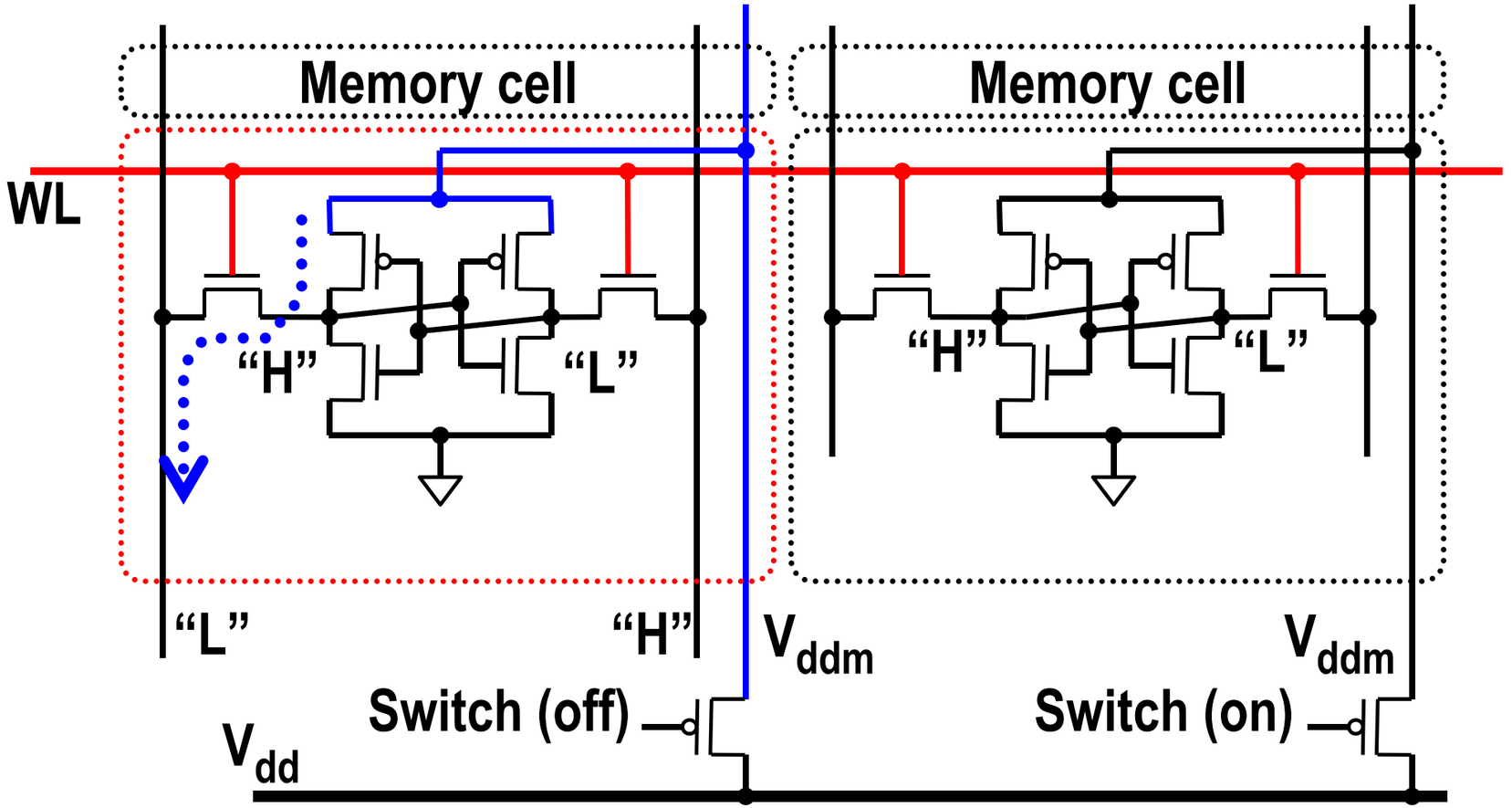


- VCC selection is along column direction to decouple the read & write

Zhang, ISSCC'05

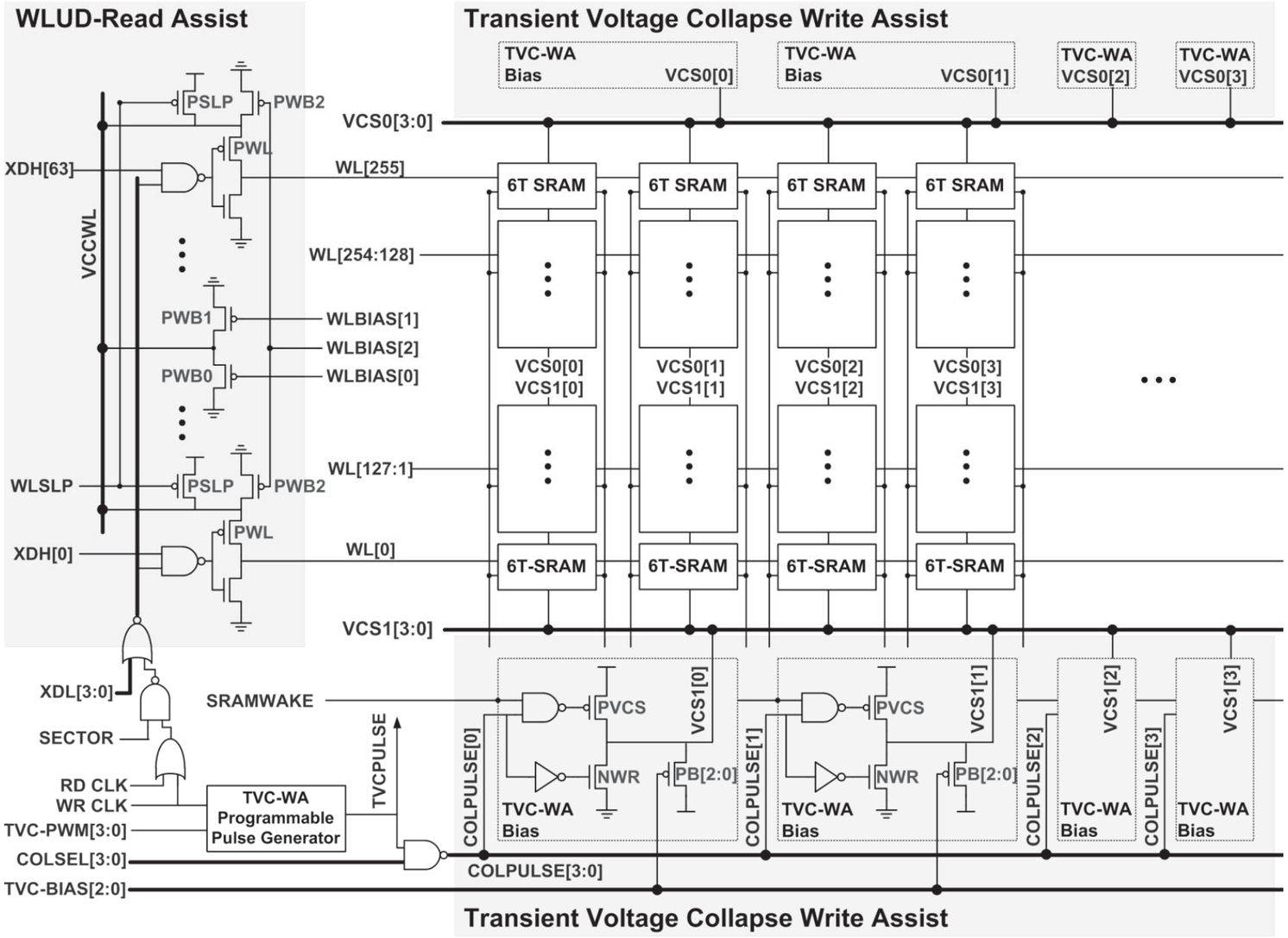
Floating VDD Technique

- W/o second supply



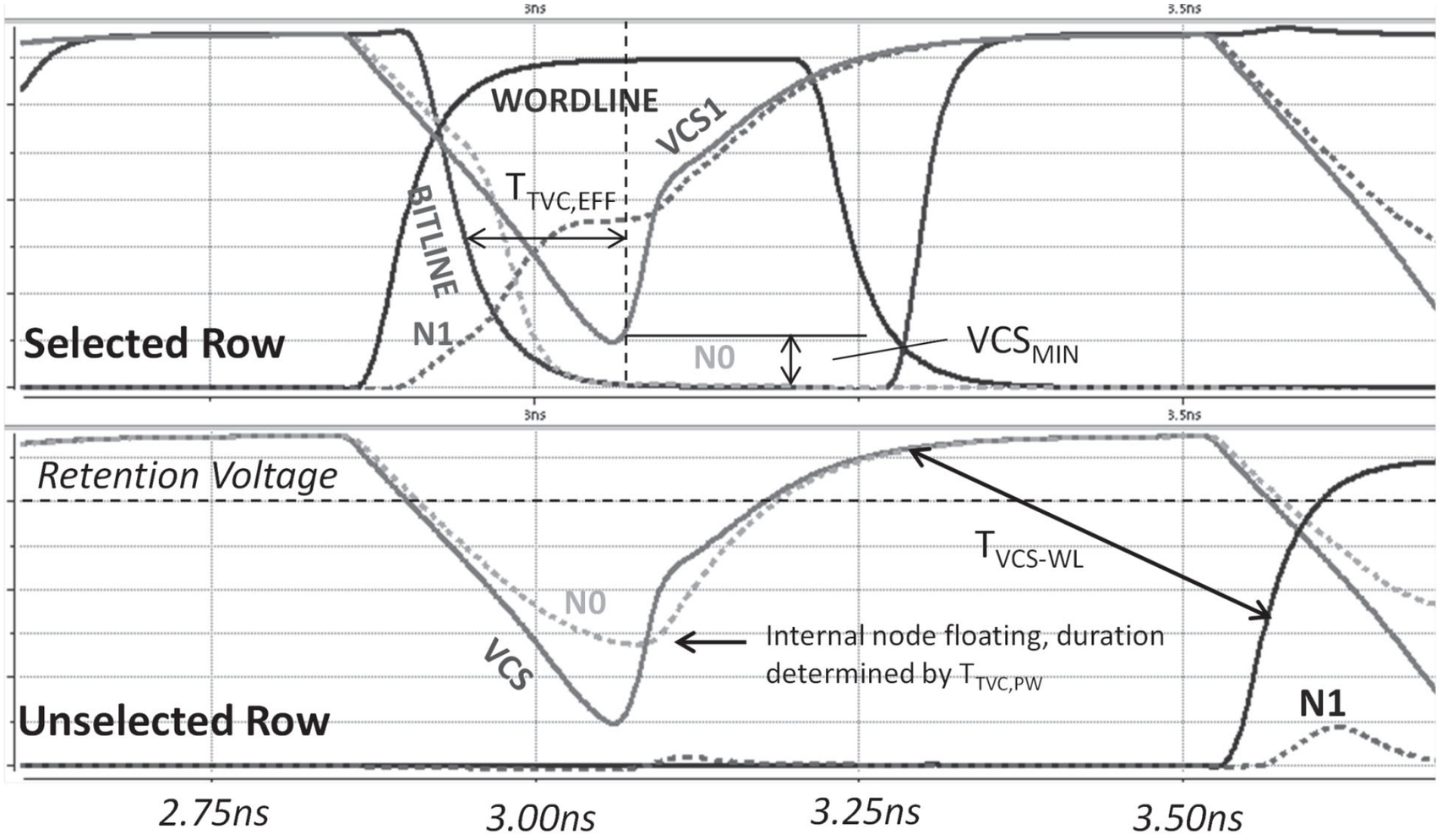
Yamaoka, ISSCC'04

Collapsing V_{DD} Technique



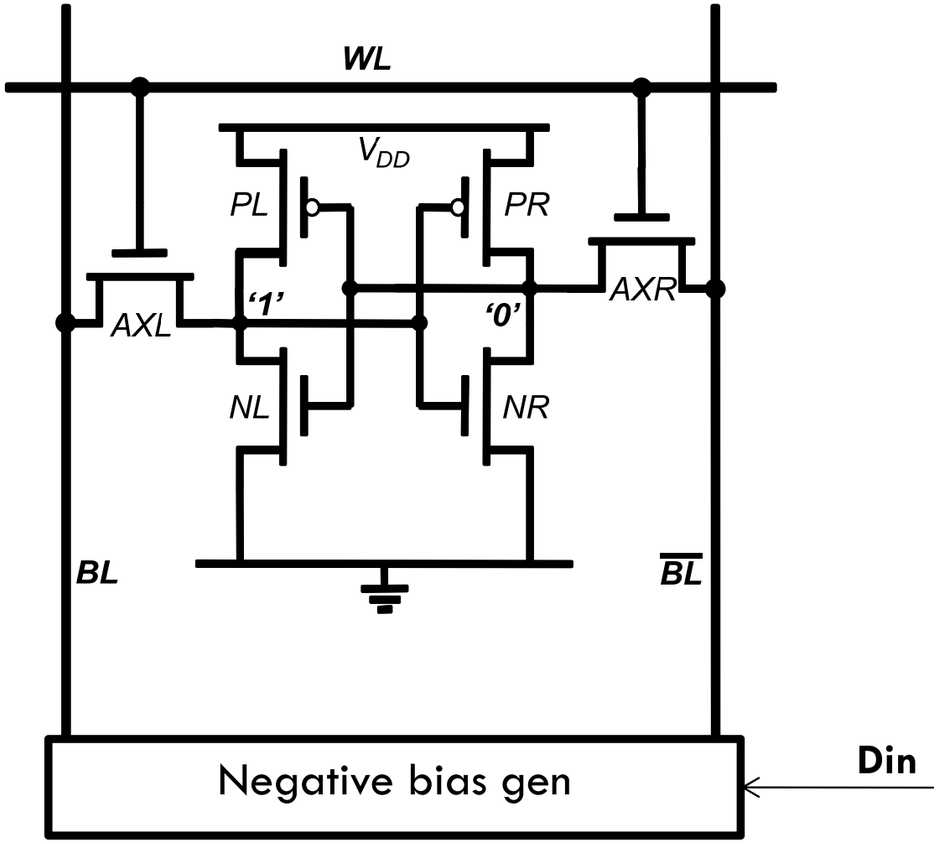
E. Karl, ISSCC'12

Collapsing V_{DD} Technique



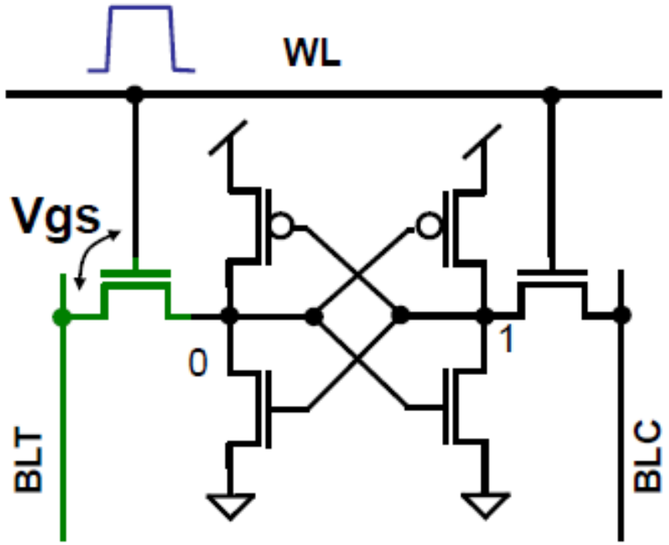
 E. Karl, ISSCC'12

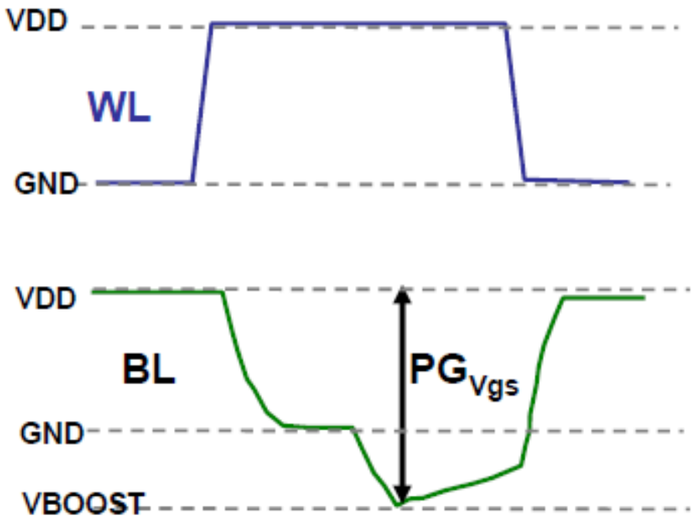
Negative BL



Nii, VLSI'08

Negative BL

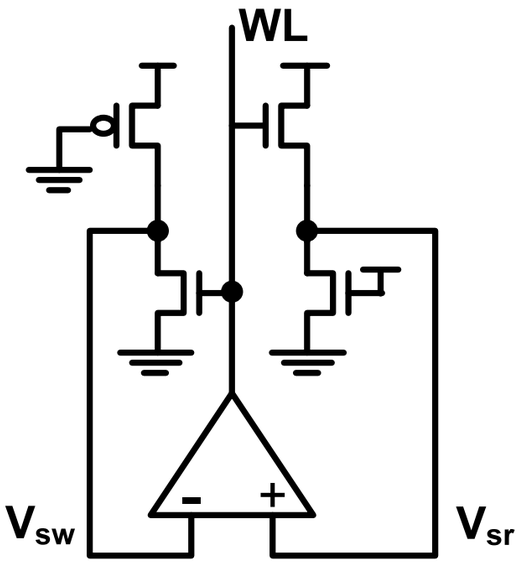




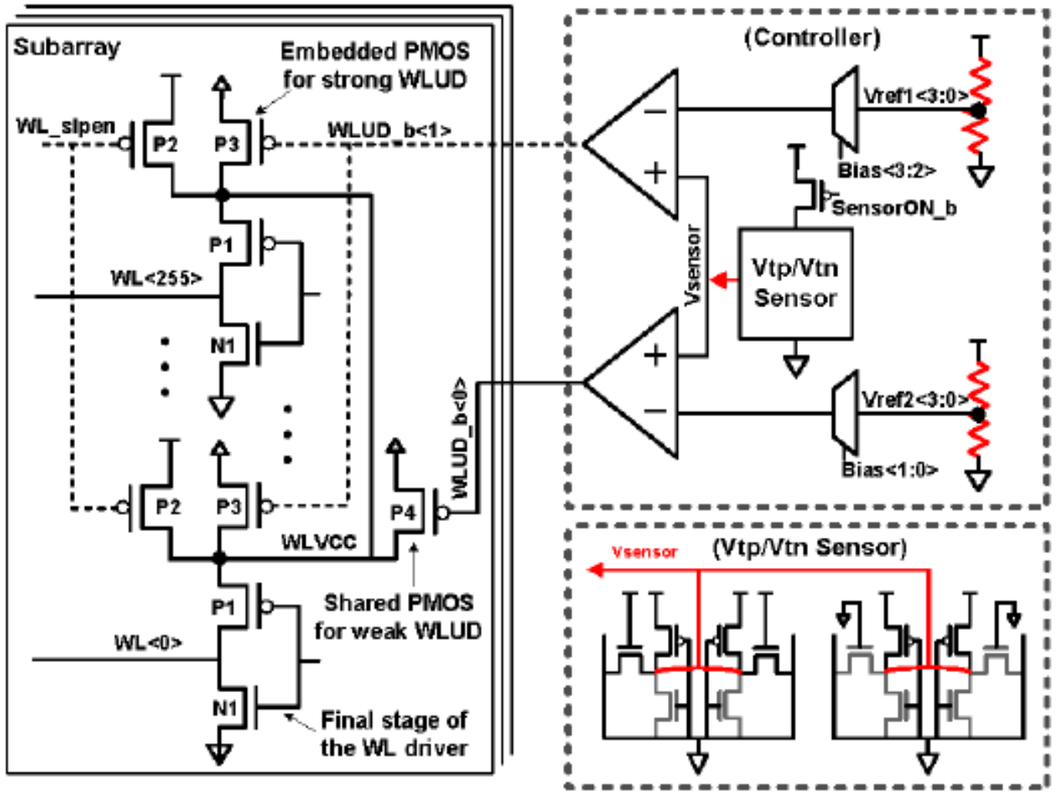
- Arsovski, ISSCC'11

WL Underdrive

- Sensing appropriate WL voltage

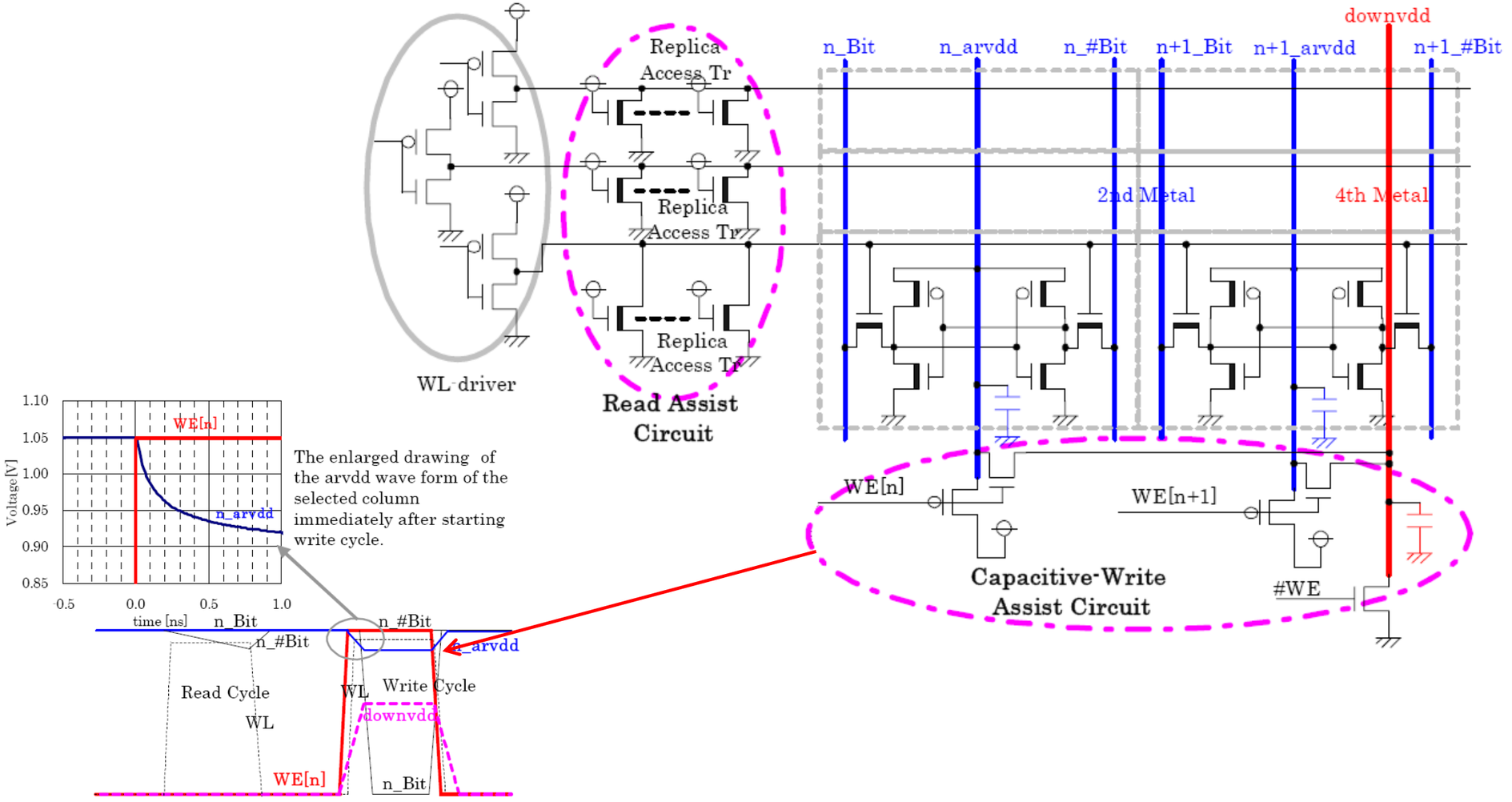


Carlson, CICC'08



Nho, ISSCC'10

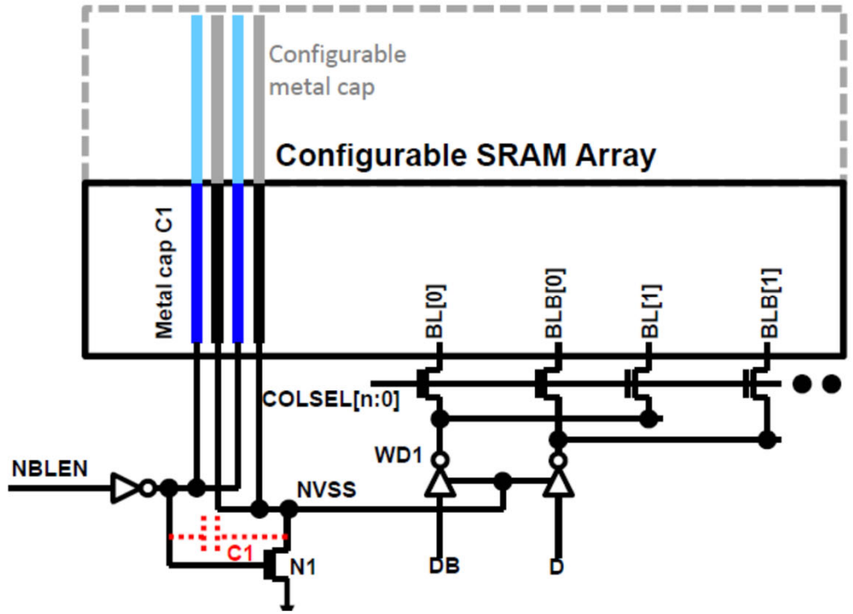
Capacitive Write Assist + WL Underdrive



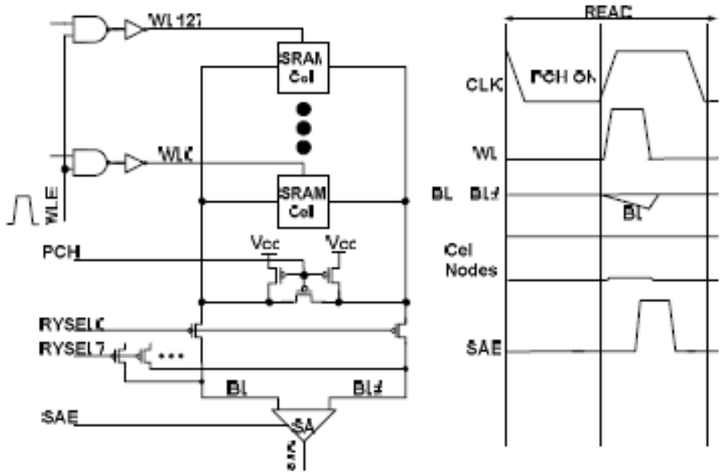
S. Ohbayashi, *VLSI* 2006

Capacitive Write Assist (ISSCC'20)

- 5nm SRAM [J. Chang, ISSCC'20]



Pulsed WL/BL



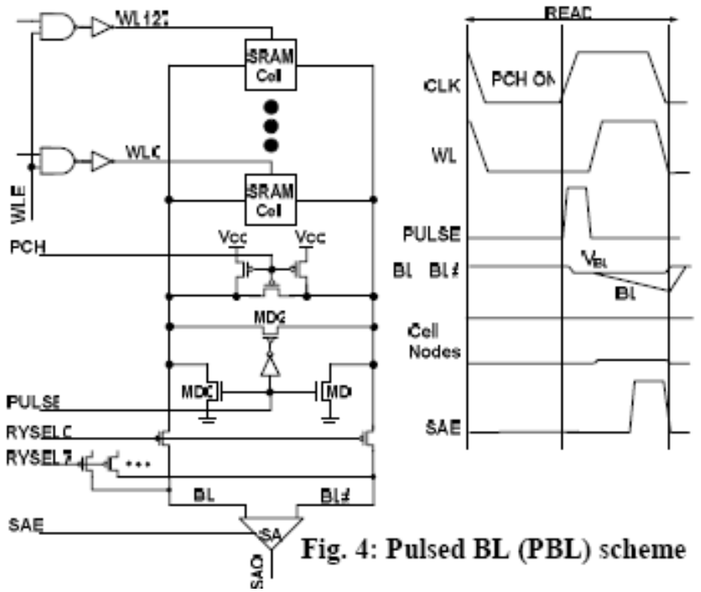


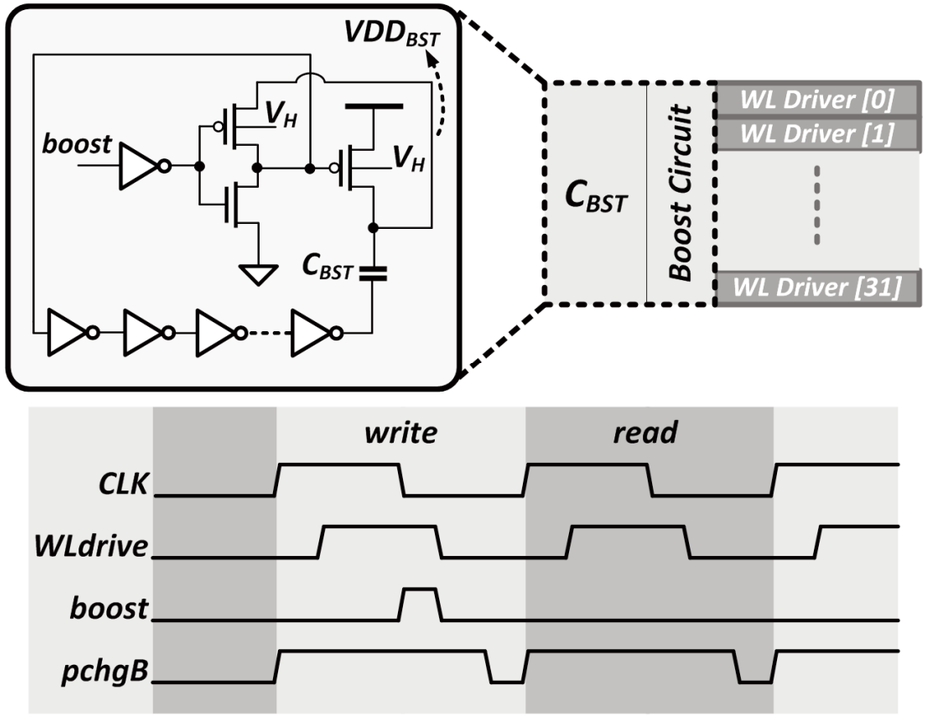
Fig. 4: Pulsed BL (PBL) scheme

M.Khellah, *VLSI* 2006

Pulsing WL

Wordline pulse shape

Generating boost



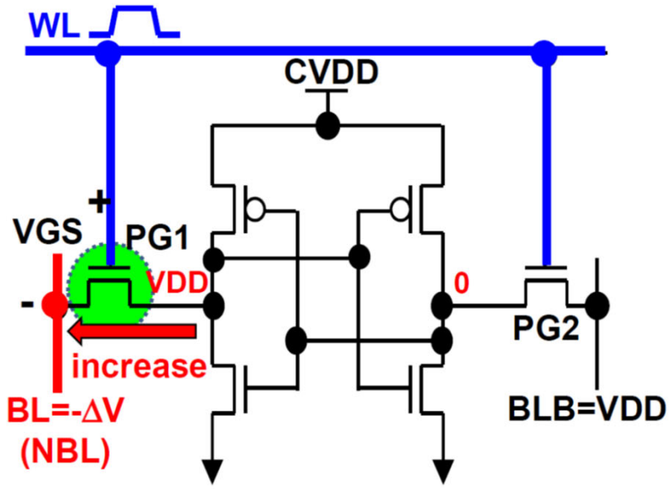
- Sinangil, ISSCC'2011

ISSCC'17 – 7nm SRAM

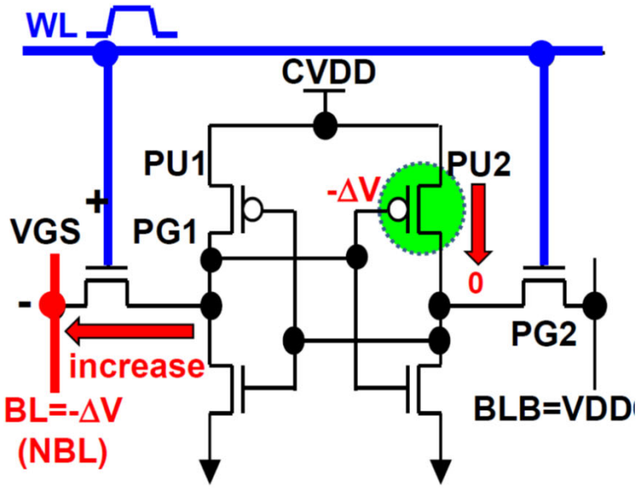
Write Assist Techniques

- Negative Bit-Line (NBL):
  - increase PG1 and PU2 strength
- Improve both contention and recovery

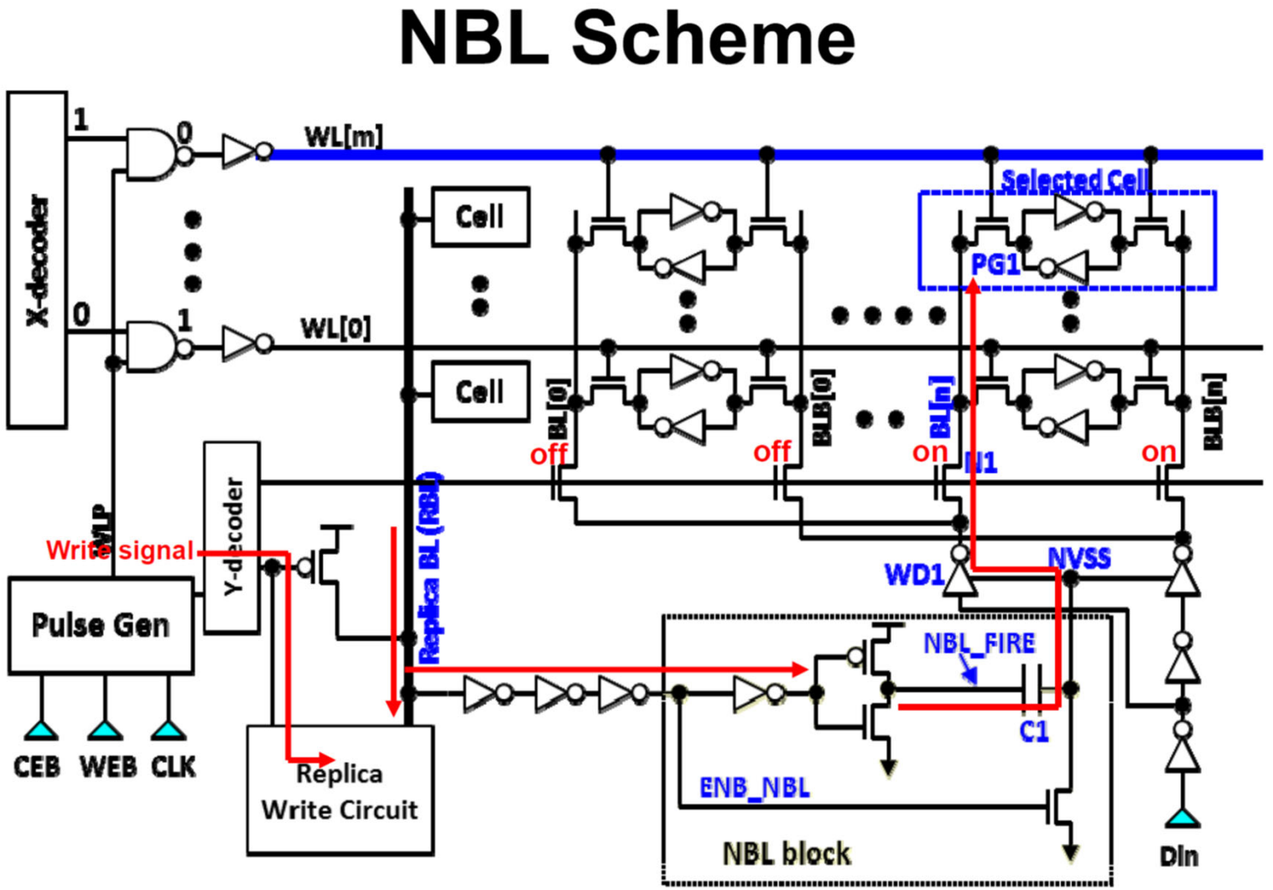
NBL: increase PG1 strength



NBL: increase PU2 strength

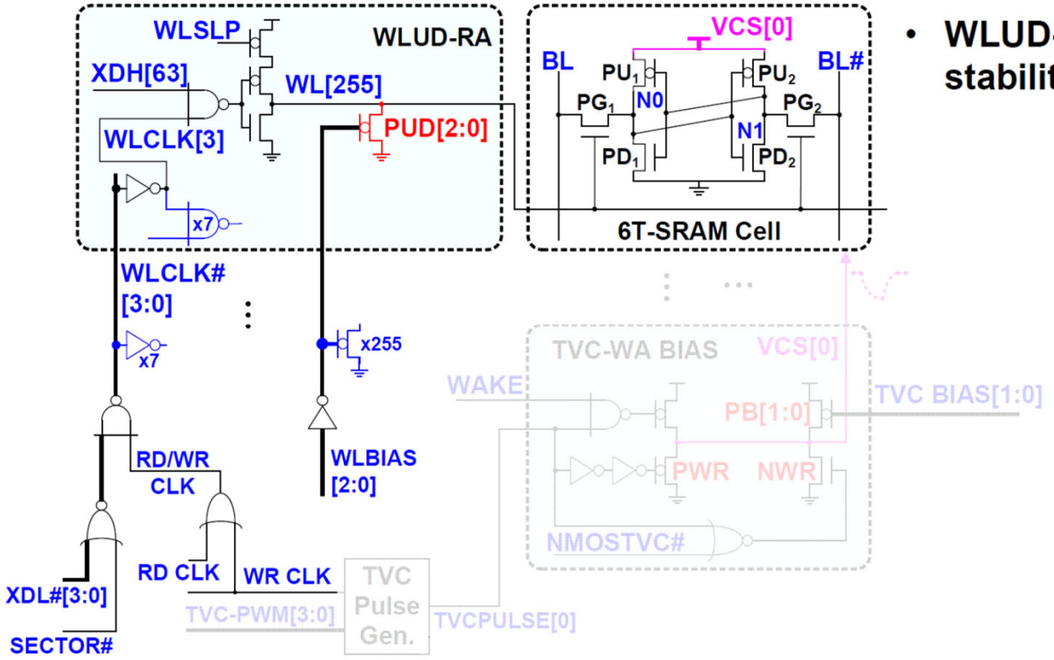


ISSCC'17 – 7 nm SRAM



ISSCC'18 - 10nm Read Assist

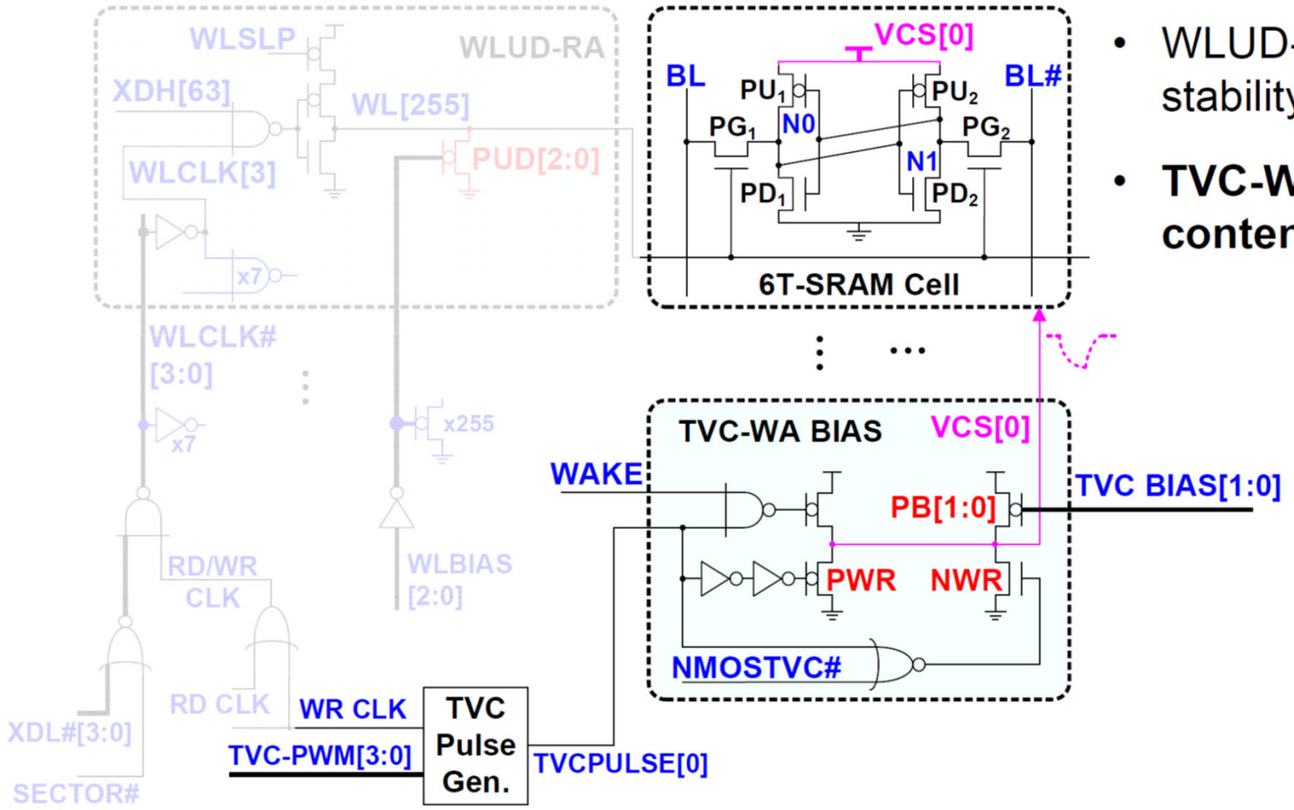
- Wordline underdrive



- **WLUD-RA for improved stability margin (1.5% area)**

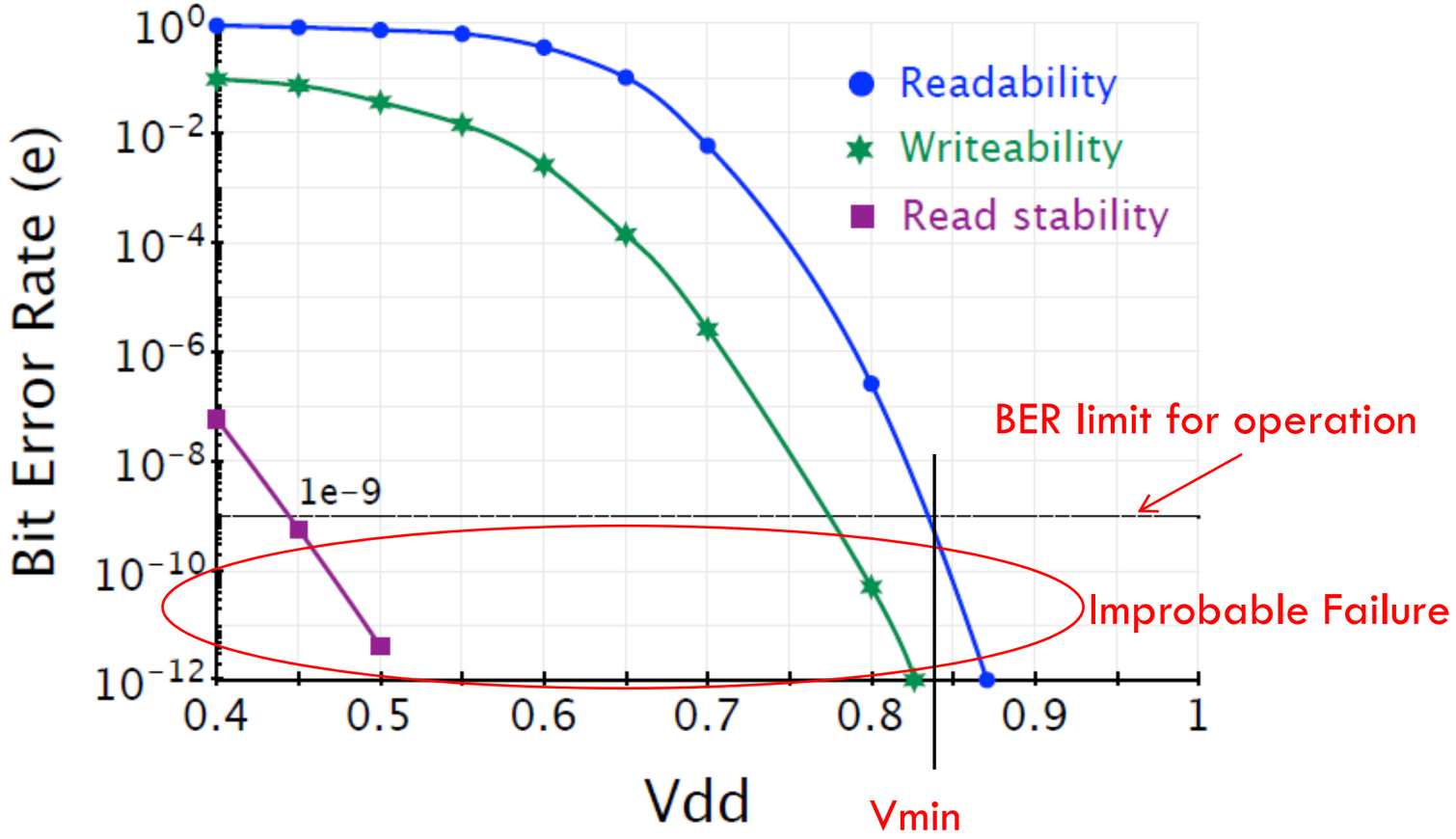
ISSCC'18 - 10nm SRAM

- Transient voltage collapse



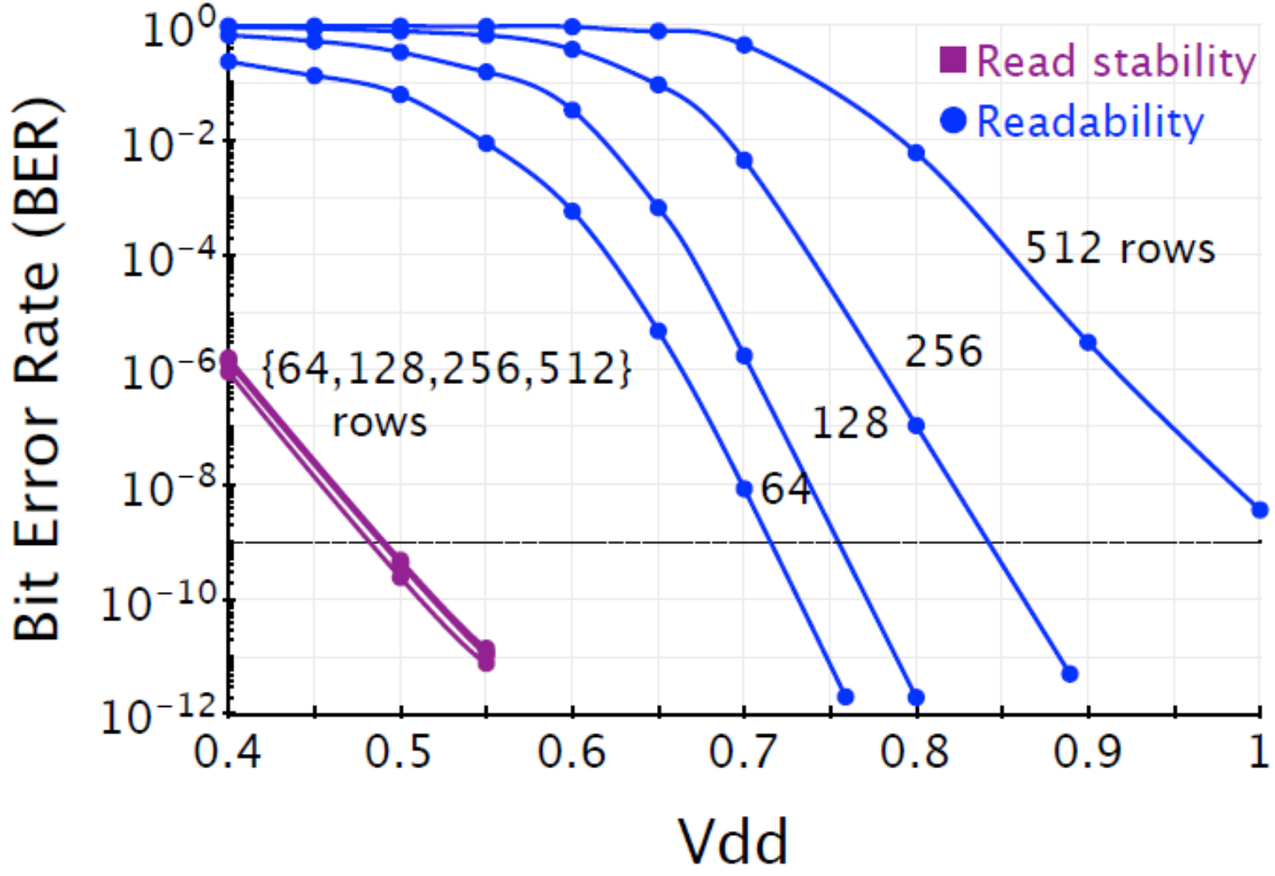
- WLUD-RA for improved stability margin (1.5% area)
- **TVC-WA to reduce PU:PG contention (3.3% area)**

SRAM Failure Rates

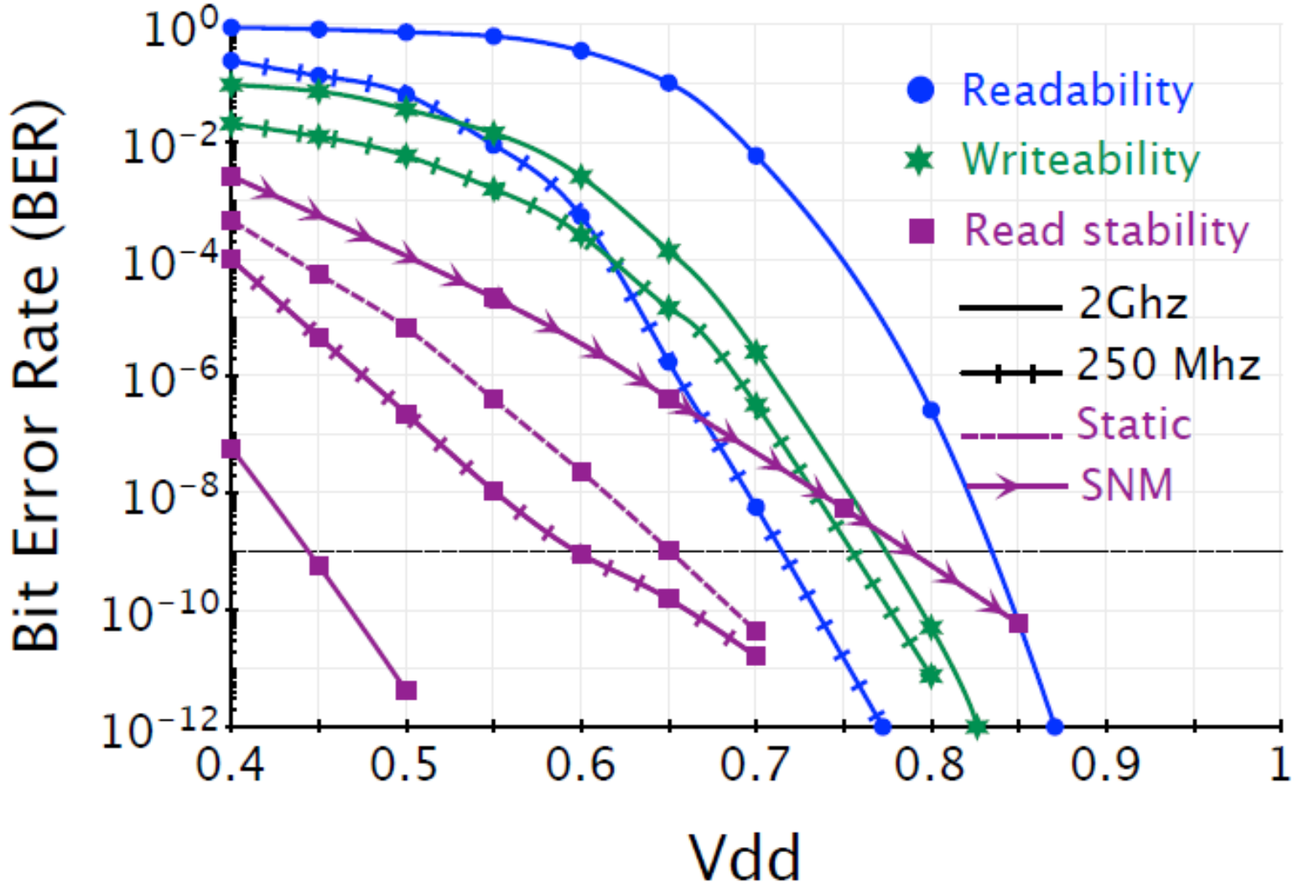


Readability, writeability, and read-stability failure rates for a 28nm 6T SRAM bitcell

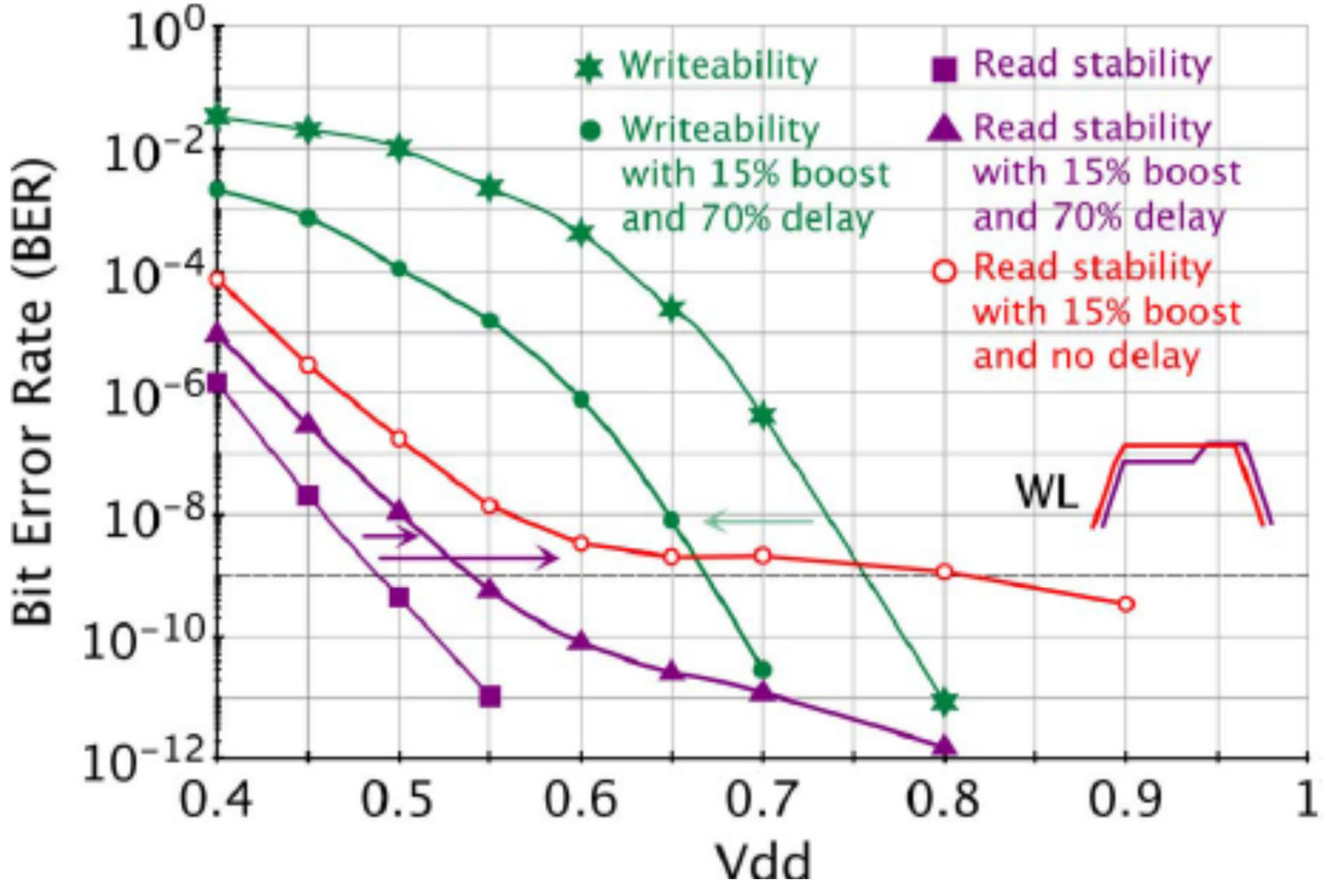
Effect of bitline capacitance



Effect of clock period



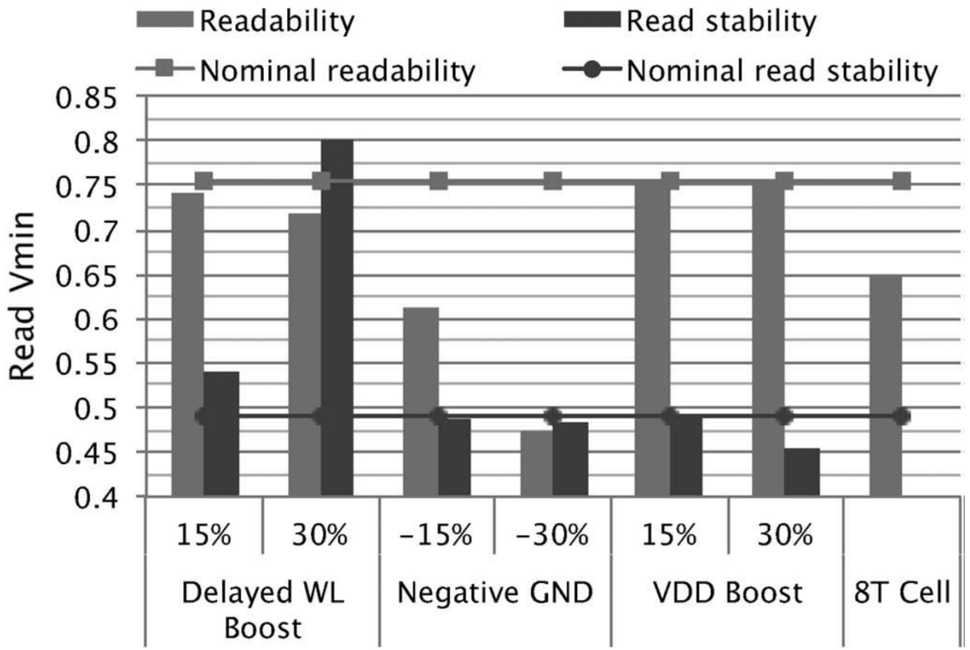
Effect of Assist Techniques

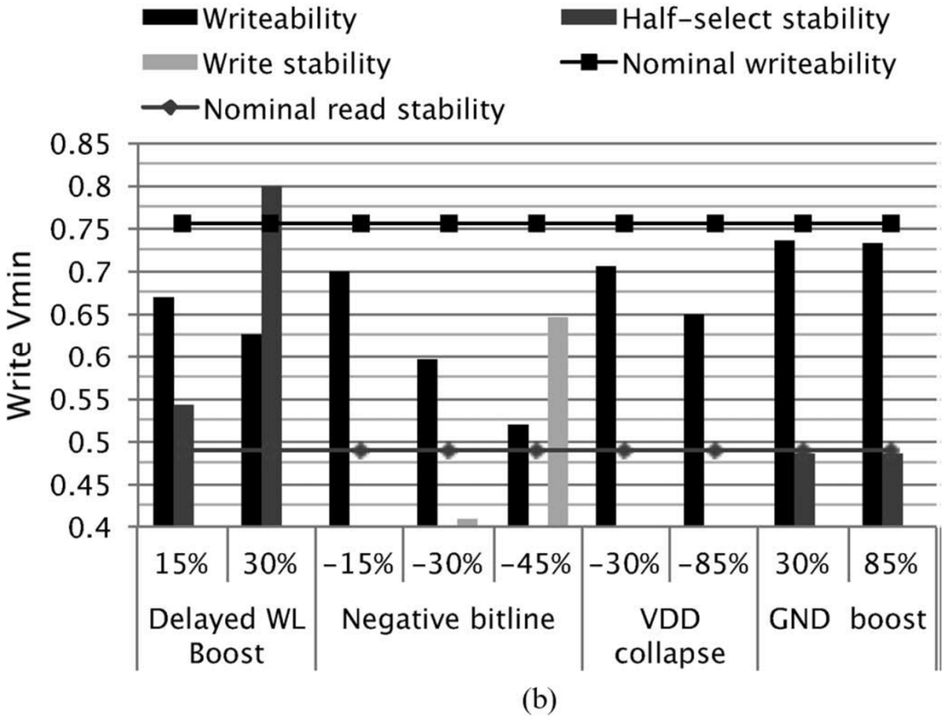


Zimmer, TCAS-I'12

How Do They Stack Up?

- 28nm bulk CMOS

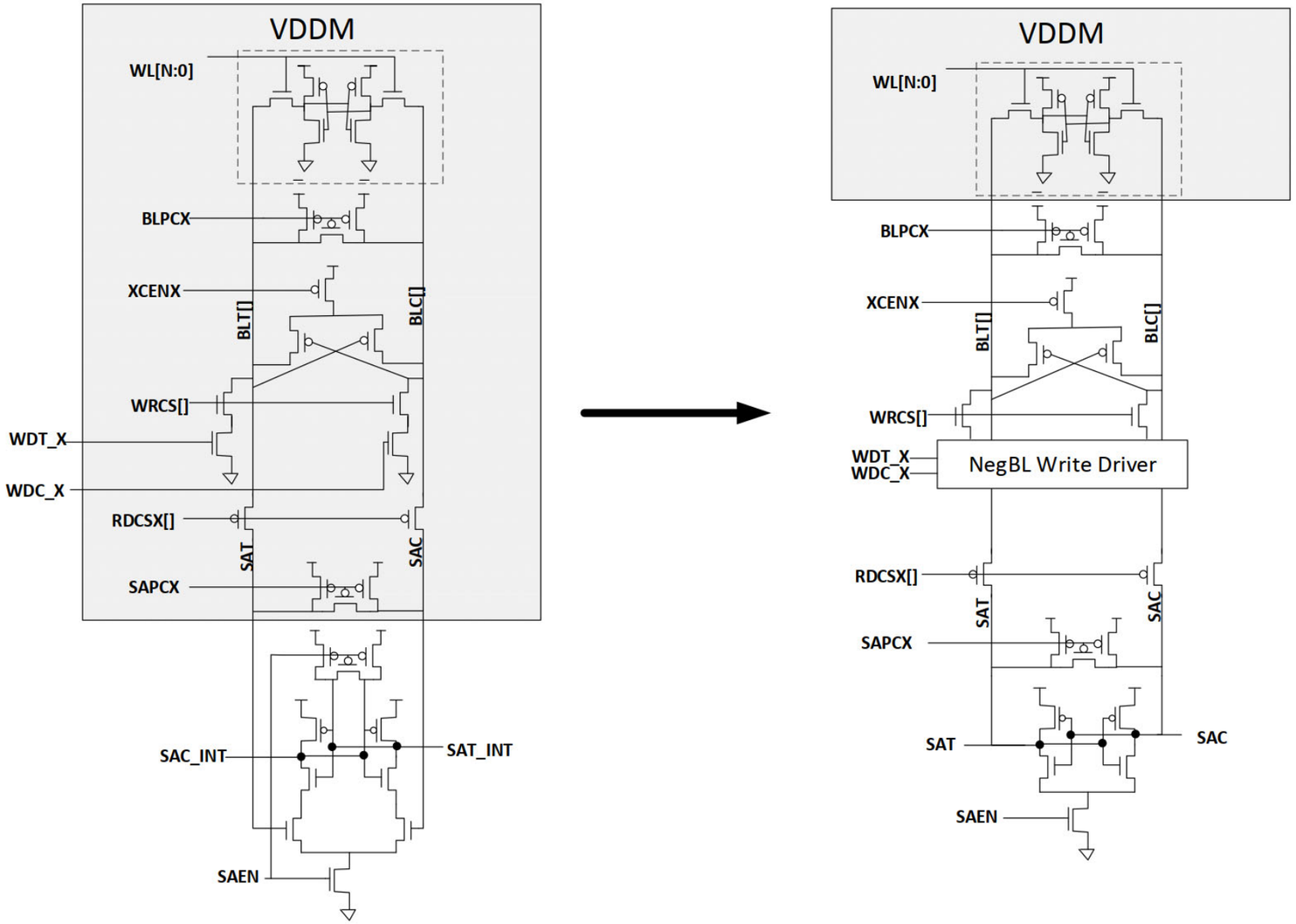




(b)

SRAM In Practice

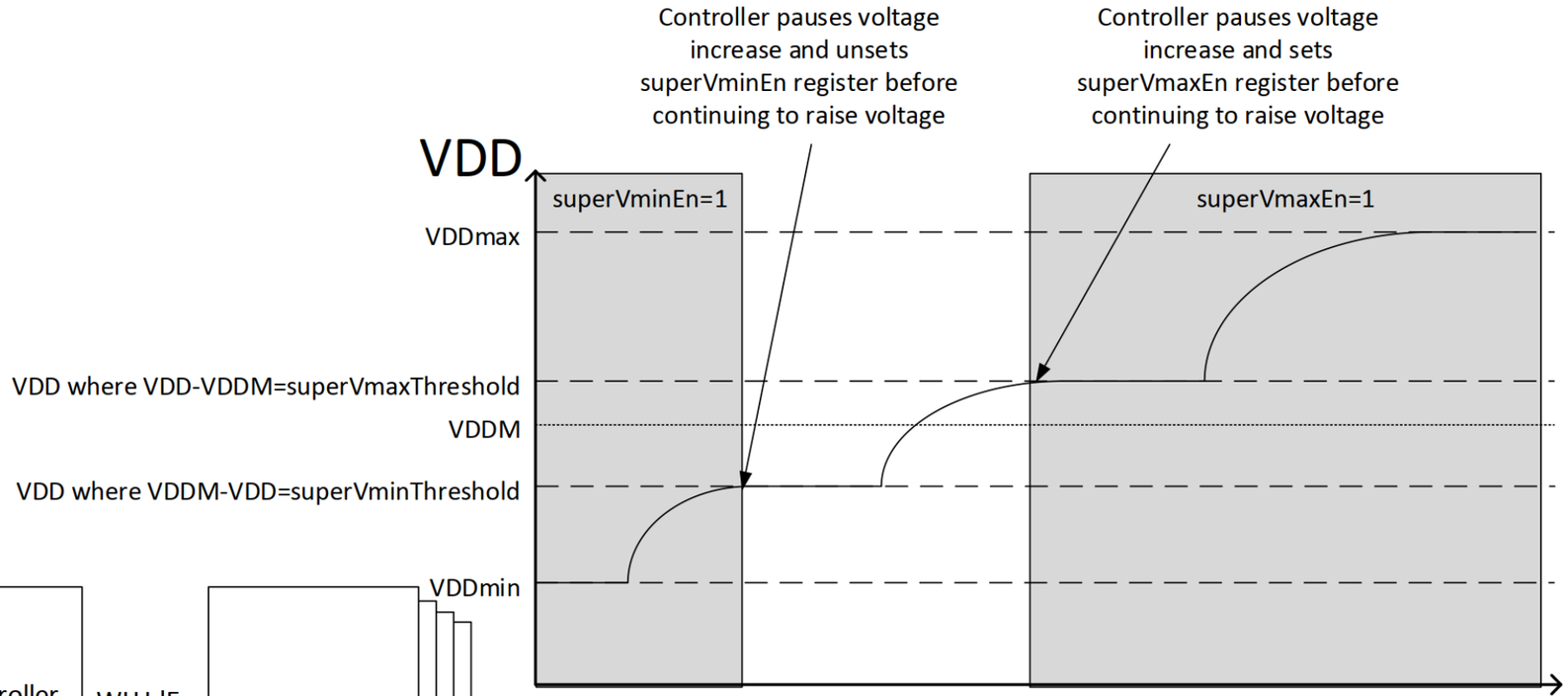
- 7nm AMD Zen2 (Singh, ISSCC'20)

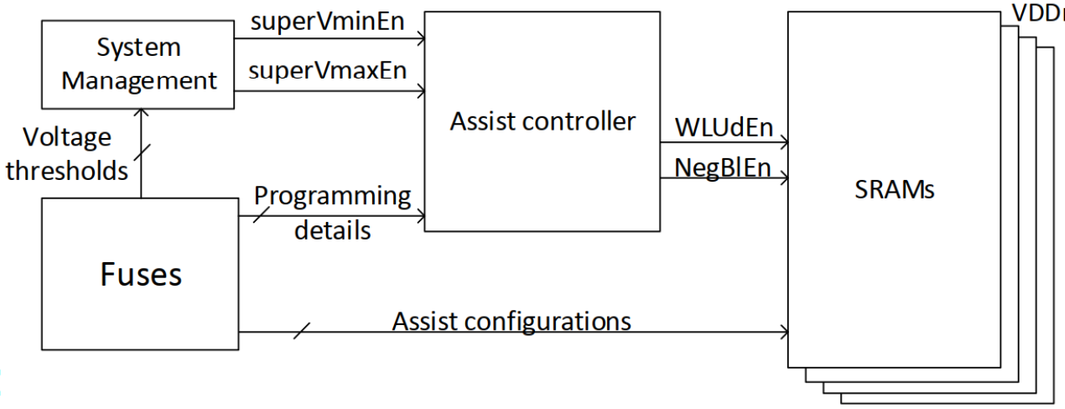


SRAM In Practice

- 7nm AMD Zen2 (Singh, ISSCC'20)

  - Moving bitline precharge to VDD creates both bitcell stability and writeability challenges
  - High level of configurability allows for silicon flexibility





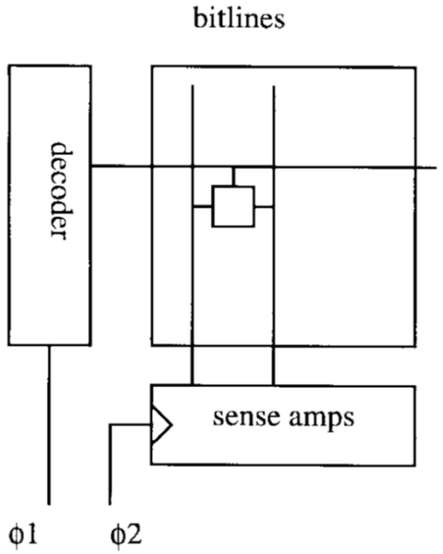
4.G Sense Amps

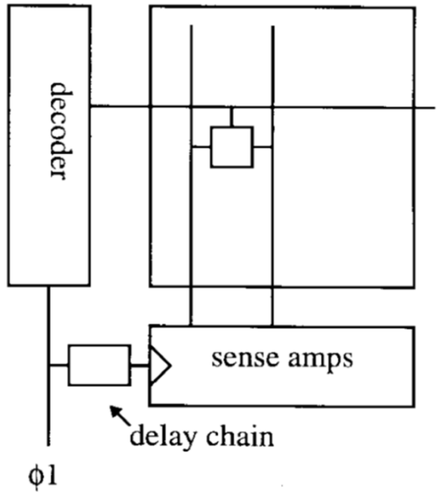
SRAM Periphery Design

- SRAM periphery:
  - Decoders (covered in EECS251A)
  - Bitline design and sense-amps

Sense-Amp Triggering

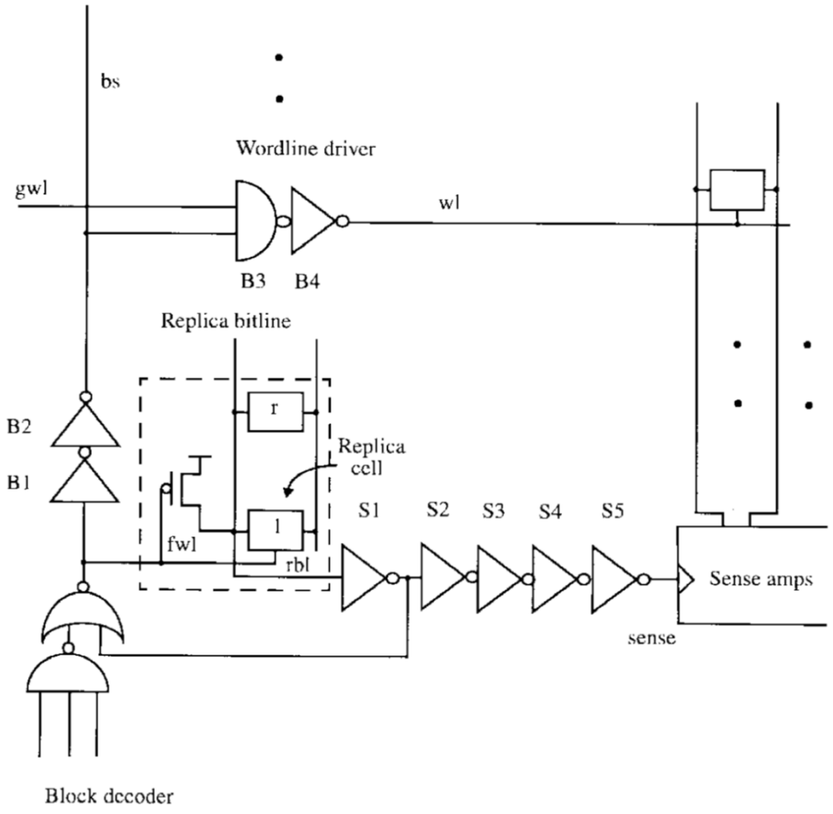
- Some older techniques

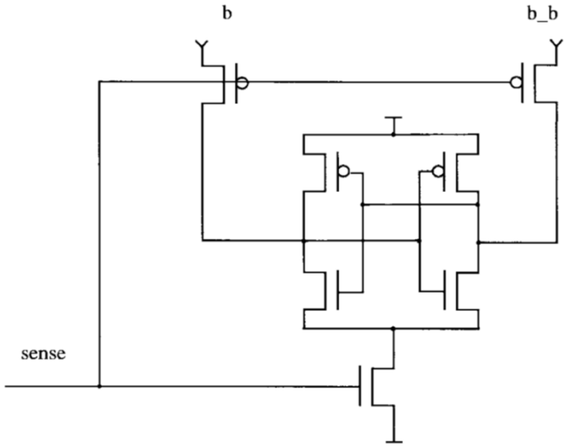


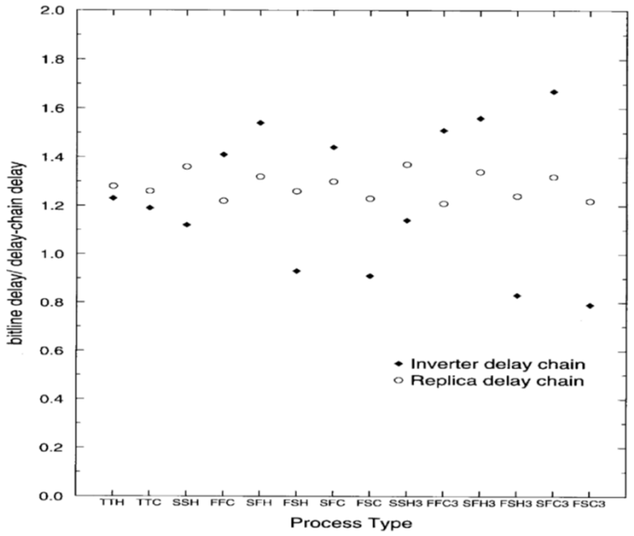


Sense-Amp Triggering

- Replica bitline



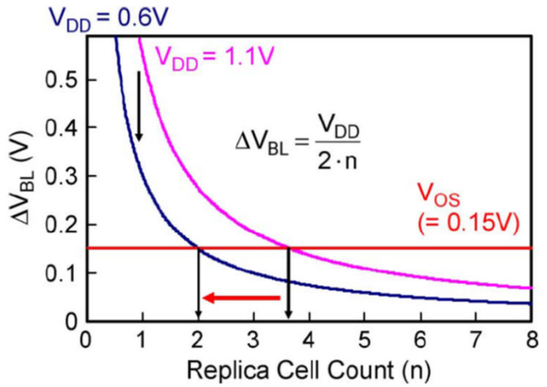




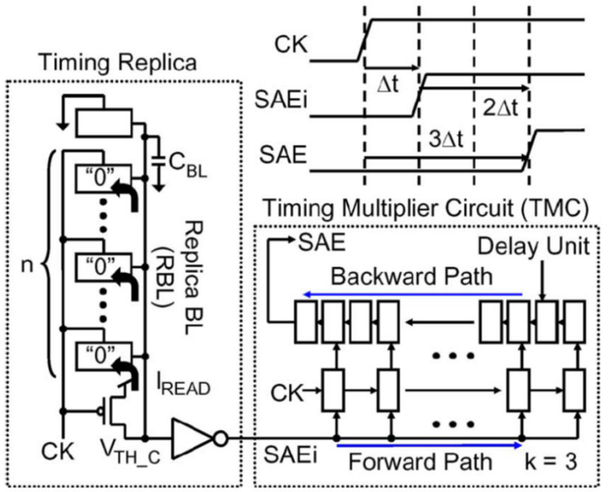
Amrutur, JSSC'98

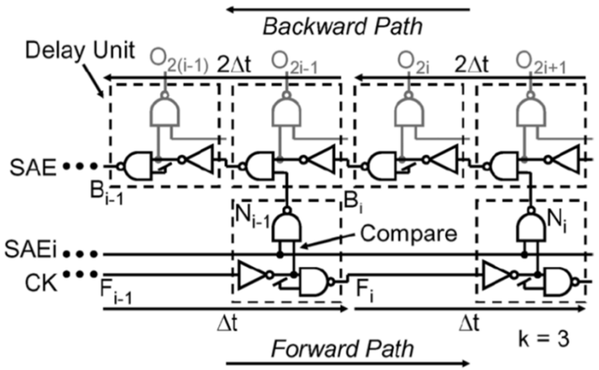
Multiplicative Replica Bitline

- Conventional replica



- Multiplictive replica





Niki, JSSC'11

Next Lecture

- Redundancy, ECC
- Alternatives to 6T SRAM