EE241B : Advanced Digital Circuits

Lecture 16 – SRAM Options

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March 16, 2020, Check: https://www.projectopenair.org/

Announcements

- Project midterm reports postponed until Tuesday, March 31
- Assignment 3 postponed until Thursday, April 2.
- Reading – req'd
  - Markovic et al, Methods for true energy-performance optimization, IEEE Journal of Solid-State Circuits, vol. 39, no.8, pp. 1281-1293, August 2004.
  - Chandrakasan and Brodersen, Low power CMOS digital design, IEEE Journal of Solid-State Circuits, vol. 27, no. 4, pp. 473-484, Apr. 1995.
- Recommended
  - Zyuban et al, Integrated Analysis of Power and Performance for Pipelined Microprocessors, IEEE Trans. on Computers, vol.53, no. 8, August 2004.

Proc IEEE

Outline

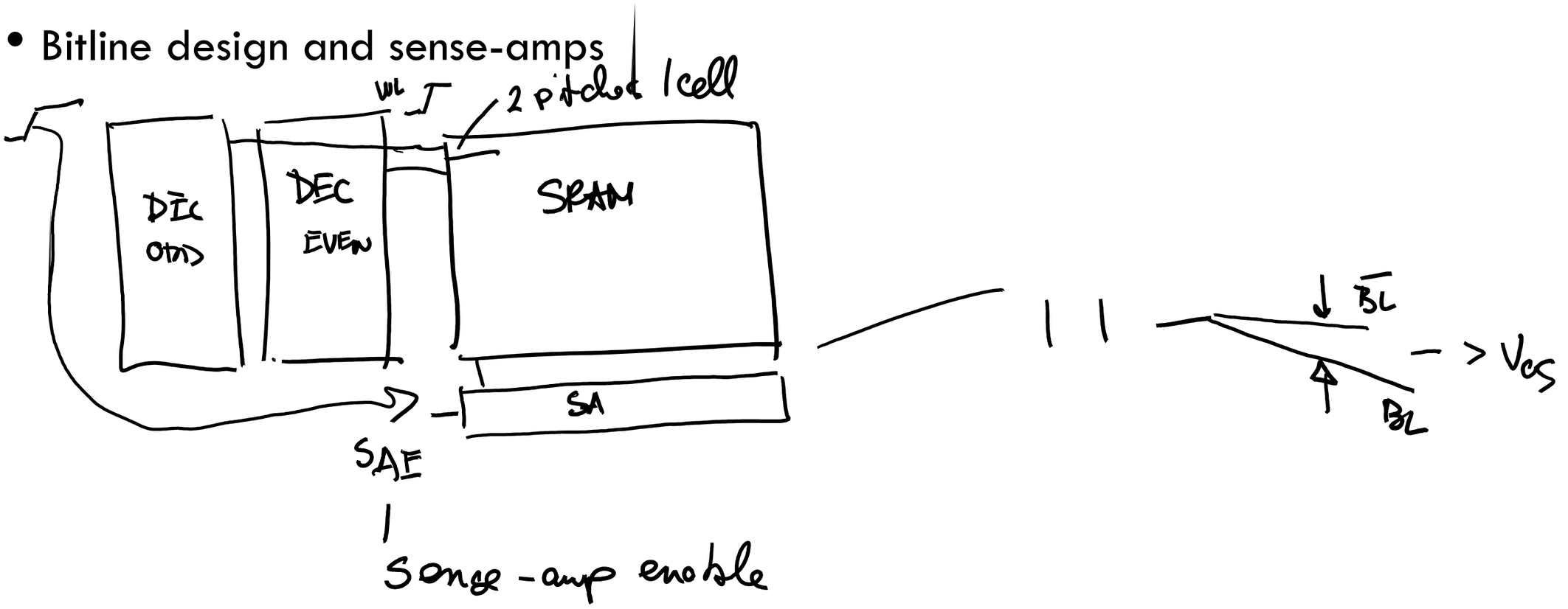
- Module 4
  - Sense amp timing
  - Redundancy and ECC

SRAM alternatives

4.G Sense-Amp Timing

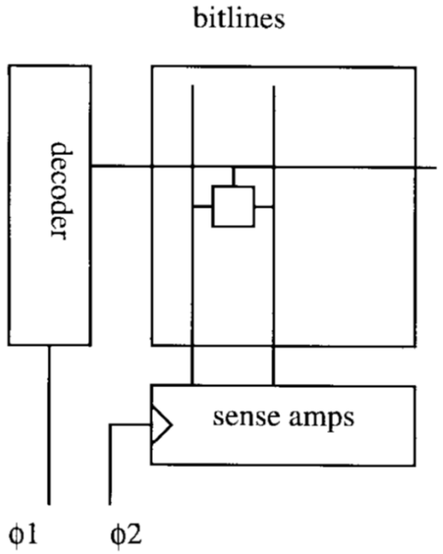
SRAM Periphery Design

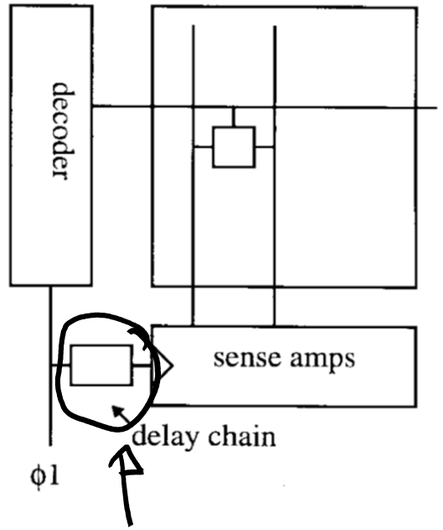
- SRAM periphery:
  - Decoders (covered in EECS251A)
  - Bitline design and sense-amps

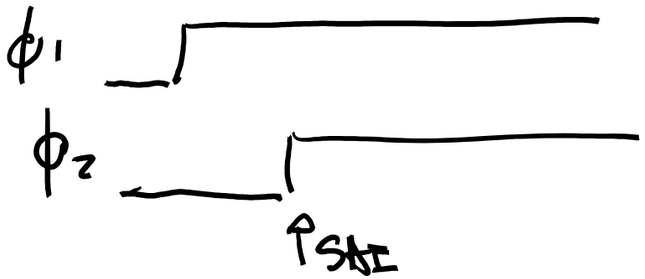


Sense-Amp Triggering

- Some older techniques

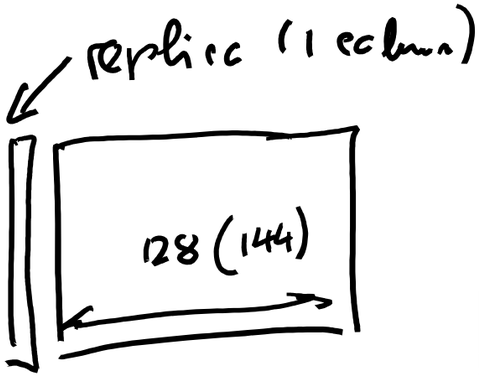


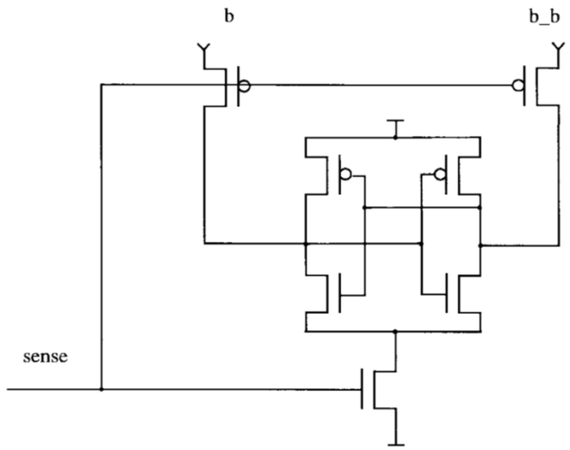


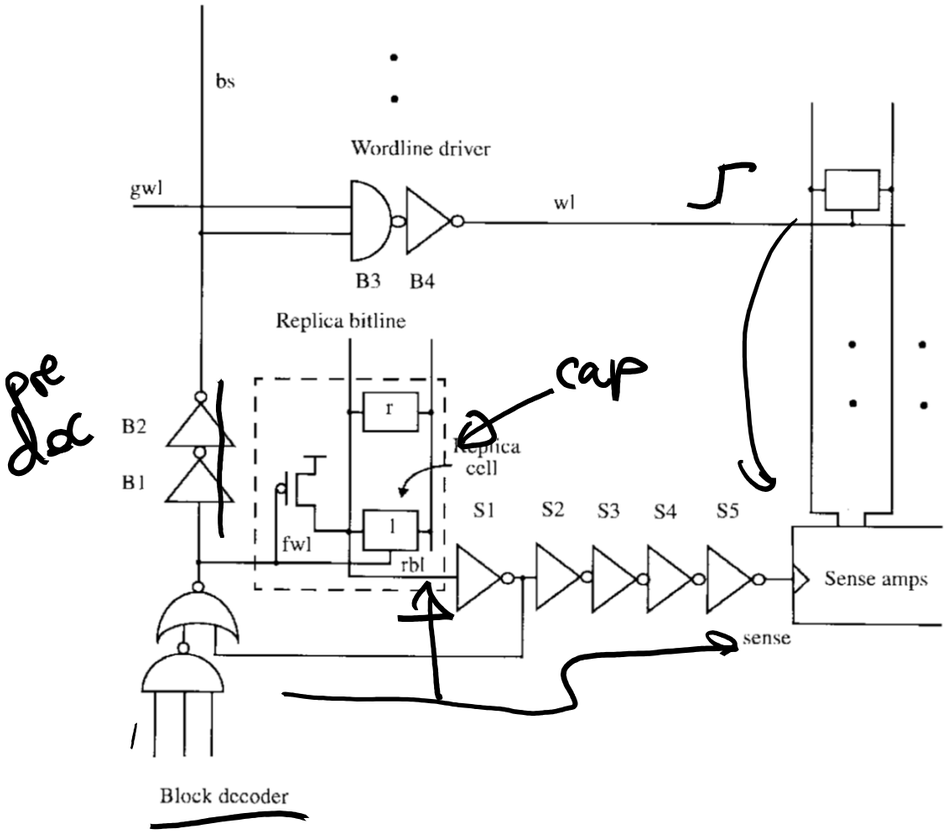


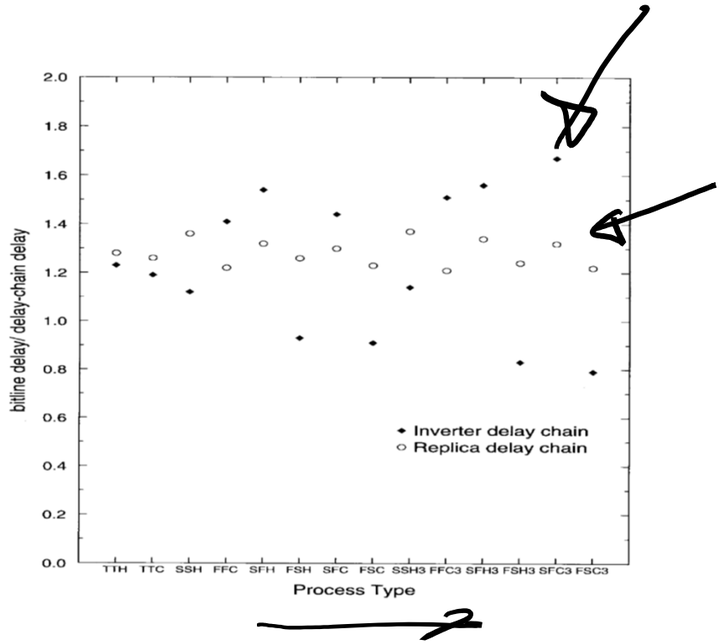
Sense-Amp Triggering

- Replica bitline





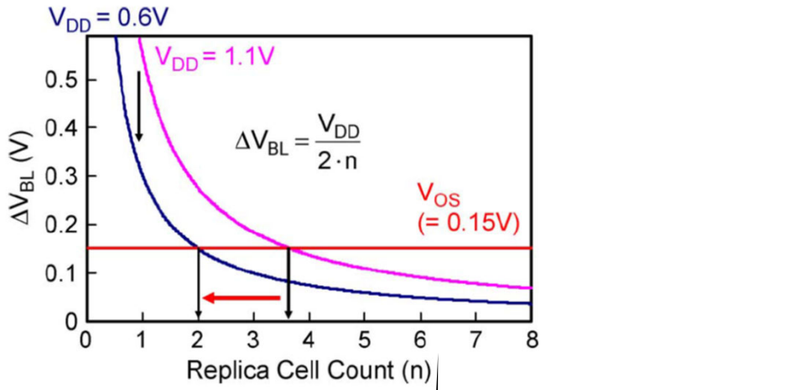


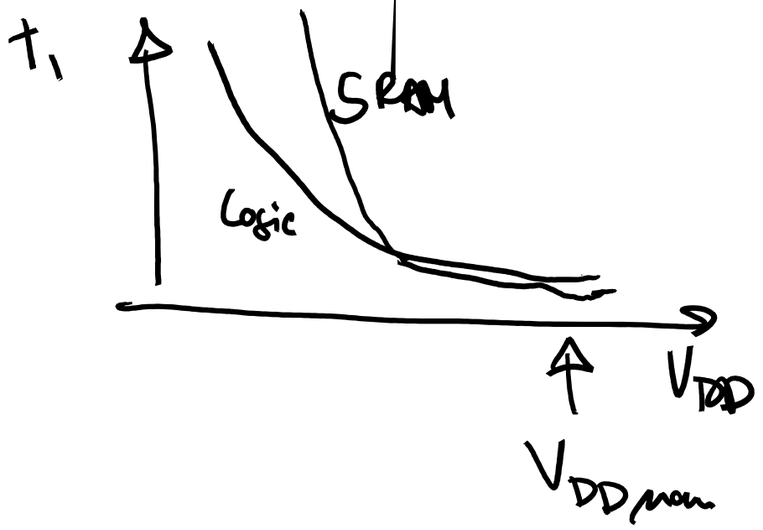


Amrutur, JSSC'98

Multiplicative Replica Bitline

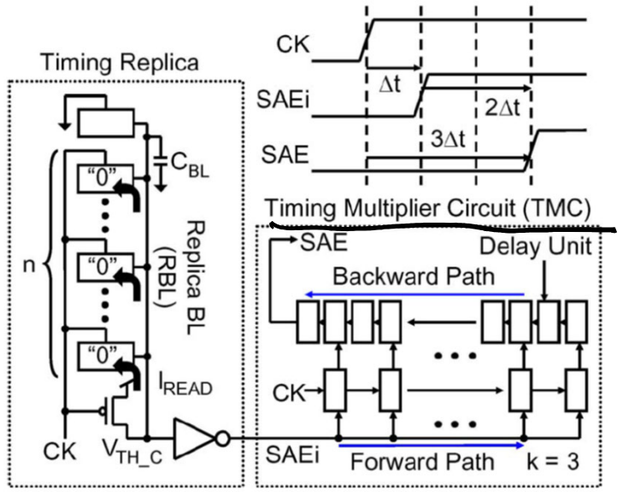
- Conventional replica

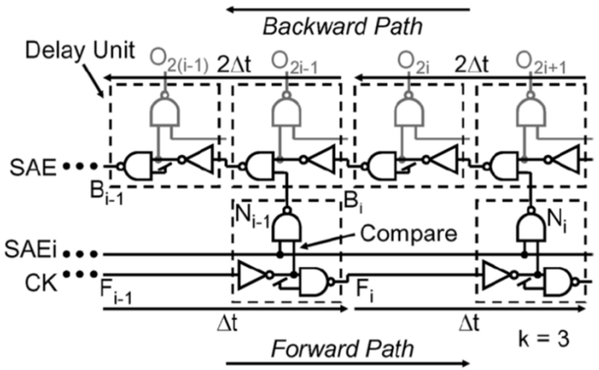




Niki, JSSC'11

- Multiplictive replica





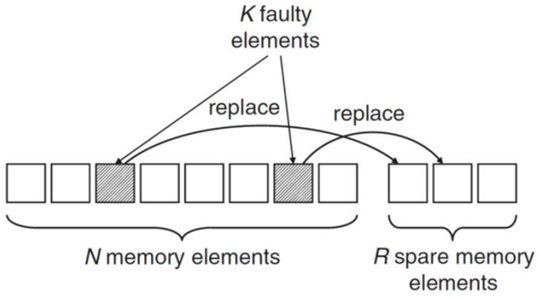
4.H Redundancy and ECC

Redundancy and ECC

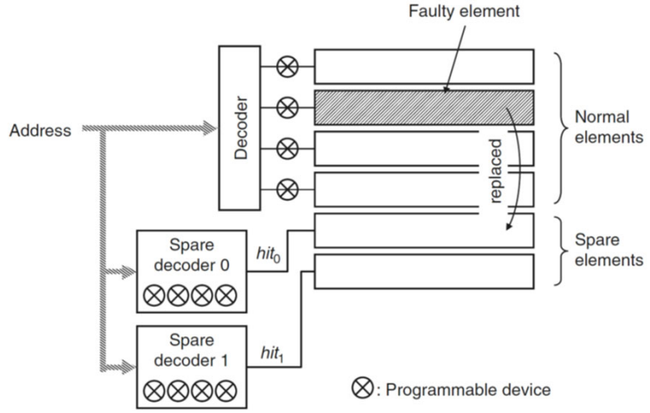
- Redundancy
  - Spare columns (or rows)
  - Selected at test via eFuse
  - Possible to dynamically program redundancy
- ECC
  - Error detection/correction codes
  - Parity
  - SECDED
  - DECTED

Redundancy

- Principle

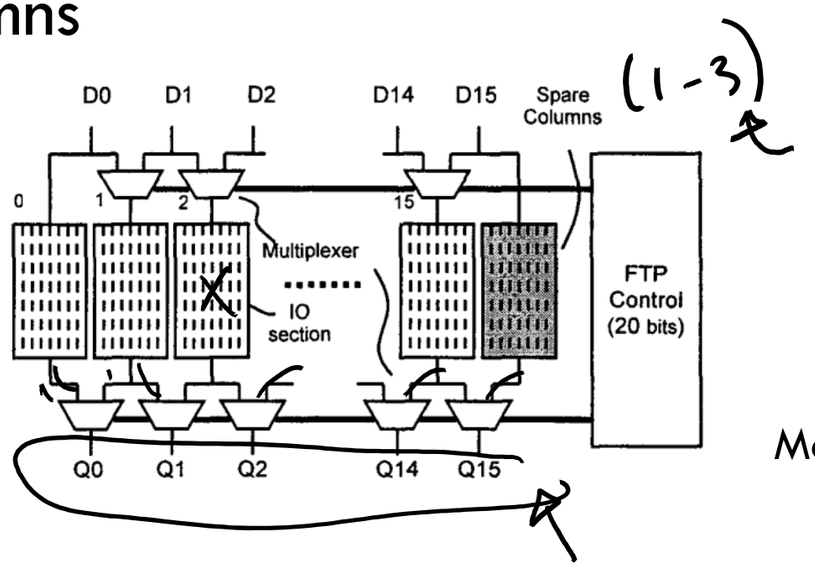


- Rows



Horiguchi, Itoh, Springer 2011.

- Columns



McPartland, CICC'00.

Redundancy

- Effectiveness (Bickford, 2008)

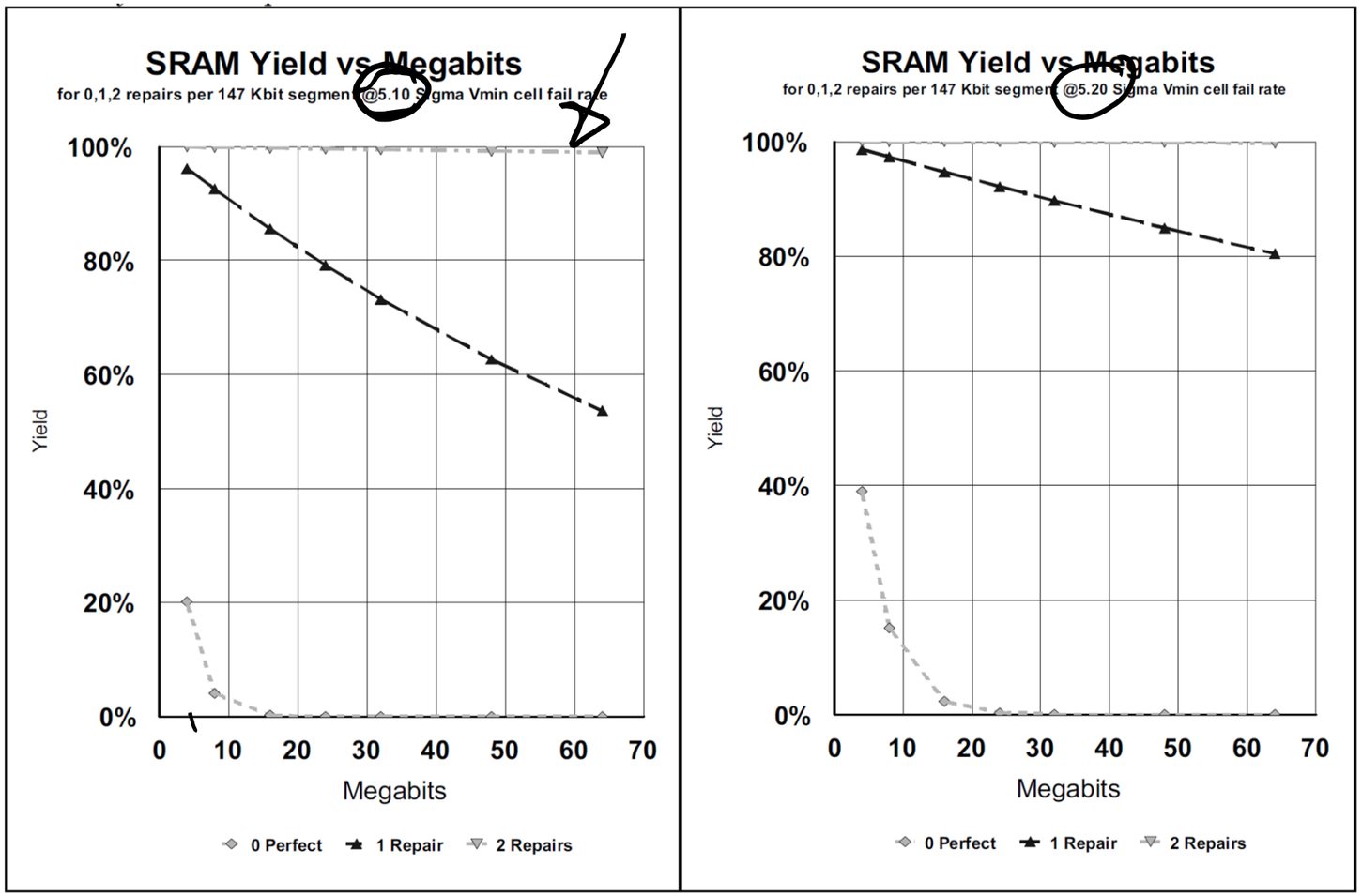
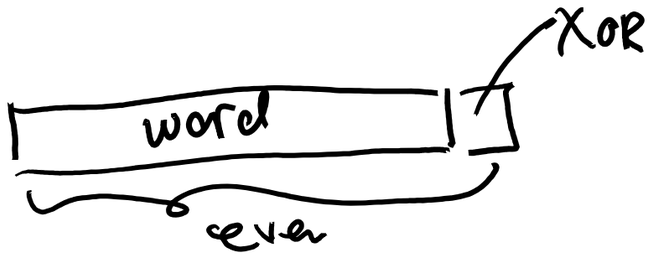


Figure 1: Modeled Yield impact comparison for 65 nm SRAM complier. Vmin cell fail rate used in analysis shown in the left chart is 5.10 sigma. Vmin cell fail rate used in the analysis shown in the right chart is 5.20 sigma. 147 Kbit segment is a standardized array size block segment used for comparison purposes .

Error Correction

- Parity (SED)

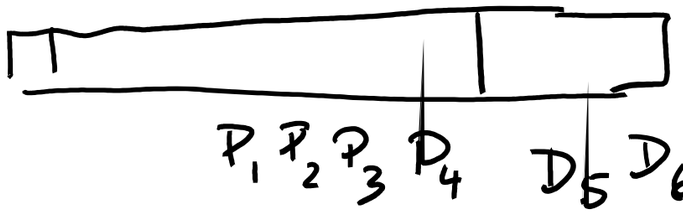
SINGLE ERROR DET.



- SECDED

single error corr. double

Hamming (7,4)



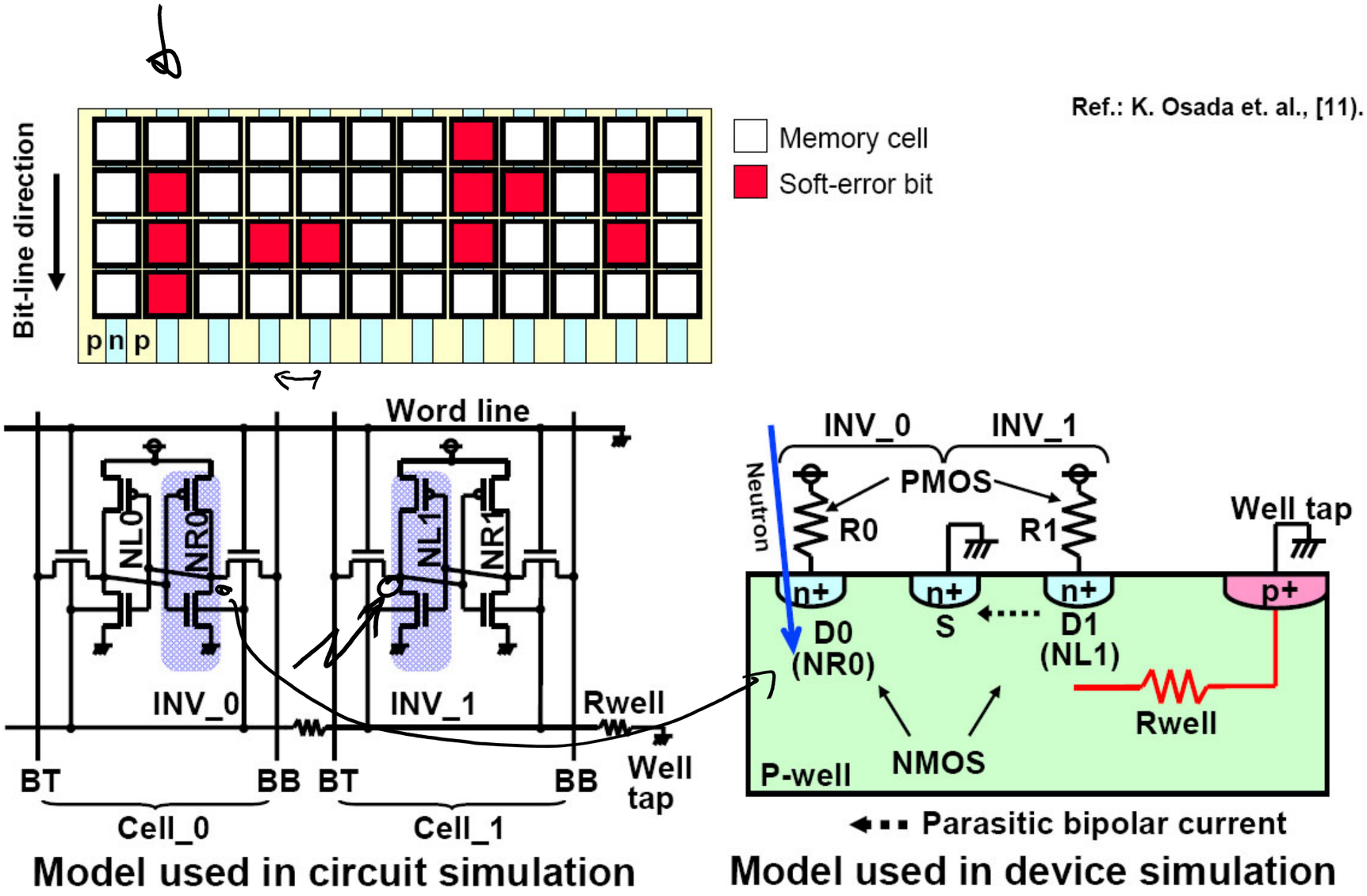
$P_4 = P_4 \oplus D_5 \oplus D_6 D_7$

P_0 P_3 =

P_2 =

- DECTED

Multi-bit Errors



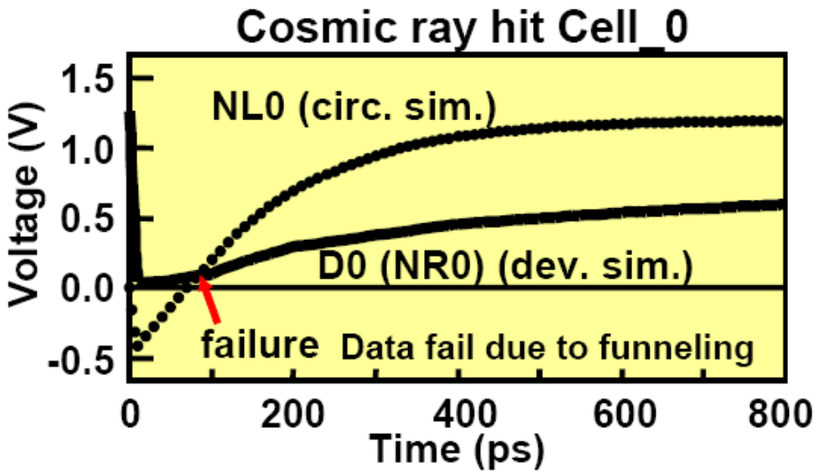
Kawahara, ISSCC'07 tutorial

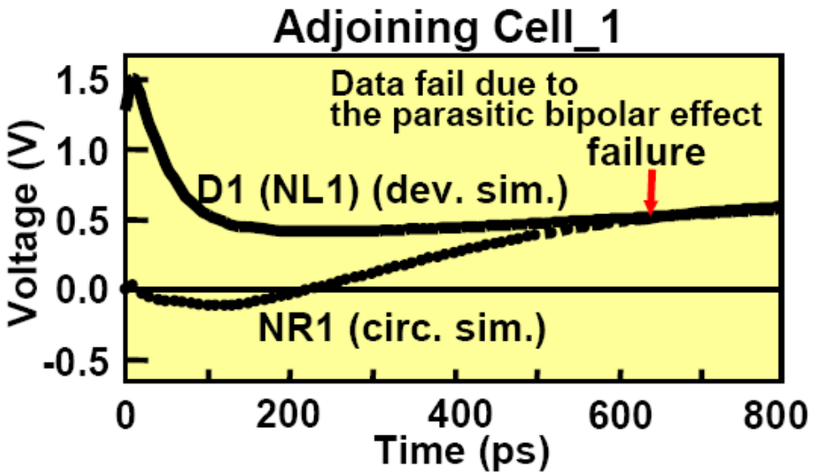
Soft Errors

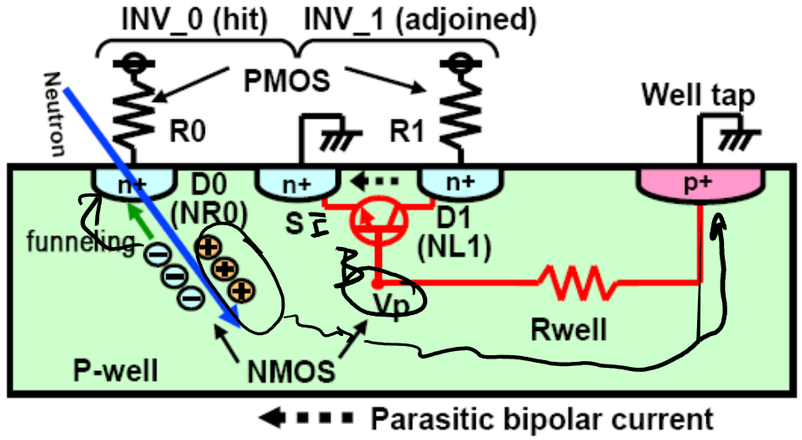
- From packaging and cosmic rays
- Packaging:
  - Lead contains Po-210 -> (5 days) -> Bi-210 -> (22.3 years) -> Pb-210
  - Or Po-210 -> (138.4 days) -> Pb-210
  - Need ‘old lead’
- Cosmic rays
  - Large particles collide with Earth’s atmosphere to produce alpha (and other) particles

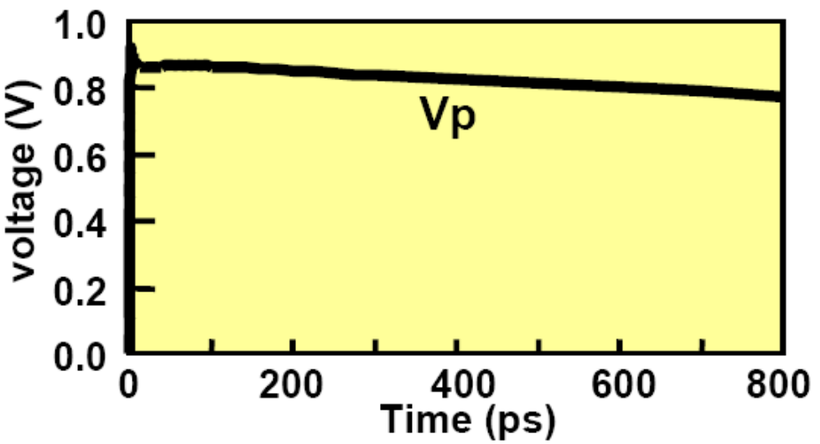
Multi-bit Errors

Ref.: K. Osada et. al., [11]



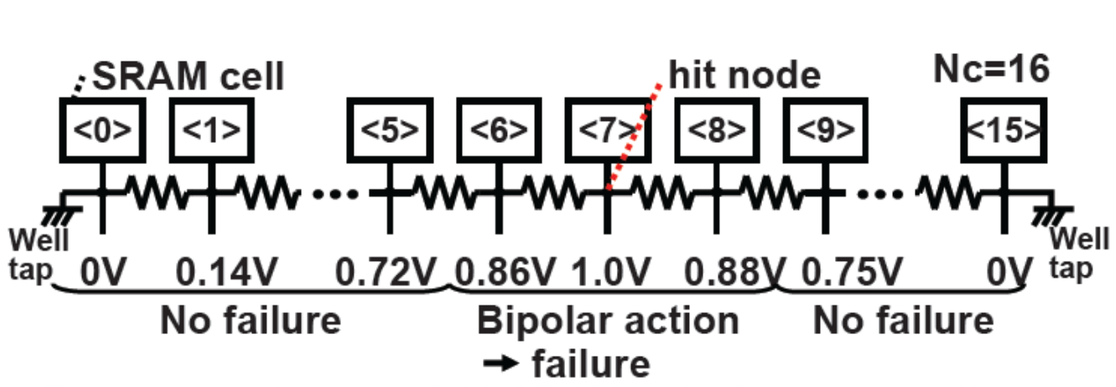






Kawahara, ISSCC'07 tutorial

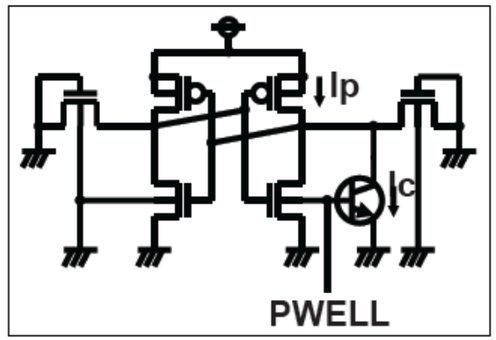
Multi-bit Errors

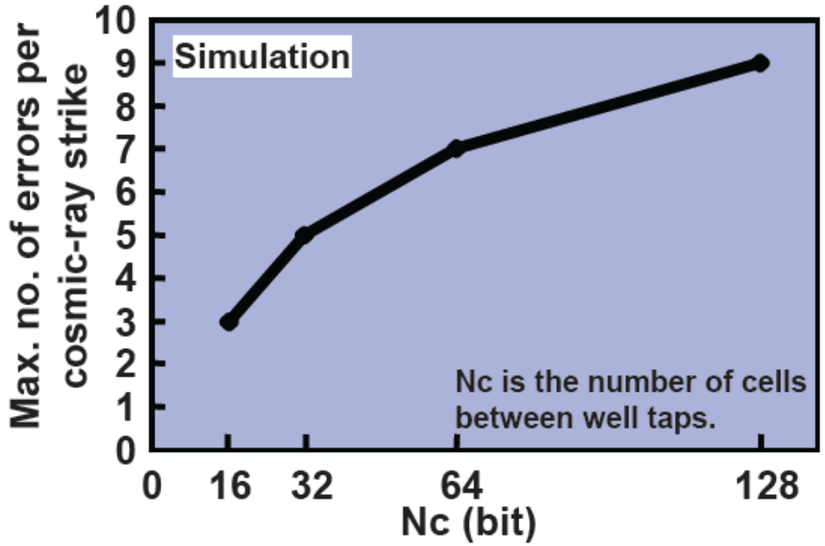


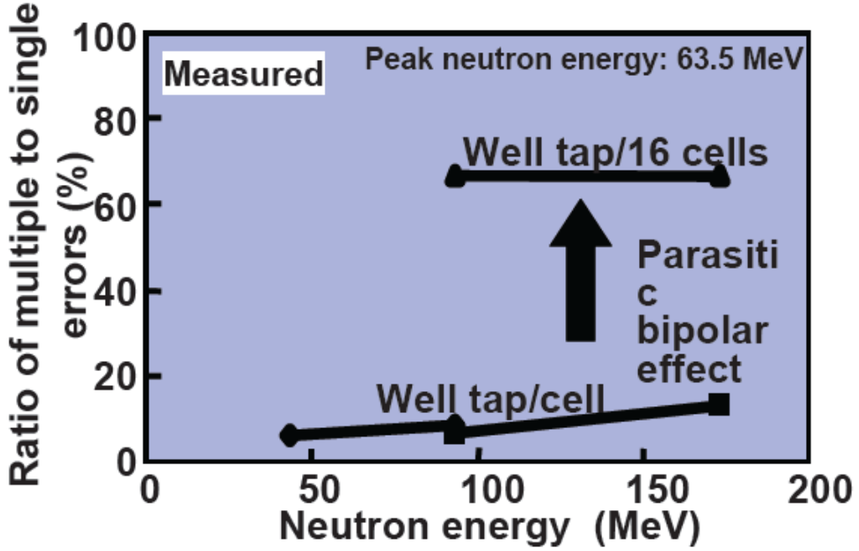
Equivalent circuits of 16 SRAM cells between well tap

Ref.: K. Osada et. al., [11]

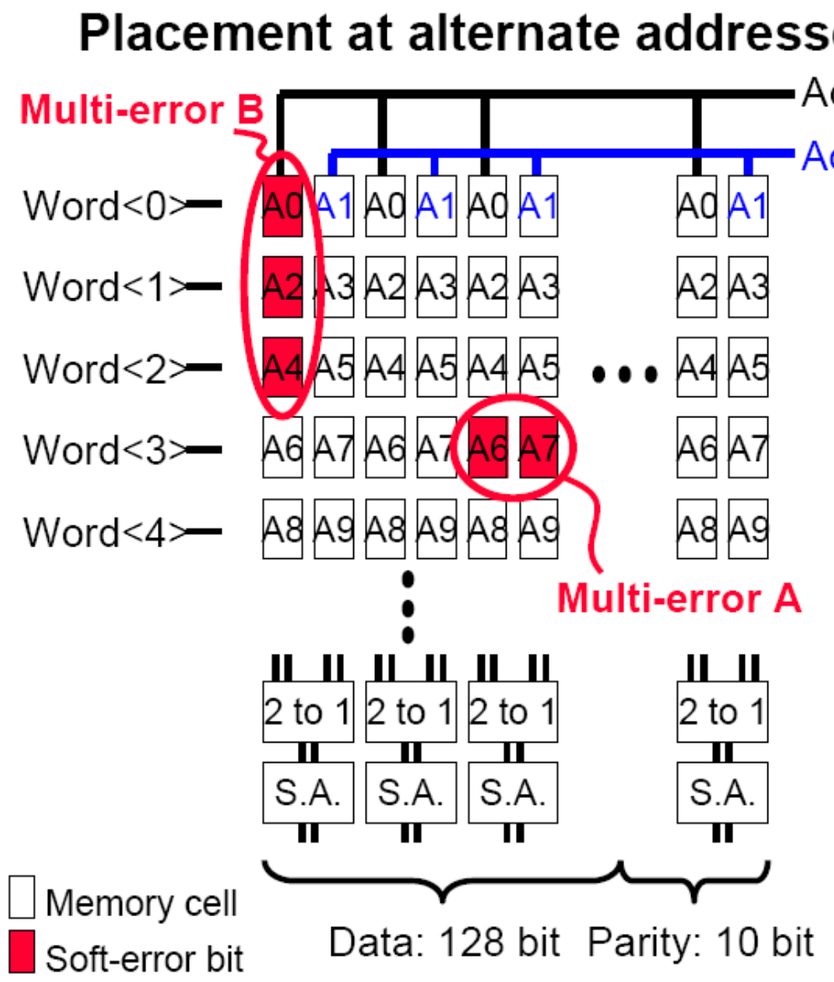
SRAM cell with parasitic bipolar

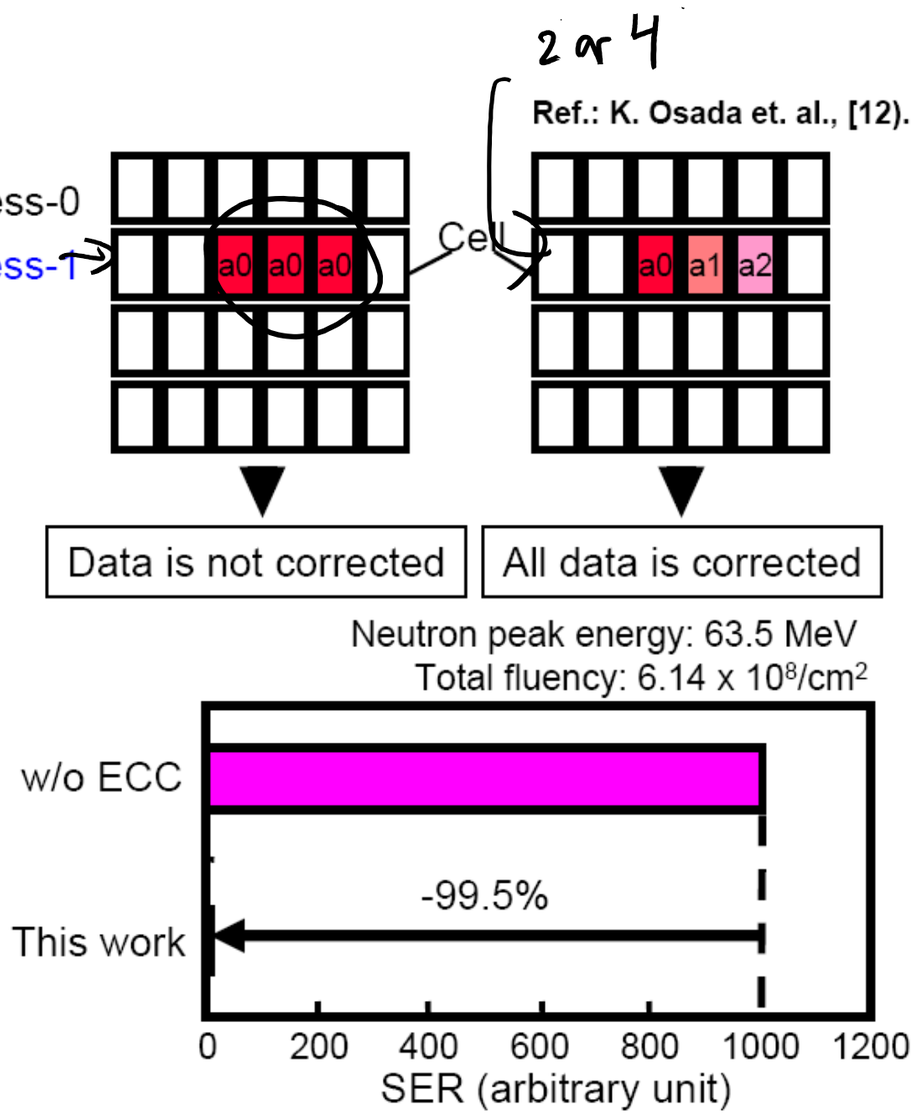






Multi-bit Errors: Interleaving

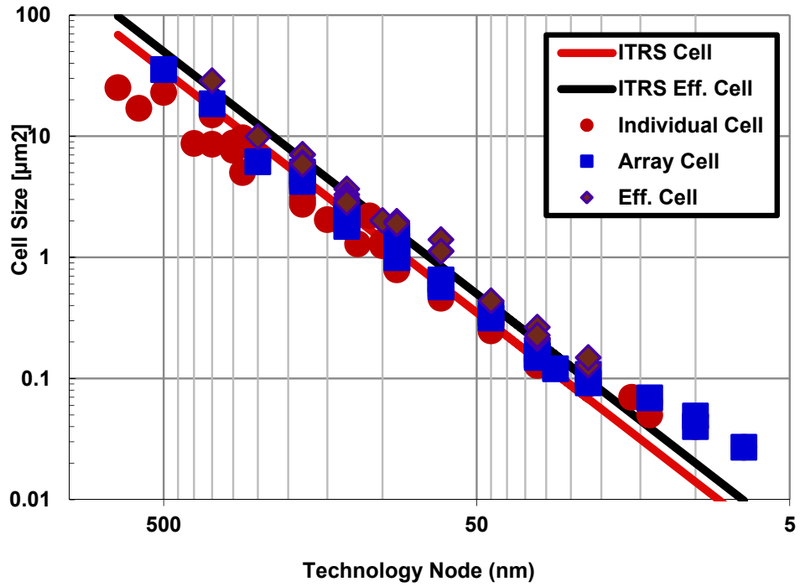




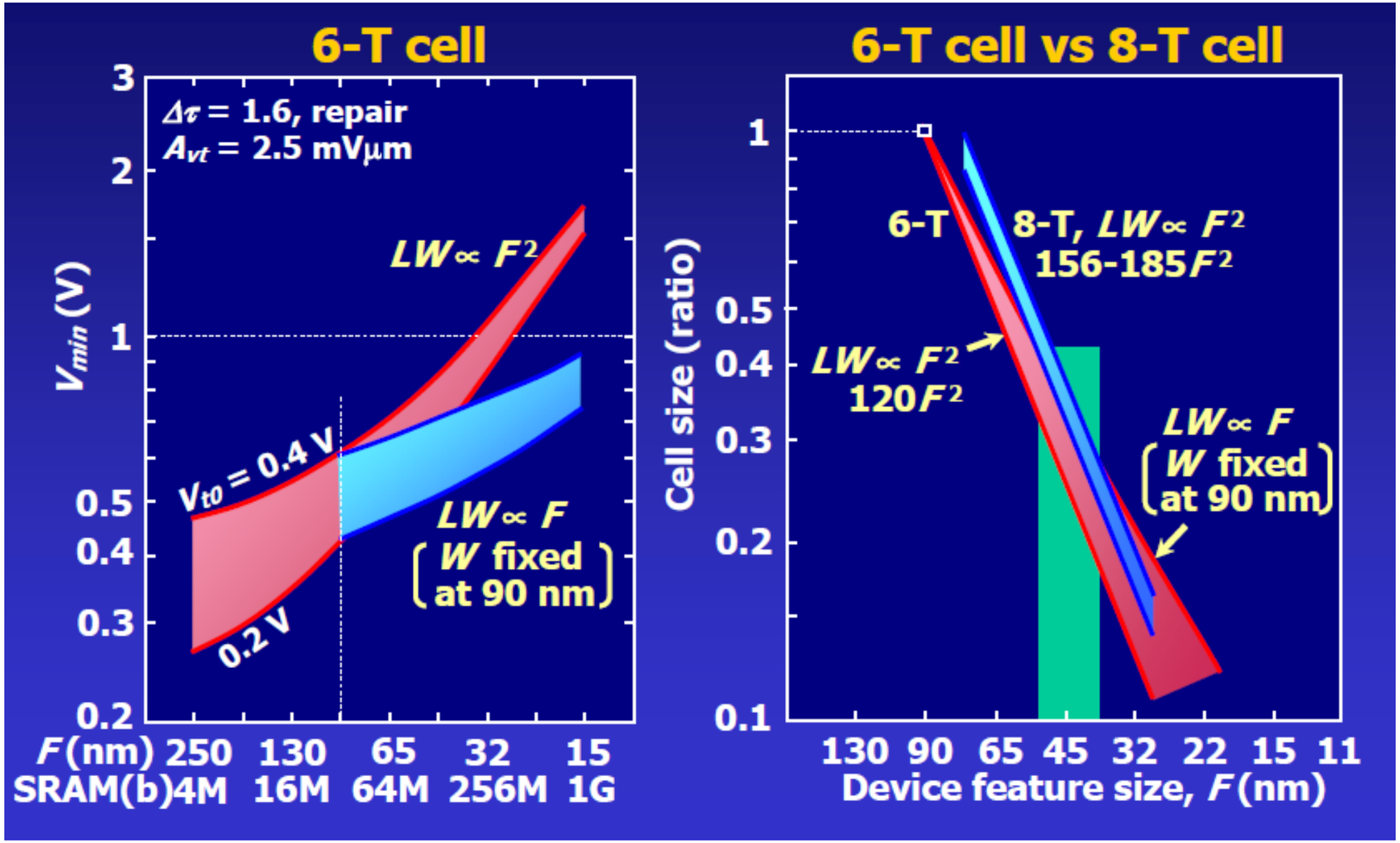
4.1 Options for Scaling

SRAM Scaling

- Approaching fundamental limits:
  - Don't scale cell size
  - Increase transistor count (from 6)
  - Change technology (e.g. channel material)
  - eDRAM
  - NVRAM
  - Or something else…

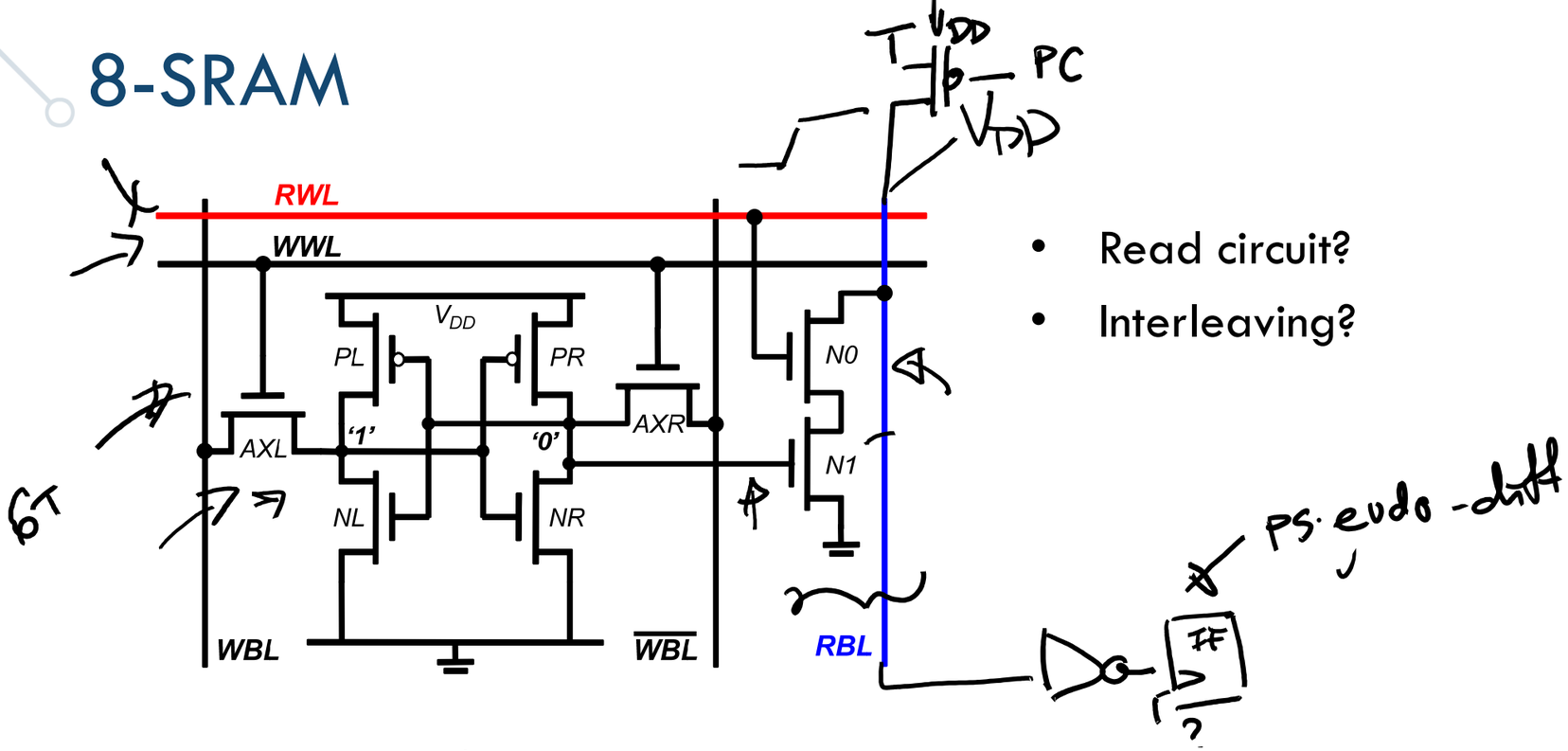


Vmin Scaling Projections



- Itoh, ISSCC'09

8-SRAM



- Read circuit?
- Interleaving?

- Dual-port read/write capability (register-file-like cells)
- N0, N1 separates read and write
  - No Read SNM constraint
  - Half-selected cells still undergo read
- Stacked transistors reduce leakage

L. Chang, *VLSI Circuits* 2005