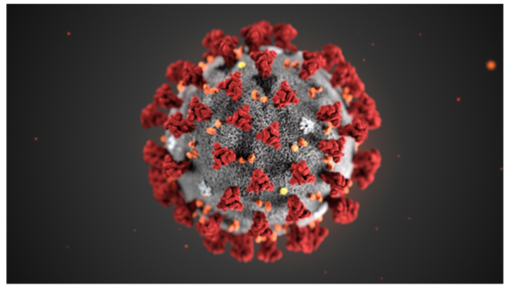
EE241B : Advanced Digital Circuits

Lecture 17 – Power-Performance Tradeoffs

Borivoje Nikolić

March 16, hpcwire.com: Folding@home Turns Its Massive Crowdsourced Computer Network Against COVID-19



Announcements

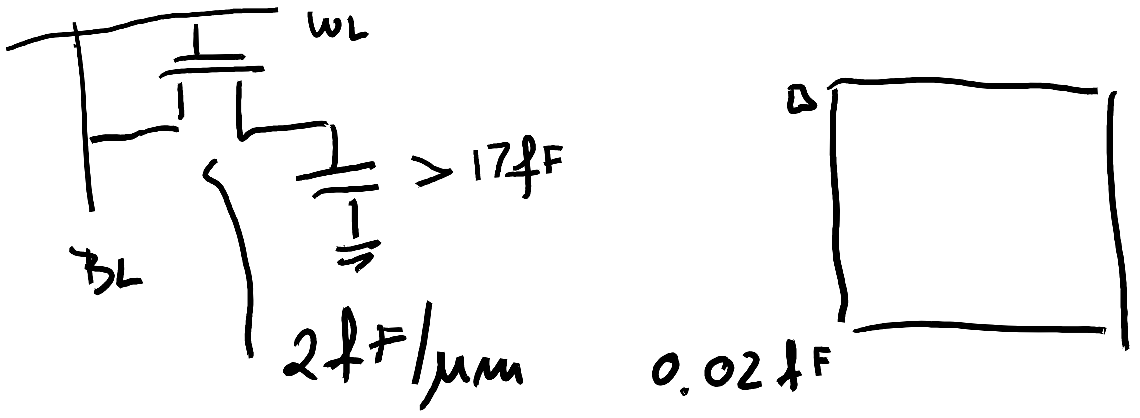
- Project midterm reports postponed until Tuesday, March 31
- Assignment 3 postponed until Thursday, April 2.
- Reading – req'd
  - Markovic et al, Methods for true energy-performance optimization, IEEE Journal of Solid-State Circuits, vol. 39, no.8, pp. 1281-1293, August 2004.
  - Chandrakasan and Brodersen, Low power CMOS digital design, IEEE Journal of Solid-State Circuits, vol. 27, no. 4, pp. 473-484, Apr. 1995.
- Recommended
  - Zyuban et al, Integrated Analysis of Power and Performance for Pipelined Microprocessors, IEEE Trans. on Computers, vol.53, no. 8, August 2004.

Outline

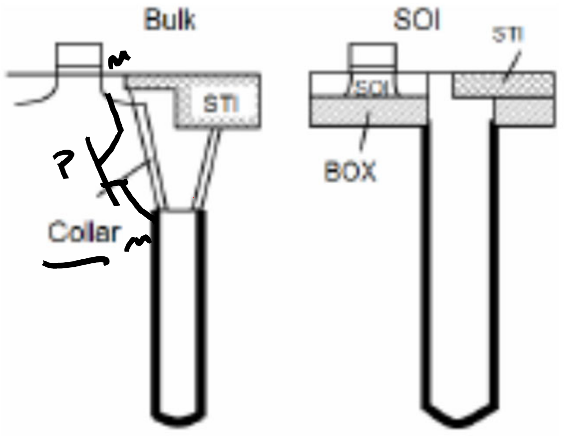
- Module 4
  - SRAM alternatives
- Module 5
  - Low-power design
  - Power-performance tradeoffs

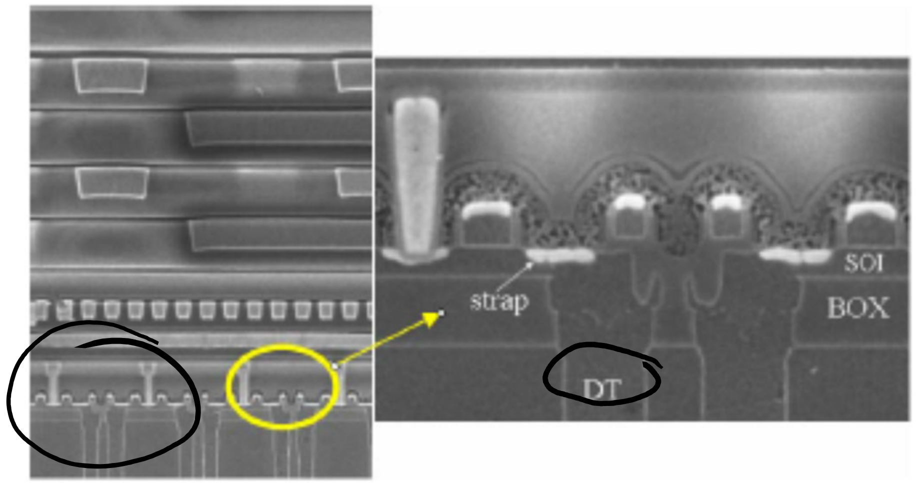
4.J SRAM Alternatives

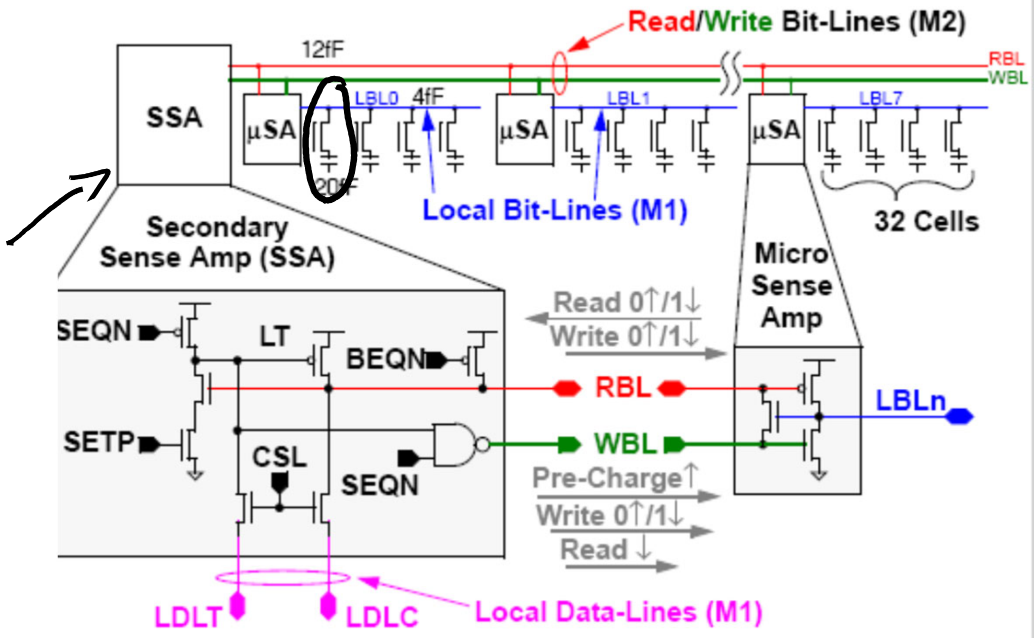
eDRAM

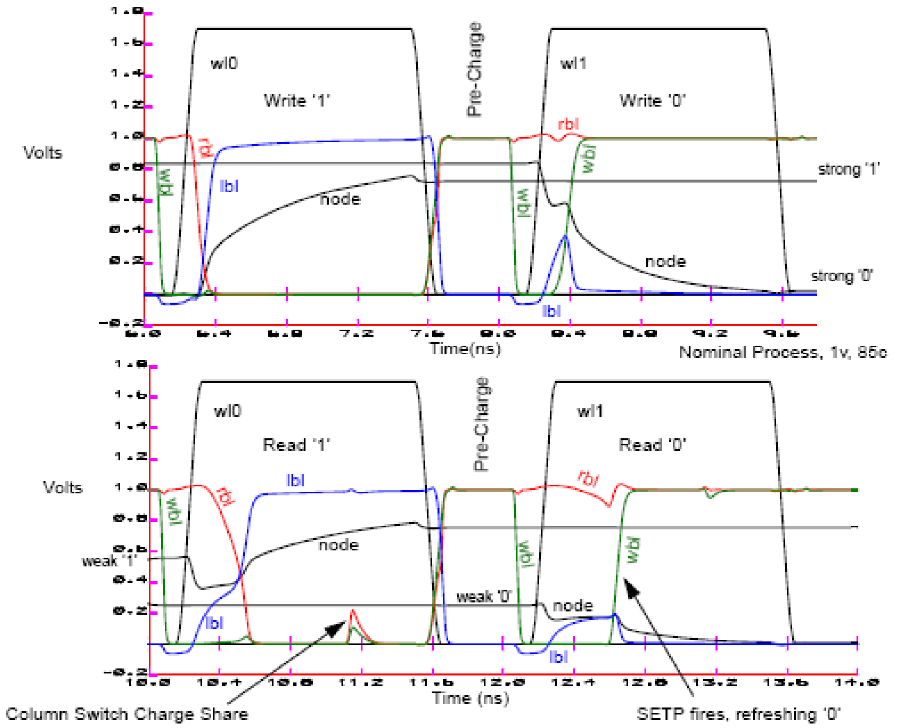


- Process cost: Added trench capacitor





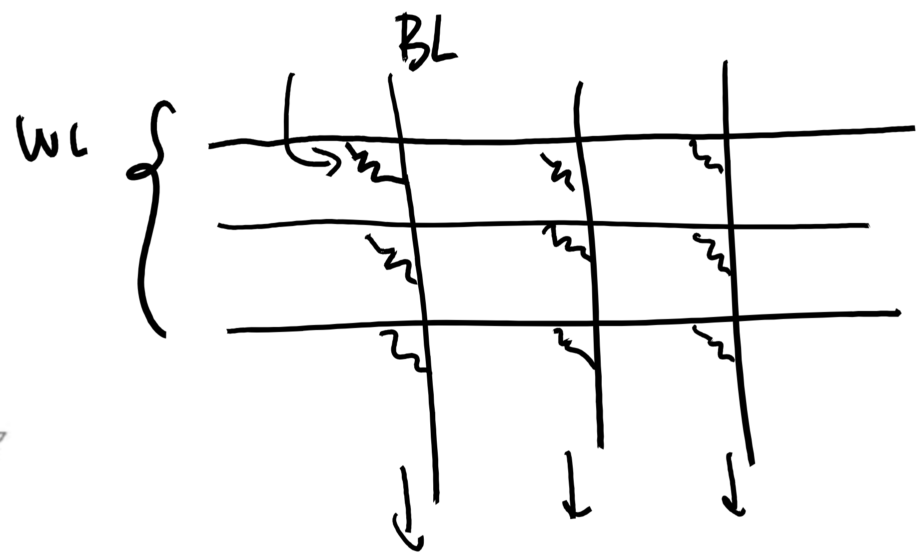




Barth, ISSCC'07, Wang, IEDM'06

Crosspoint Memories

- Barrett, IRE Trans. Comp. 1961.



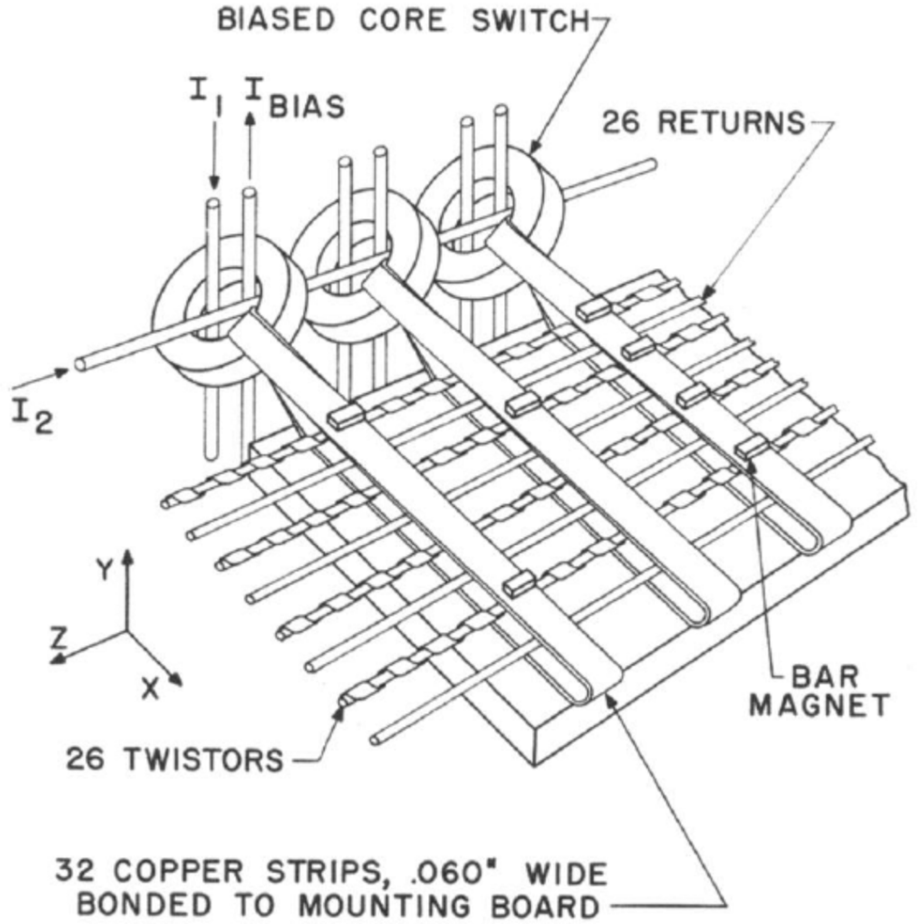
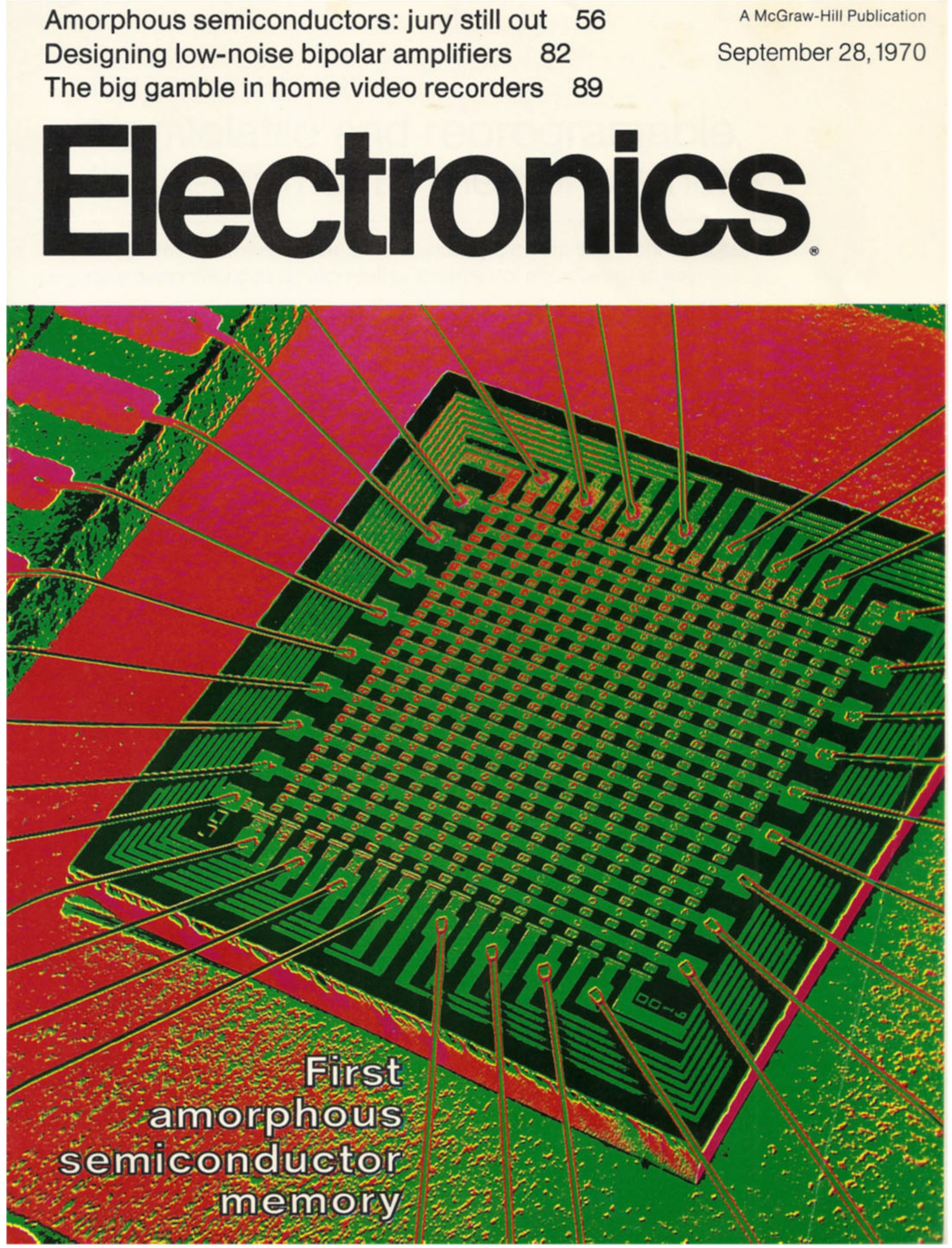
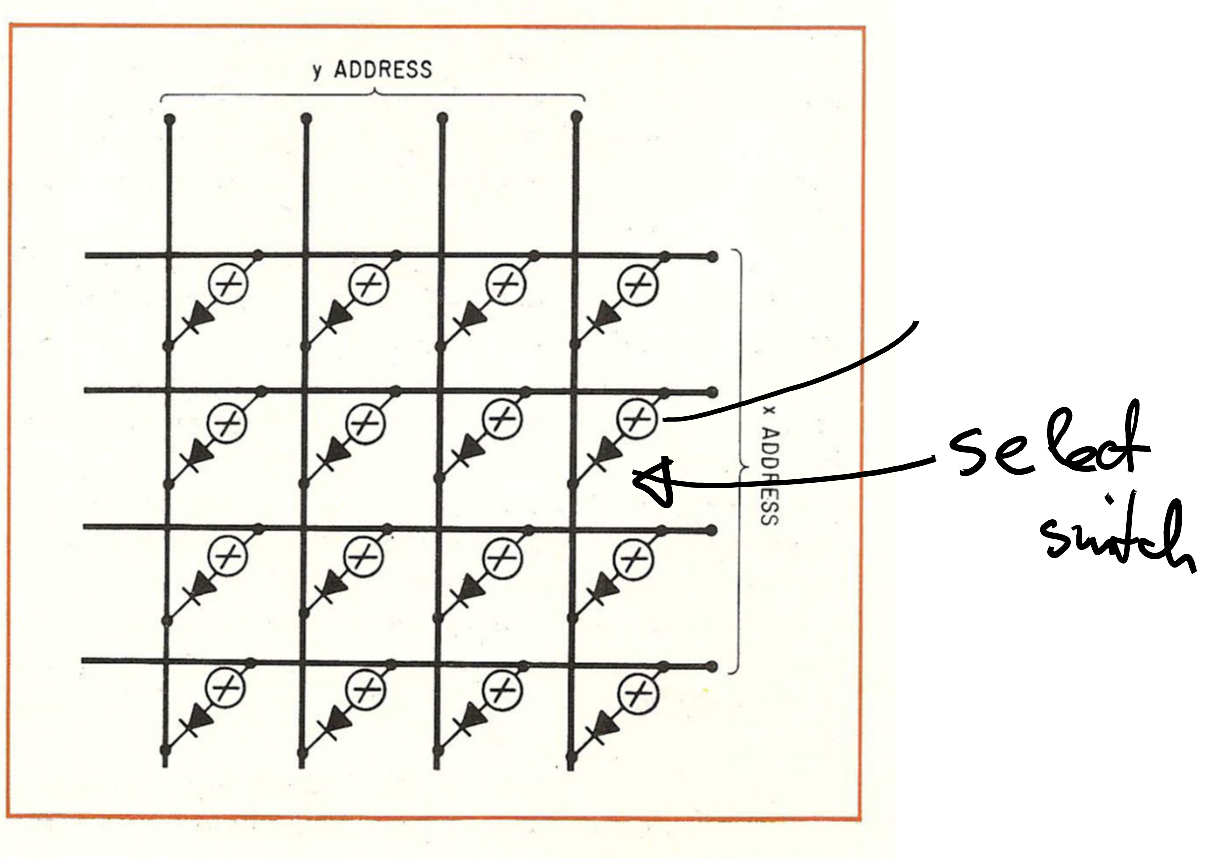


Fig. 2—Memory structure. I_1 and I_2 are access drive currents to core-selection switch. Presence or absence of a magnet over a twistor-strip solenoid crosspoint yields a "zero" or "one." Signals observed between twistor and return wire.

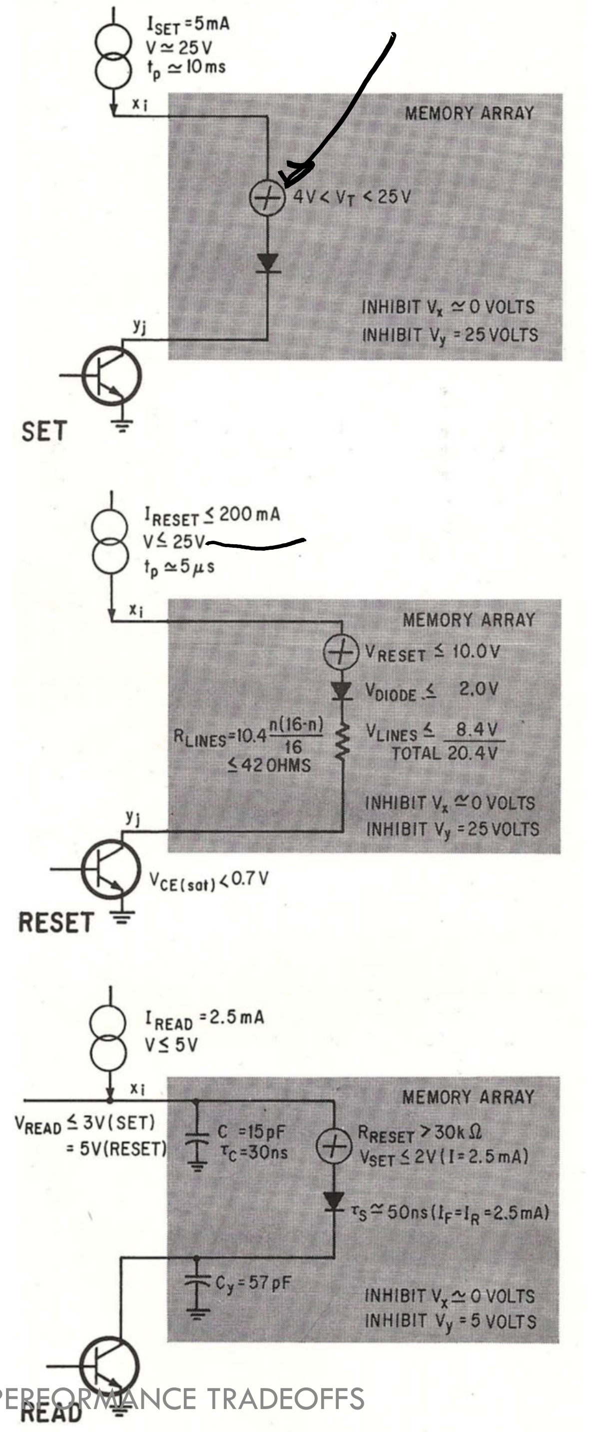
Crosspoint Memories



- Neale, Nelson, Moore, Electronics'70
  - 16 x 16 array (256b) of 'read-mostly memory'

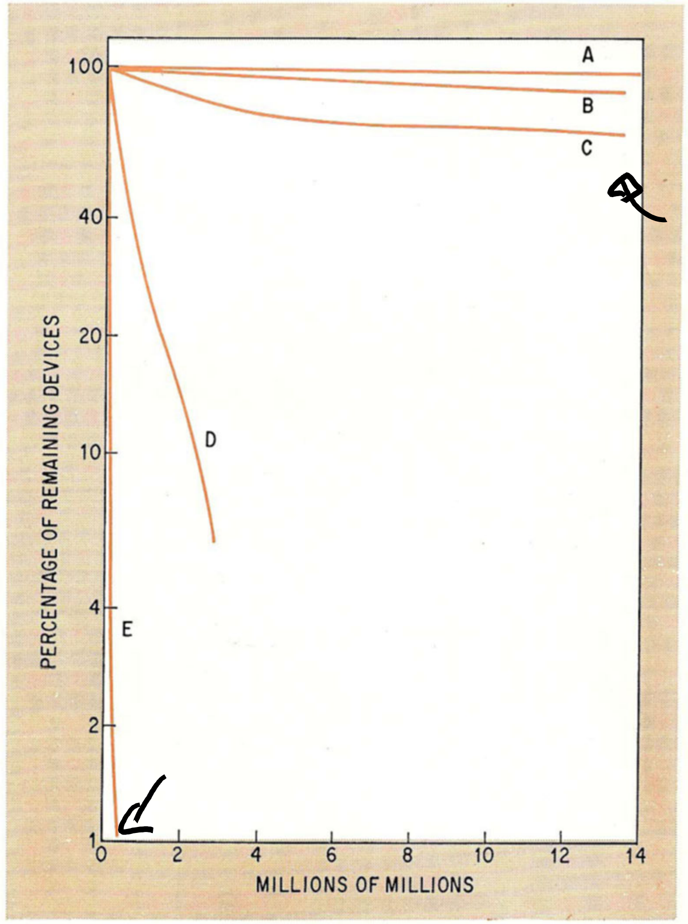


Crosspoint Memory



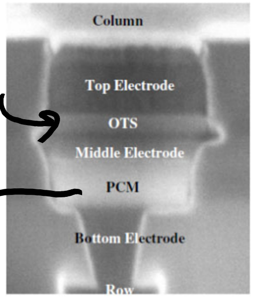
- Four modes
  - Form
  - Set
  - Reset
  - Read

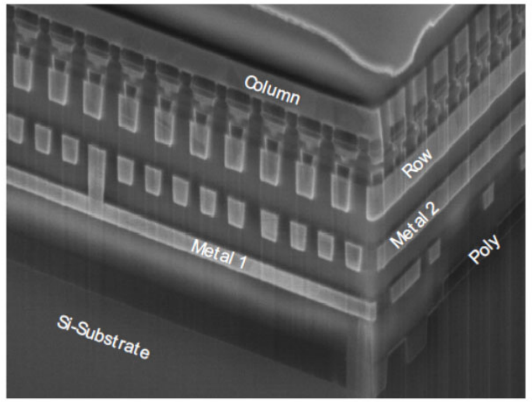
Endurance

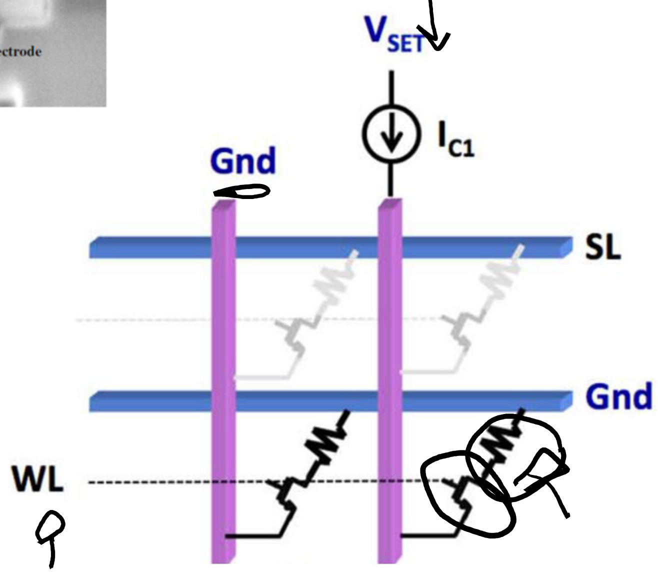


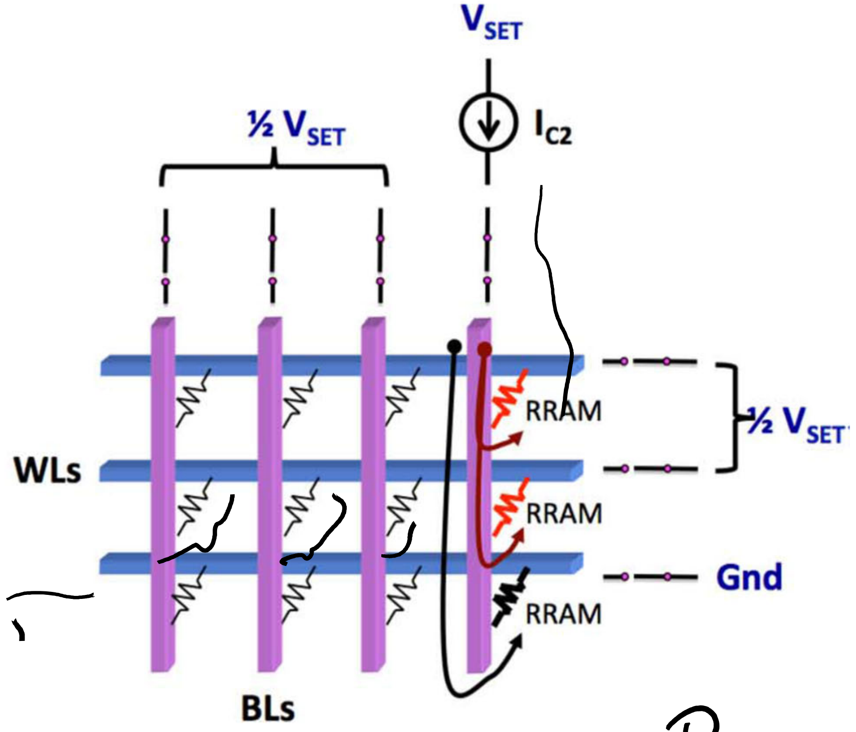
3D Crosspoint Arrays

- Kau, IEDM'09

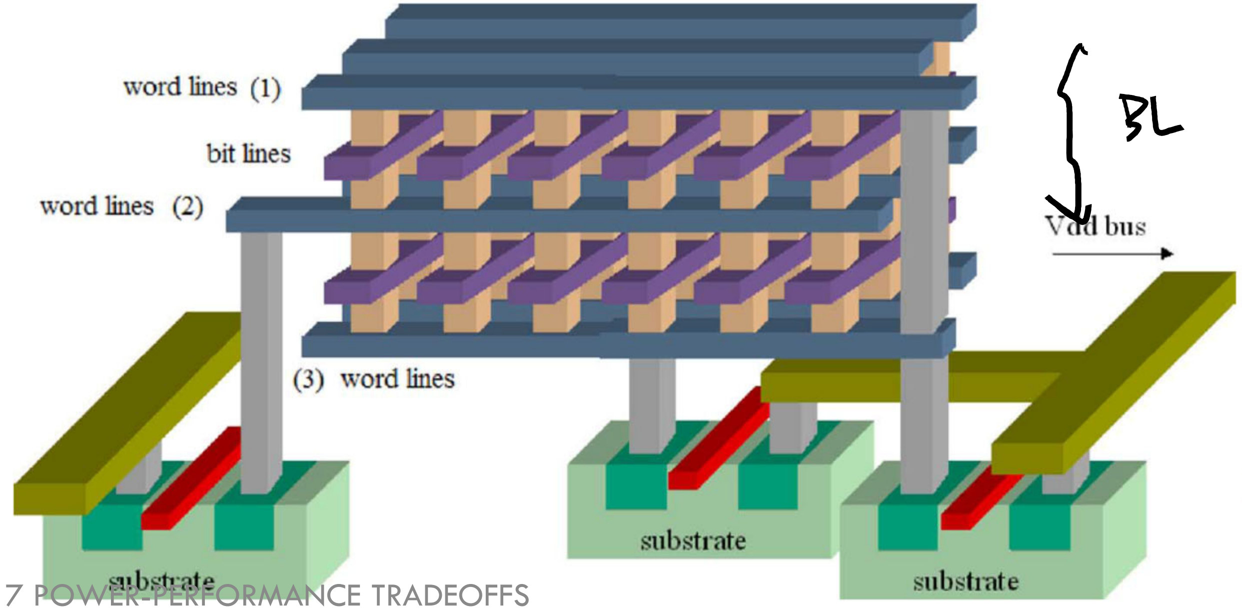








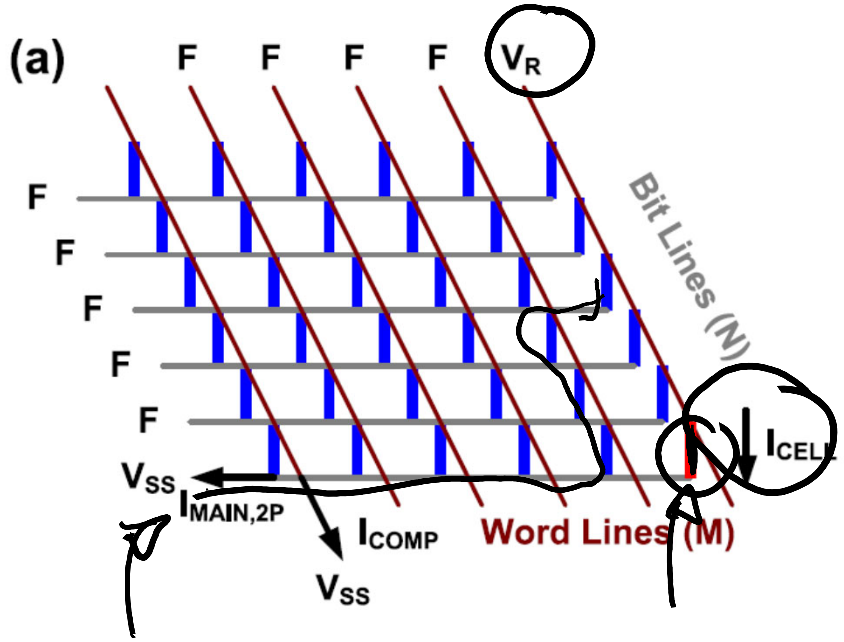
- Yeh, JSSC'15

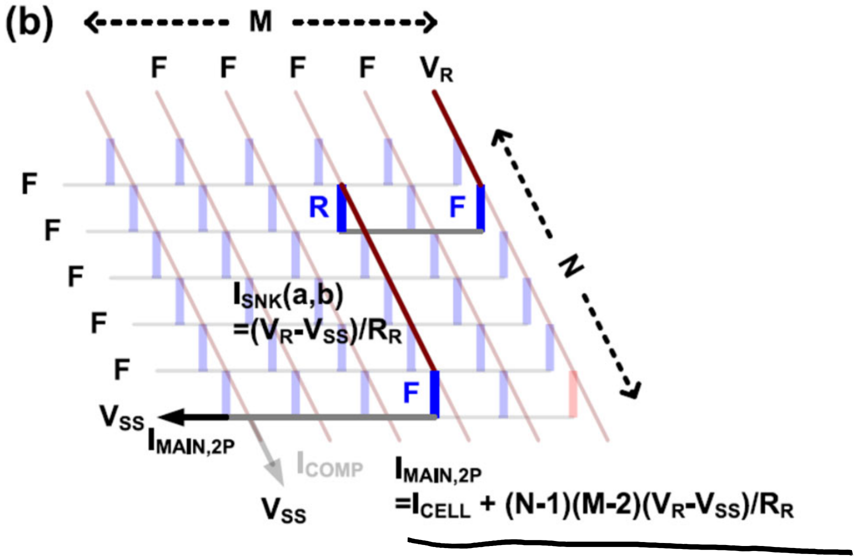


- Ou, JSSC'11

Crosspoint Arrays

- Read and sneak currents

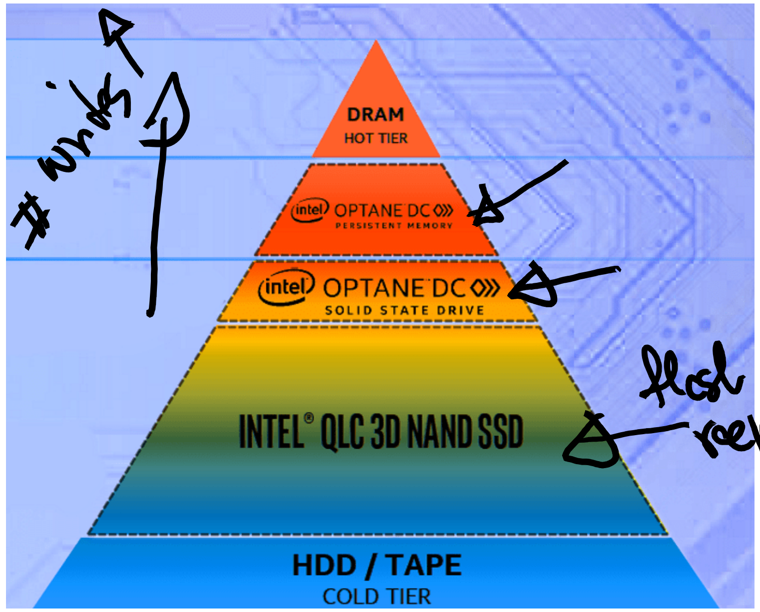




Bae, TED 4/17

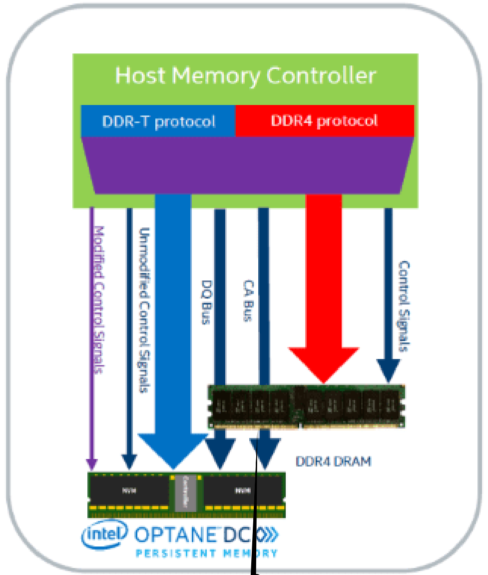
In the News…

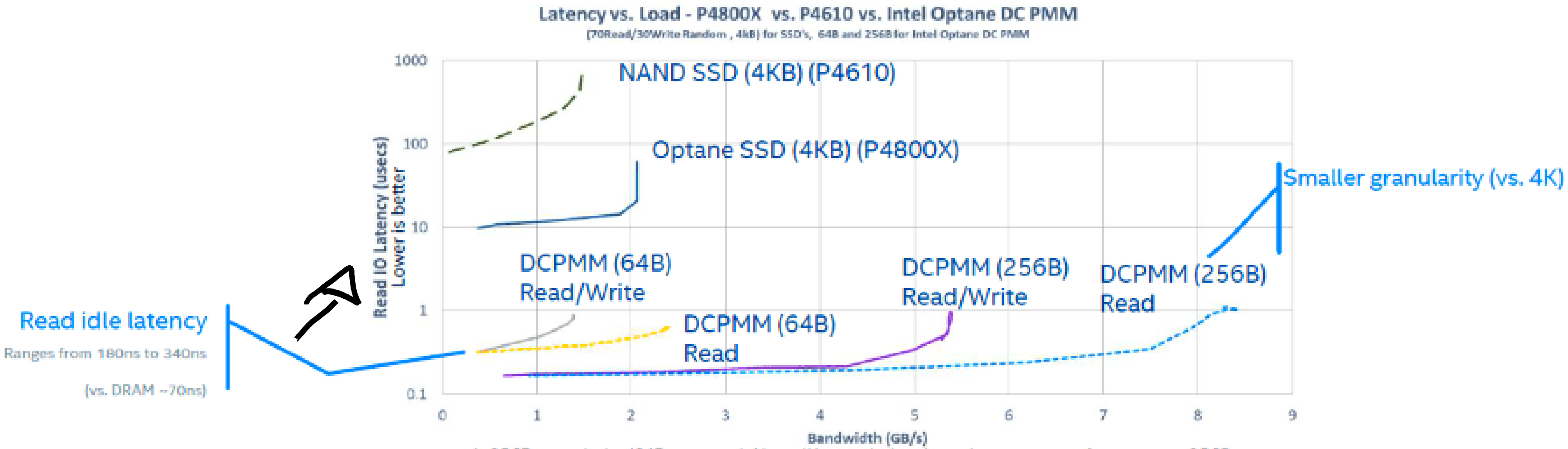
- Intel Optane = 3D XPoint



DDR-T PROTOCOL

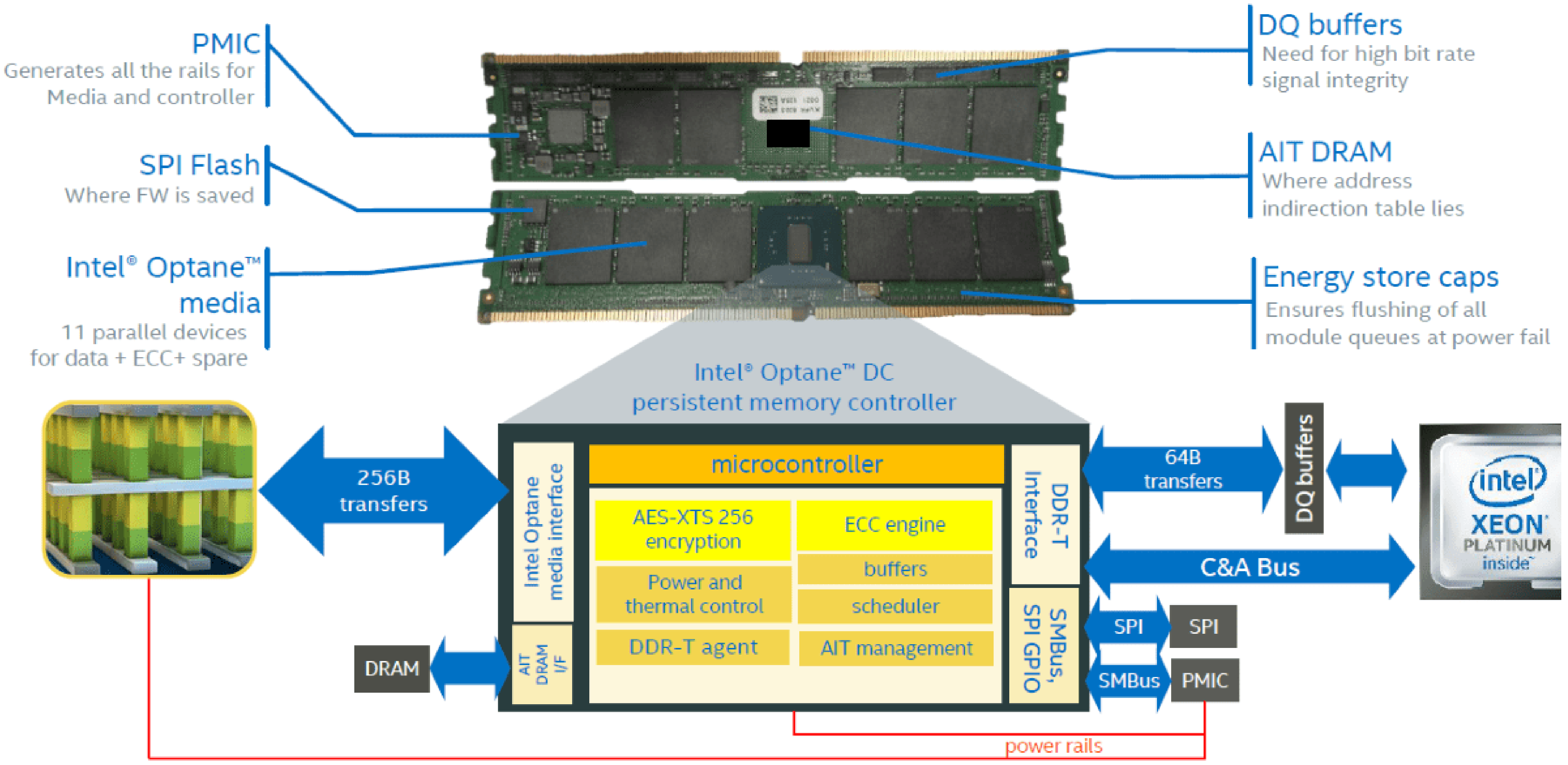
- Protocol on top of electrical/mechanical interface for DDR4
- Allows for asynchronous command/data timing
  - Controller uses request/grant scheme to communicate with host controller
  - Data bus direction and timing controlled by host
  - Command packet per request sent from host to Intel® Optane™ DC persistent memory controller
- Transaction can be re-ordered in the Intel Optane DC persistent memory controller
- 64B cache line access granularity (similar to DDR4)

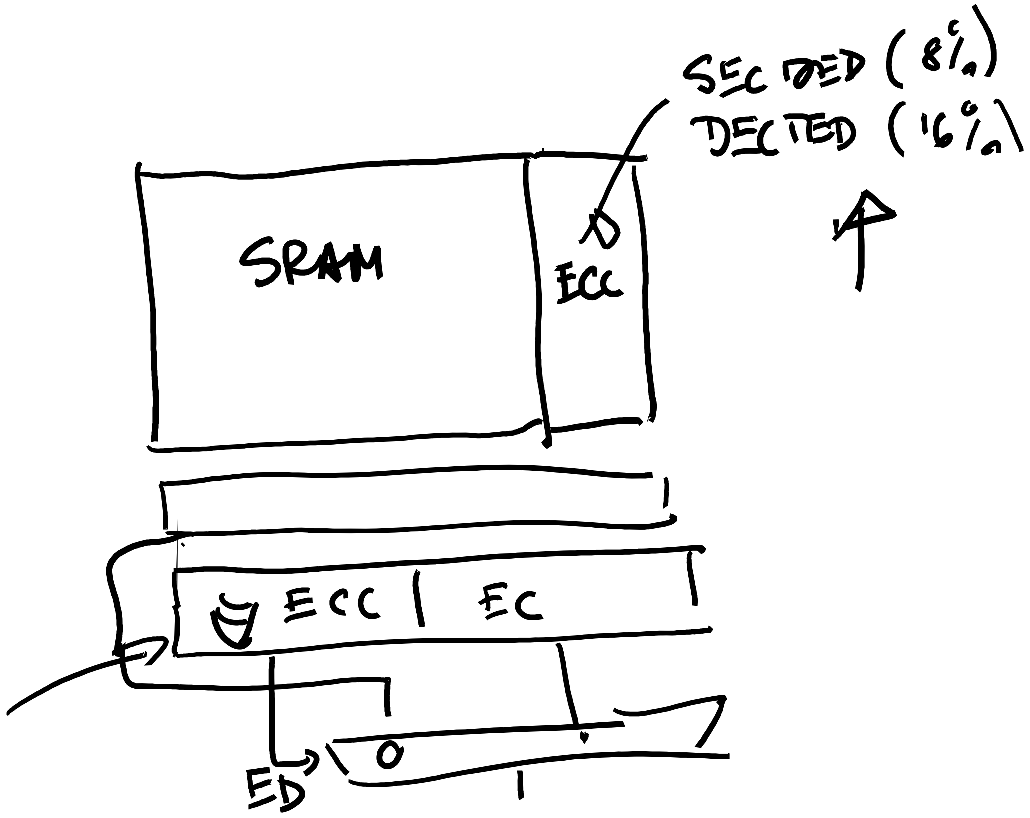




1. 256B granularity (64B accesses). Note 4K granularity gives about same performance as 256B

Optane DDR


PMIC
Generates all the rails for Media and controller
SPI Flash
Where FW is saved
Intel® Optane™ media
11 parallel devices for data + ECC+ spare
DQ buffers
Need for high bit rate signal integrity
AIT DRAM
Where address indirection table lies
Energy store caps
Ensures flushing of all module queues at power fail
Intel® Optane™ DC persistent memory controller
256B transfers
Intel Optane media interface
microcontroller
AES-XTS 256 encryption
ECC engine
buffers
Power and thermal control
scheduler
DDR-T agent
AIT management
DDR-T Interface
SMBus, SPI GPIO
AIT DRAM I/F
DRAM
64B transfers
DQ buffers
C&A Bus
SPI
SPI
SMBus
PMIC
power rails
intel
XEON
PLATINUM
inside



5. Low-Power Design

Importance of Power Awareness

- Energy: Crucial for Portable Applications
  - Determines battery lifetime — idle / active
  - Amount of computation that can be performed — J
  - Performance is what sells products → Energy efficiency
- Power: Crucial for High-Performance Applications & Portable
  - Determines cooling and energy costs
  - Most designs today are power limited — package / socket { passive, forced air, liquid }
  - Still need maximum performance

$P = E \cdot f$

Power efficiency

The Old Design Philosophy

- Maximum performance is primary goal
  - Minimum delay at circuit level
- Architecture implements the required function with target throughput, latency
- At circuit level, supplies, thresholds set to achieve maximum performance, subject to reliability constraints
- Performance achieved through optimum sizing, logic mapping, architectural transformations

Constant Field Scaling Model

Scale by 0.7

130 → 90 → 65 → 45 → 32

Traditional scaling model

If $V_{DD} = 0.7$, and $Freq = (\frac{1}{0.7})$, ≈ 1.43

$$Power = CV_{DD}^2 f = (\frac{1}{0.7} \times 1.14^2) \times (0.7^2) \times (\frac{1}{0.7}) = 1.3$$

die size increase

$\frac{1}{(0.7)^2} = 2$

Maintaining the frequency scaling model of 1990s

If $V_{DD} = 0.7$, and **Freq = 2,**

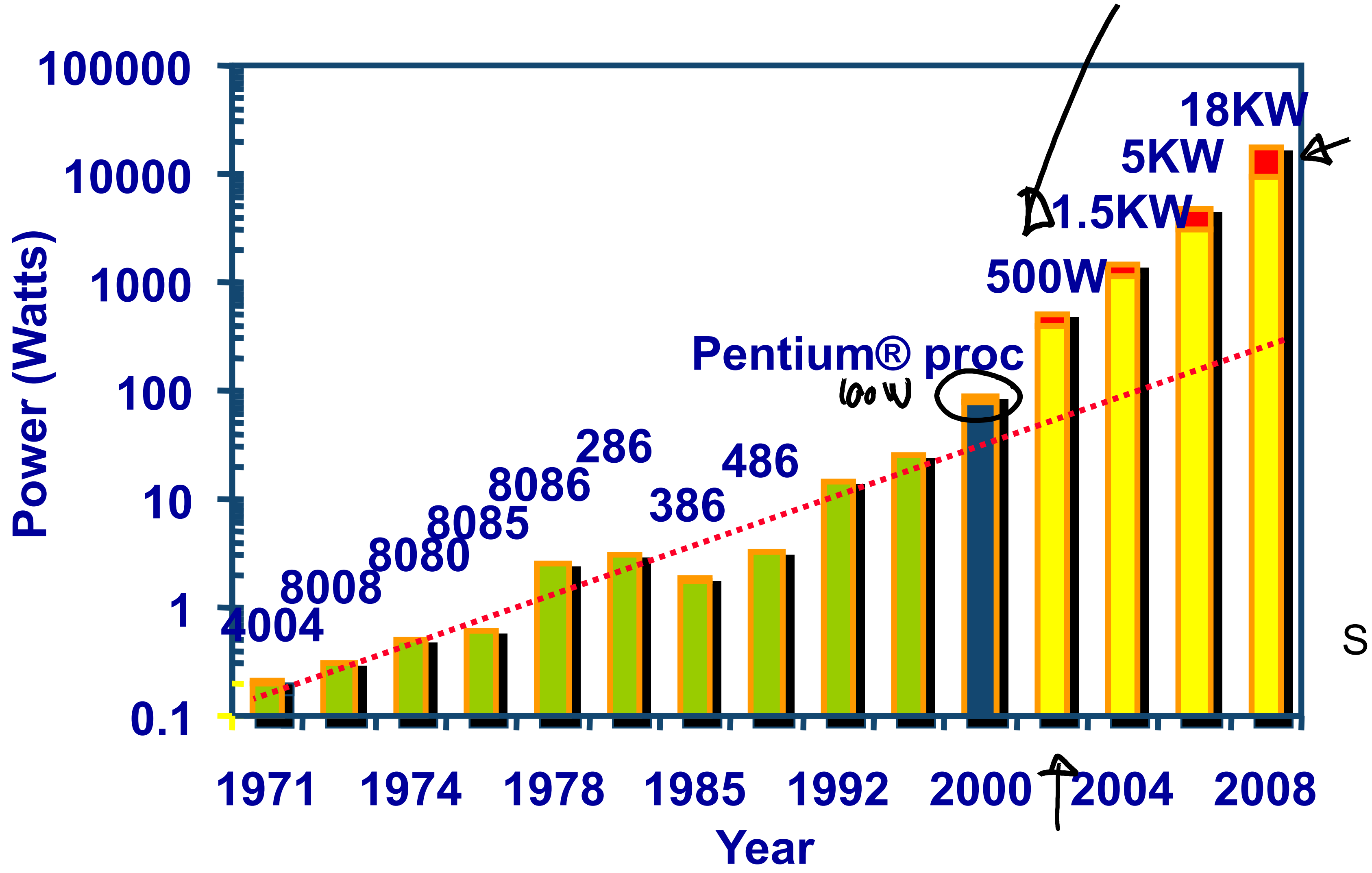
$$Power = CV_{DD}^2 f = (\frac{1}{0.7} \times 1.14^2) \times (0.7^2) \times (2) = 1.8$$

While slowing down voltage scaling

If V_{DD} **= 0.85**, and $Freq = 2$,

$$Power = CV_{DD}^2 f = (\frac{1}{0.7} \times 1.14^2) \times (0.85^2) \times (2) = 2.7$$

2001 Picture: Power As a Problem



S. Borkar

Power delivery and dissipation will be prohibitive

The New Design Philosophy

- Maximum performance is too power-hungry, and/or not even practically achievable
- Extract maximum performance under a power/energy envelope
- Excess performance (as offered by technology) to be used for energy/power reduction

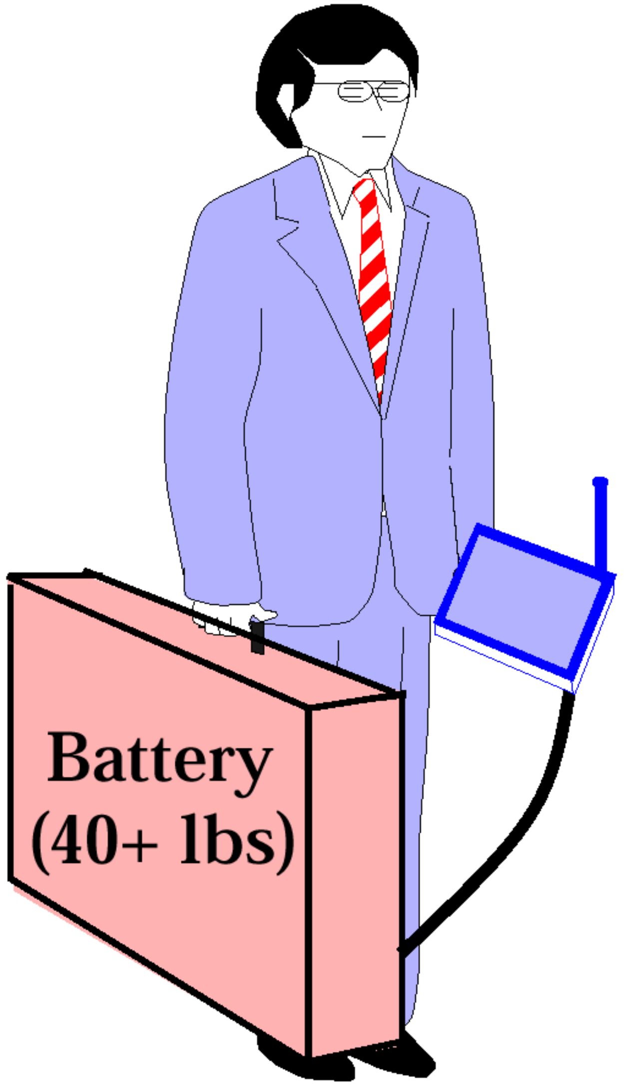
Trading off speed for power

5.A Power and Energy Basics

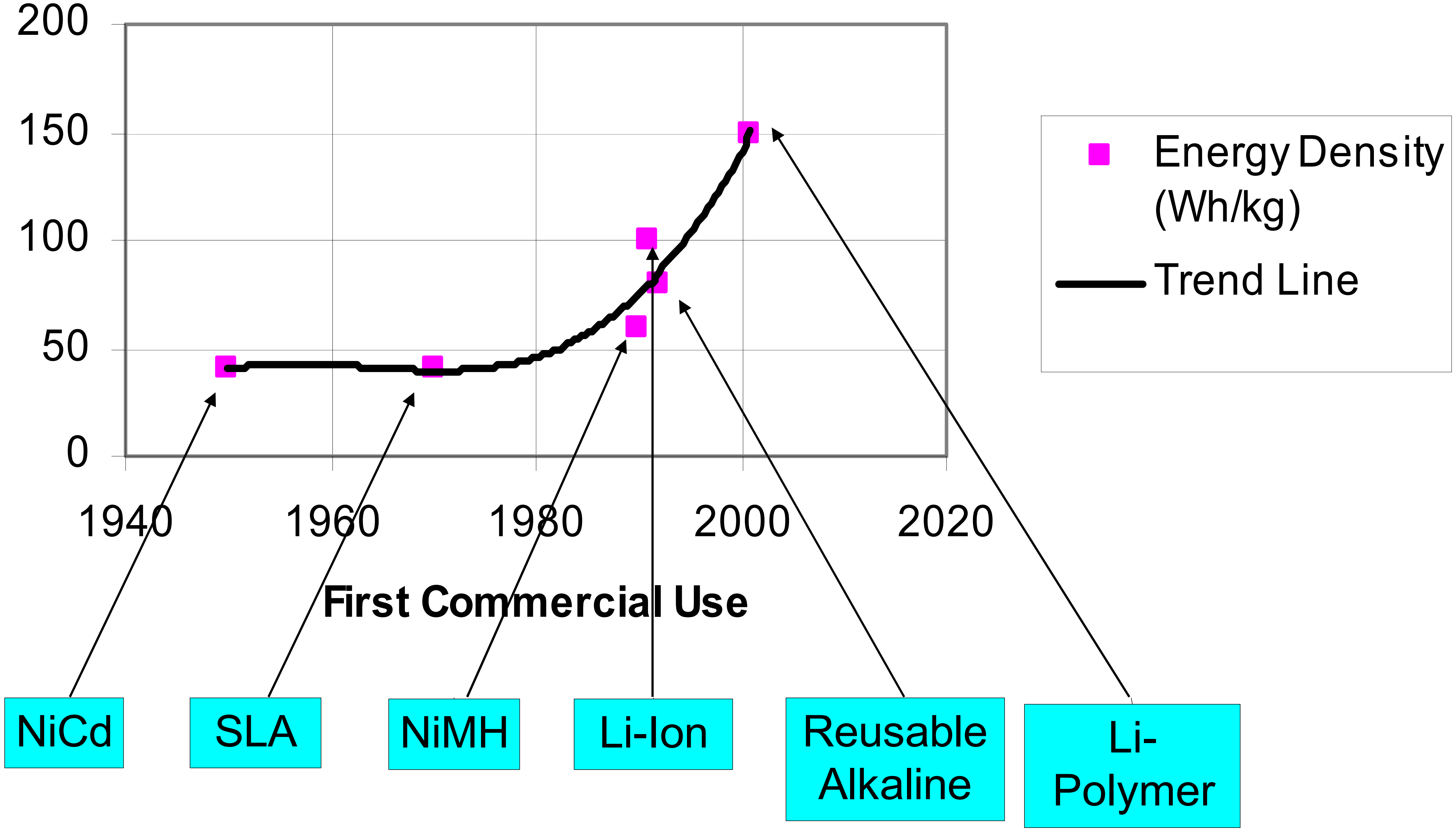
Portability: Battery Limits

- Little change in basic technology
  - store energy using a chemical reaction
- Battery capacity doubles every 10 years
  - Has slowed down
- Energy density/size, safe handling are limiting factor

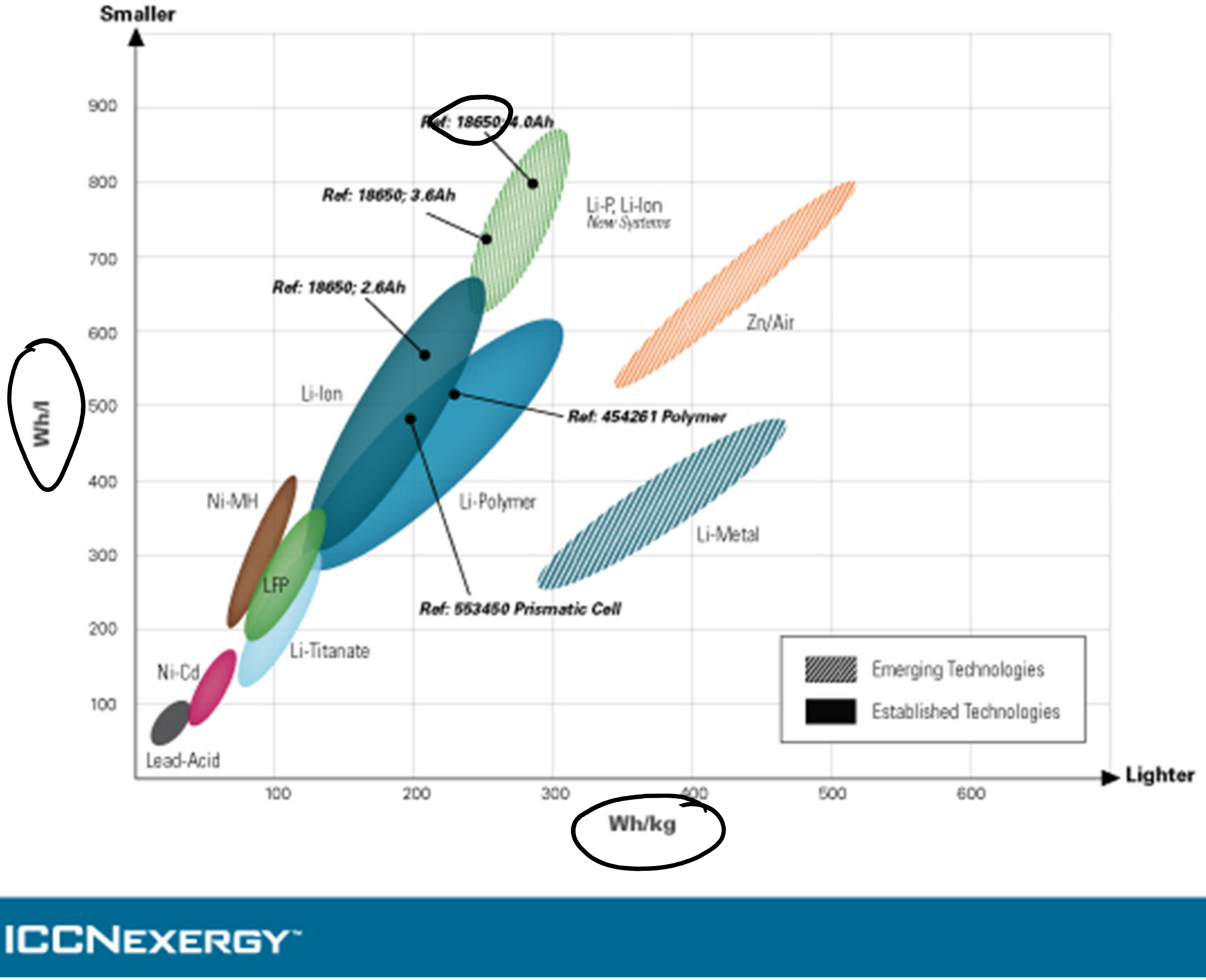
Energy density of material	***KWH/kg***
Gasoline	14
Lead-Acid	0.04
Li polymer	0.15



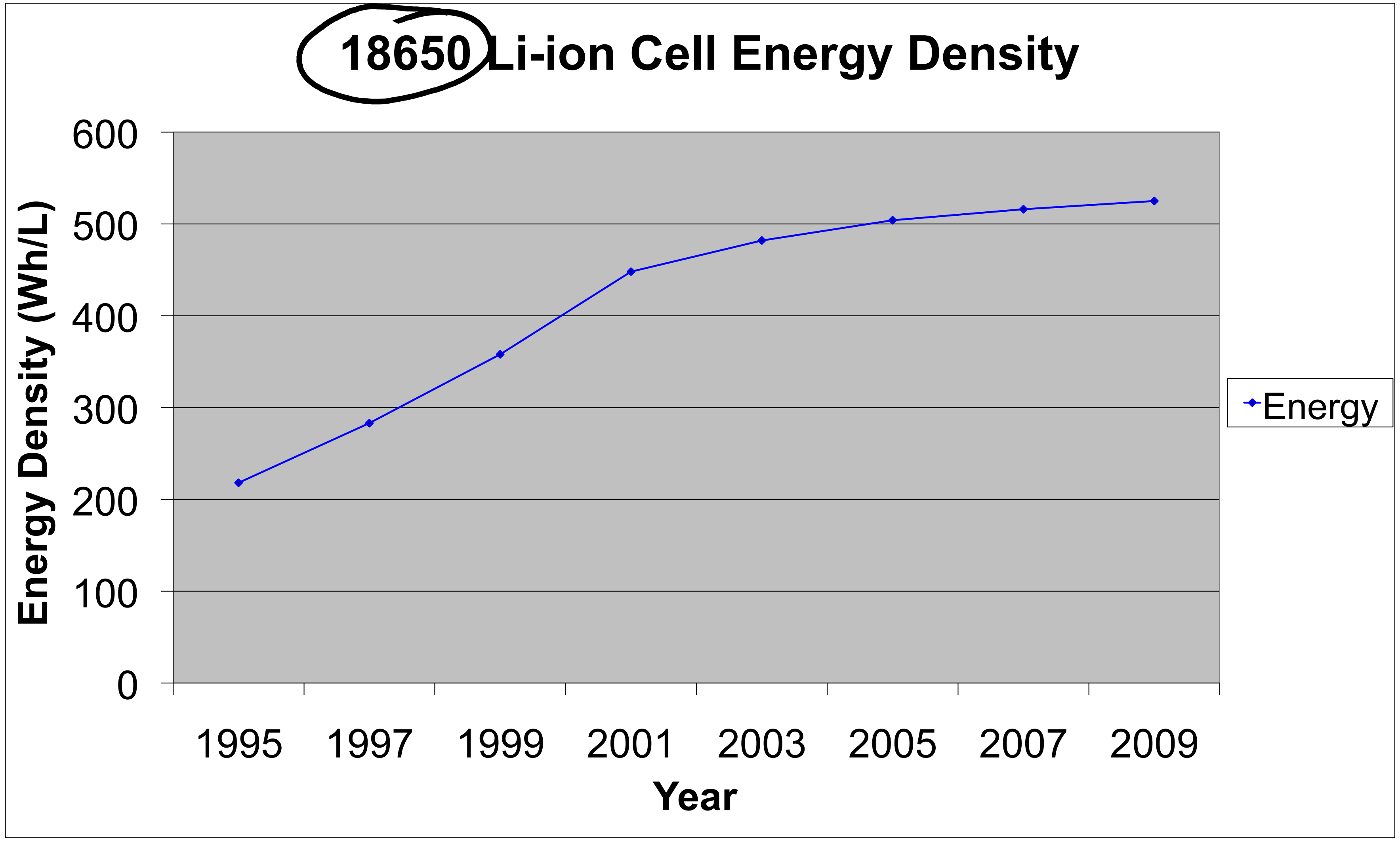
Battery Progress



Comparison of Energy Densities for Various Battery Chemistries



Battery Technology Saturating



Battery capacity naturally plateaus as systems develop

[Courtesy: M. Doyle, Dupont]