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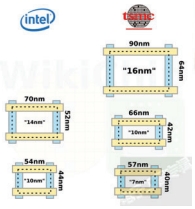
EE241B : Advanced Digital Circuits

Lecture 2 – Scaling Trends

Borivoje Nikolić

Apple, Huawei Use TSMC, But Their 7nm SoCs Are Different. When talking about the most advanced semiconductor manufacturing processes, it seems that most of the SoCs in 2019 can be collectively classified as 7nm. But not all 7nm is equal.

EE Times, January 22, 2020.



Announcements

- Sign up for Piazza if you haven't already

Assigned Reading

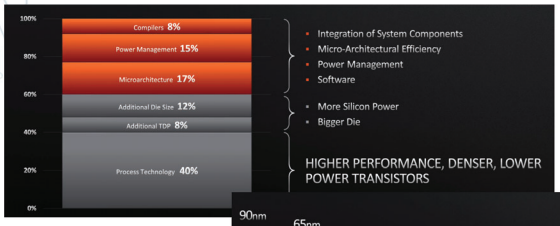
- R.H. Dennard et al, "Design of ion-implanted MOSFET's with very small physical dimensions" IEEE Journal of Solid-State Circuits, April 1974.
  - Just the scaling principles
- C.G. Sodini, P.-K. Ko, J.L. Moll, "The effect of high fields on MOS device and circuit performance," IEEE Trans. on Electron Devices, vol. 31, no. 10, pp. 1386 - 1393, Oct. 1984.
- K.-Y. Toh, P.-K. Ko, R.G. Meyer, "An engineering model for short-channel MOS devices" IEEE Journal of Solid-State Circuits, vol. 23, no. 4, pp. 950-958, Aug. 1988.
- T. Sakurai, A.R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," IEEE Journal of Solid-State Circuits, vol. 25, no. 2, pp. 584 - 594, April 1990.

Outline

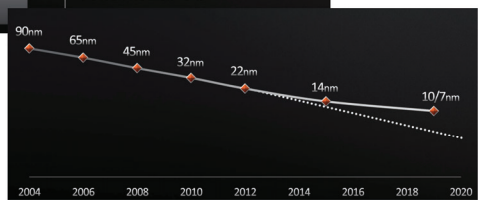
- Scaling issues
- Technology scaling trends
- Features of modern technologies
  - Lithography
  - Process technologies

Trends and Challenges in Digital Integrated Circuit Design

Putting Scaling in Perspective

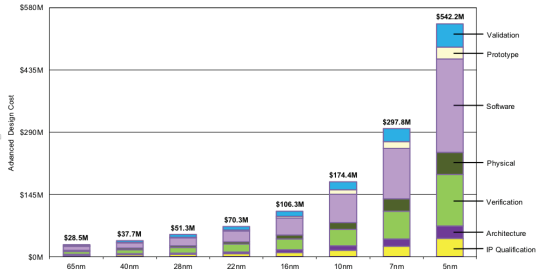


Performance gains over the past decade



Lisa Su, HotChips'19 keynote

Cost Of Developing New Products



- These are non-recurring (NRE) costs, need to be amortized over the lifetime of a product
- We will attempt to dismantle this…

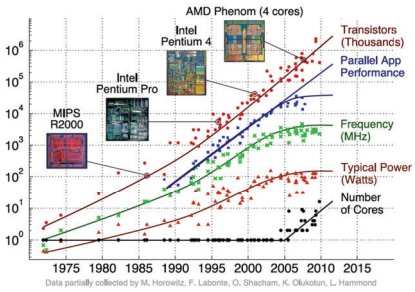
Major Roadblocks

1. Managing complexity
   How to design a 10 billion (100 billion) transistor chip?
   And what to use all these transistors for?
2. Cost of integrated circuits is increasing
   It takes >>$10M to design a chip
   Mask costs are many $M in 16nm technology
3. Power as a limiting factor
   End of frequency scaling
   Dealing with power, leakages
4. Robustness issues
   Variations, SRAM, memory, soft errors, signal integrity
5. The interconnect problem

Part 1: Technology

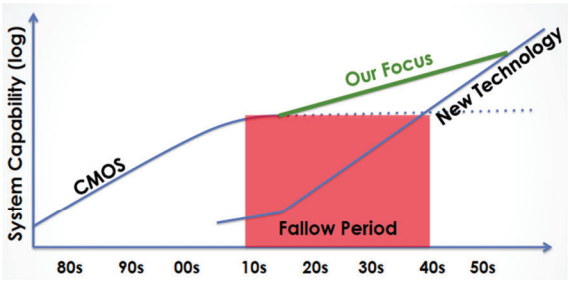
1.A Scaling Trends

Power and Performance Trends



- What do we do next?

What Should We Do?



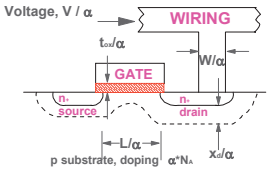
[Graph from "Advancing Computers without Technology Progress", Hill, Kozyrakis, et al., DARPA ISAT 2012]

1.B Scaling Issues

Key Points

- Technology scaling (Moore's law) is slowing down
  - But logic and memory are continuing to scale, possibly at different pace
  - We anyway can't power up all transistors we can put on a chip
- Dennard scaling has ended >10 years ago
  - We cover it for understanding of current issues
- There are many technology flavors available at the moment
  - We need to know what each one brings to us, so we can choose the right one for your project
    (may have to wait until the end of the class to figure out all options)

CMOS Scaling Rules (Dennard)

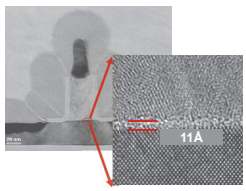


SCALING:

Voltage:	V/α
Oxide:	t_{ox}/α
Wire width:	W/α
Gate length:	L/α
Diffusion:	x_d/α
Substrate:	$\alpha * N_A$

RESULTS:

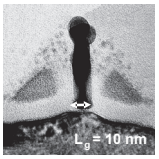
Higher Density:	$\sim\alpha^2$
Higher Speed:	$\sim\alpha$
Power/ckt:	$\sim 1/\alpha^2$
Power Density:	~~Constant~~

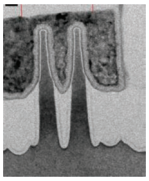


R. H. Dennard *et al.*, *IEEE J. Solid State Circuits*, (1974).

Research vs. Production Devices

10nm device (Intel), circa 2003

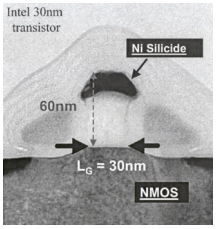




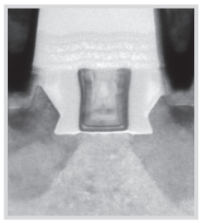
10nm node (Intel), IEDM'2017

CMOS Scaling

- Two 30nm transistors (research and production)



~2000 (research)



~2010 (production)

Transistors are Changing

- From bulk to finFET and FDSOI

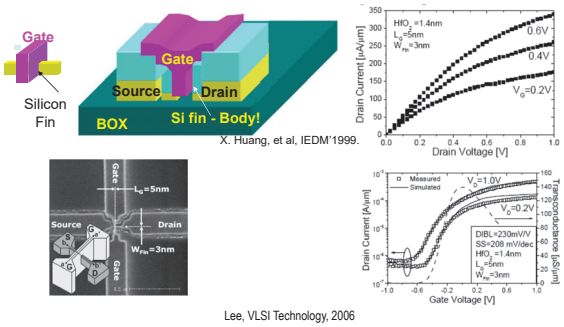
65/55 nm | 45/40 nm | 32/28nm | 22/20nm | 16/14nm | 10nm | 7nm | 5nm

Bulk → SiO_2/SiN Strain, Intel, IEDM'07 HK/MG Strain → Intel, IEDM'09 → TSMC, Samsung

FinFET: Intel, IEDM'12 → Intel, VLSI'14 → Intel, IEDM'17

FDSOI: ST, VLSI'12

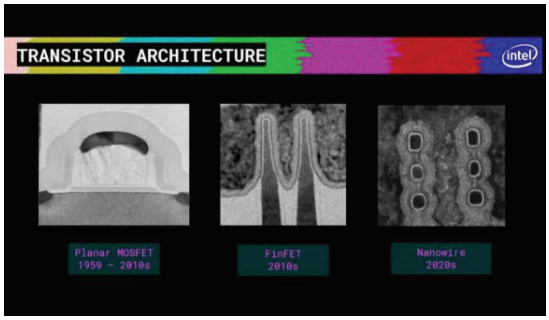
Sub-5nm FinFET



Lee, VLSI Technology, 2006

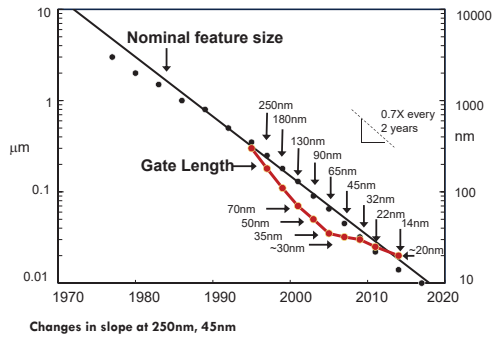
Beyond 5nm

- Gate-all-around transistors/nanowires



J. Keller, EECS Colloquium, UC Berkeley, Sept 2019.

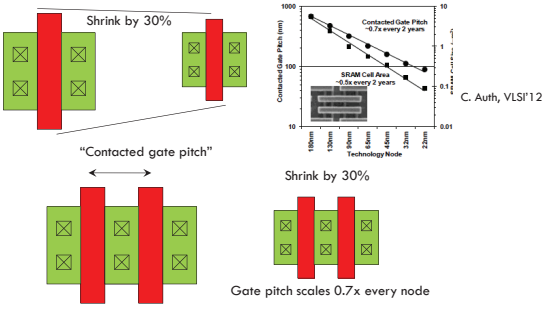
Physical Gate Scaling



Changes in slope at 250nm, 45nm

Source: Intel, IEDM presentations

Transistor Scaling



Intel	45nm	32nm	22nm	14nm	10nm
Contacted gate pitch	160nm	112.5nm	90nm	70nm	54nm

Pitch Scaling

Intel	45nm	32nm	22nm	14nm	10nm
Contacted gate pitch	160nm	112.5nm	90nm	70nm	54nm
Shrink	0.7		0.8	0.78	0.77

- **Clearly not 0.7 anymore…**
- **But (Intel 14nm, Natarajan, IEDM'14)**
  - Fin pitch: 42nm (0.7x shrink)
  - Metal 0: 56nm (-)
  - Metal 1: 70nm (0.78x)
  - Metal 2: 52nm (0.65x)
- **Intel's metric:**
  - CPP x MXP
  - 0.78 x 0.65 = 0.5!
- **CPP & FP matter more**

Various Technology flavors

- Intel 14nm

	High Speed Logic Transistor		Ultra Low Power Transistor	High Volt. I/O Transistor
Options	(HP)	(SP)	(ULP)	(TG)
Vdd (Volt)	0.7	0.7	0.7	1.5-3.3
Gate Pitch(nm)	70	70	84	Min. 140
Fin Pitch (nm)	42	42	42	42
NMOS/PMOS Idsat/Ioff (mA/um)	1.3/ 1.2 @ 0.7 V, 100 nA/um	.85 / .72 @ 0.7 V, 1 nA/um	.50 / .32 @ 0.7 V 15 pA/um	1.15/1.11 @ 1.8 V 10 pA/um

Layer	Pitch	CPU [5]	SoC
Gate	70 nm	Gate	Gate
M0	56 nm	M0	M0
M1	70 nm	M1	M1
Metal 1x	52 nm	M2	M2/3/4/5
Metal 1.1x	56 nm	M3	N/A
Metal 1.5x	80 nm	M4	1-3 layers
Metal 2x	100 nm	M5	1-2 layers
Metal 3x	160 nm	M6-8	1-2 layers
Metal 5x	252 nm	M9/M10	1-2 layers
Metal Top	1080nm	M11	Top Metal
TM1	14 um	TM1	TM1

- Different foundries

Feature	Samsung 14 nm	Intel 14 nm	TSMC 16 nm
Fin pitch (nm)	48	42	48
1/3 fin pitch	16	14	16
Gate length (nm)	~30	~24	~33
Contacted gate pitch (nm)	78	70	90
Minimum metal pitch (nm)	64	52	64
6T SRAM cell area (μm^2)	0.08	0.059	0.074

Source: Tech Insights EETimes

Not All Technologies are Equal

Intel

Node	CPP	MxP	FP
65nm	230	230	
45nm	160	160	
32nm	112.5	112.5	
22nm	90	80	60
14nm	70	52	42
10nm	54	36	34
7nm	37	32	

Samsung

Node	CPP	MxP	FP
45nm	180	140	
32nm	130	100	
28nm	115	90	
20LPE	90	80	60
14LPE	78	64	48
10LPE	68	48	42
7LPP	54	36	27

TSMC

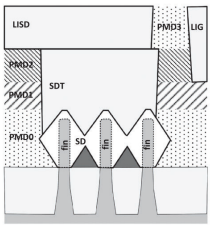
Node	CPP	MxP	FP
45nm	190	140	
40nm	170	130	
28nm	120	90	
20SoC	90	64	
16FF	90	64	48
16FFC	96	64	48
10FF	66	44	36
7FF	57	40	30
5FF	50	28	

- **CPP = Contacted poly pitch**
- **MxP = Minimum metal pitch**
- **FP = Fin pitch**

Source:
A. Wei, TechInsights
IEDM'17, IEDM'19, WikiChip, SemiWiki'20

ASAP7

- Predictive technology kit used in this class
  - None of the above processes, but close

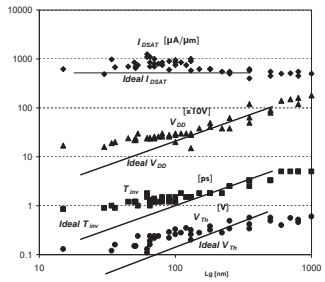


Layer	Lithography	Width/drawn (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active (horizontal)	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54[b]
LIG	EUV	16/16	54
VIA0–VIA3	EUV	18/18	25[a]
M1–M3	EUV	18/18	36
M4 and M5	SADP	24/24	48
VIA4 and VIA5	LELE	24/24	34[a]
M6 and M7	SADP	32/32	64
VIA6 and VIA7	LELE	32/32	45[a]
M8 and M9	SE	40/40	80
VIA8	SE	40/40	57[a]

[a] Corner to corner spacing as drawn.
[b] Horizontal only.

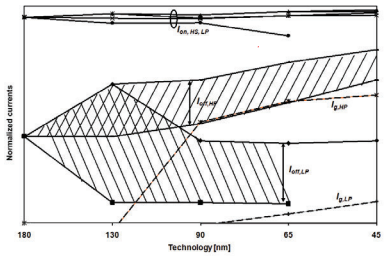
Ideal vs. Real Scaling

- Leakage slows down V_{Th}, V_{DD} scaling

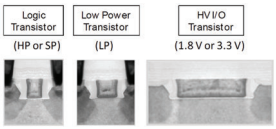


Technology Flavors

- LP keeps drain leakage constant



32nm Technology Flavors (Intel)



Transistor Type	Logic (option for HP or SP)		Low Power	HV I/O (option for 1.8 or 3.3 V)	
	HP	SP	LP	1.8V	3.3V
EOT(nm)	0.95	0.95	0.95	~ 4	~ 7
Vdd (V)	.75/ 1	.75/ 1	0.75/1.2	1.5 /1.8	1.5 /3.3
Pitch(nm)	112.5	112.5	126	min. 338	min. 675
Lgate (nm)	30	34	46	>140	>320
NMOS Idsat (mA/um)	1.53 @ 1 V	1.12 @ 1 V	0.71 @ 1 V	0.68 1.8 V	0.7 3.3 V
PMOS Idsat (mA/um)	1.23 @ 1V	0.87 @ 1 V	0.55 @ 1 V	0.59 1.8 V	.34 @3.3 V
Ioff (nA/um)	100	1	0.03	0.1	<0.01

C.-H. Jan, IEDM'09, P. VanDerVoorn, VLSI Tech'10

5nm Flavors

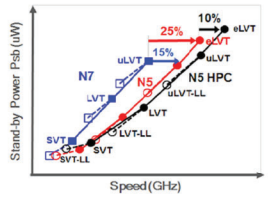
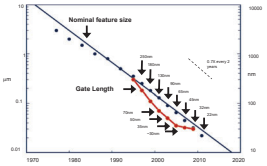
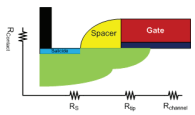


Fig.3 The 5nm also offers a set of critical HPC features. Extremely LVT (eLVT) for 25% faster peak speed over 7nm, and HPC 3-fin standard cell for additional 10% performance.

TSMC, IEDM'19

Lg, R, C scaling

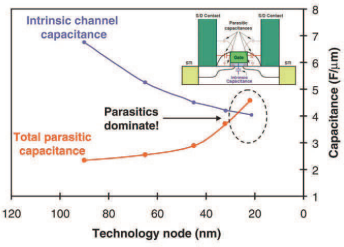




- With scaling L, need to scale up doping - scale junction depth (control leakage) – S/D resistance goes up
- External resistance limits current

$$I_D \approx V_{DS} / (R_{channel} + R_{ext})$$

Parasitic Capacitance Scaling



Reality: Overlap + fringe can be 50% of $C_{channel}$ in 32nm

S. Thompson, *Materials Today*, 2006.