Announcements

- Assignment 4 due next Friday.
- Reading

Outline

- Module 5
  - Dynamic voltage and frequency scaling

5.F Dynamic Voltage Scaling

Power/Energy Optimization Space

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Adaptive Supply Voltages

Exploit Data Dependent Computation Times To Vary the Supply

from (Nielsen94)

(IEEE Transactions on VLSI Systems)

Processors for Portable Devices

• Eliminate performance ↔ energy trade-off

Typical MPEG IDCT Histogram
**Processor Usage Model**

- **Desired Throughput**
  - Compute-intensive and low-latency processes
  - Maximum Processor Speed

**System Optimizations:**
- Maximize Peak Throughput
- Minimize Average Energy/operation

**Common Design Approaches (Fixed VDD)**

- **Compute ASAP:**
  - Excess throughput

**Clock Frequency Reduction:**

- Always high throughput
- Energy/operation remains unchanged...while throughput scaled down with $f_{CLK}$

**Scale $V_{DD}$ with Clock Frequency**

- Constant supply voltage
- $3.3V$
- Reduce $V_{DD}$, slow circuits down.
- $10x$ Energy Reduction

**CMOS Circuits Track Over $V_{DD}$**

- Normalized max. $f_{SW}$ vs $V_{DD}$
- Delay tracks within +/- 10%

**Dynamic Voltage Scaling (DVS)**

- Vary $f_{CLK}$, $V_{DD}$
- Dynamically adapt

- Delivered Throughput vs $f_{CLK}$
- Time

- **Operating System Sets Processor Speed**
  - DVS requires a voltage scheduler (VS).
  - VS predicts workload to estimate CPU cycles.
  - Applications supply completion deadlines.

- $\frac{CPU \ cycles}{\Delta \ time} = F_{DESIRED}$

**Converter Loop Sets $V_{DD}$, $f_{CLK}$**

- Feedback loop sets $V_{DD}$ so that $F_{ERR} \to 0$.
- Ring oscillator delay-matched to CPU critical paths.
- Custom loop implementation → Can optimize $C_{DD}$.

**Design Over Wide Range of Voltages**

- Circuit design constraints. (Functional verification)
- Circuit delay variation. (Timing verification)
- Noise margin reduction. (Power grid, coupling)
- Delay sensitivity. (Local power distribution)

Design verification complexity similar to high-performance processor design @ fixed $V_{DD}$
**Delay Variation & Circuit Constraints**

- Cannot use NMOS pass gates – fails for $V_{DD} < 2V_T$.
- Functional verification only needed at one $V_{DD}$ value.

**Relative Delay Variation**

- Timing verification only needed at min. & max. $V_{DD}$.

**Multiple Path Tracking**

- Four extreme cases of critical paths:
  - Gate
  - Interconnect
  - Diffusion
  - Series

- All vary monotonically with $V_{DD}$.

**Alternative: Error Detection**

- Mismatch between logic and SRAM
- SRAM multiplicative replica
- Tracking with SRAM in Critical Path
- SRAM multiplicative replica

- Max. allowed $|dV_{DD}/dt| ightarrow$ Min. $C_{DD} = 100nF$ (0.6µm)

- Circuits continue to properly operate as $V_{DD}$ changes

**Static CMOS Logic**

- Static CMOS logic.
- Ring oscillator.
- Dynamic logic (& tri-state busses).
- Sense amp (& memory cell).

- $0.6\mu m$ CMOS: $|dV_{DD}/dt| < 200V/\mu s$

- Static CMOS robustly operates with varying $V_{DD}$. 
Ring Oscillator

- Output $f_{\text{CLK}}$ instantaneously adapts to new $V_{\text{DD}}$.

Dynamic Logic

- $0.6\mu m$ CMOS: $|dV_{\text{DD}}/dt| < 20V/\mu s$
  - Cannot gate clock in evaluation state.
  - Tri-state busses fail similarly → Use hold circuit.

Measured System Performance & Energy

- Dynamic operation can increase energy efficiency $> 10x$.

Dynamic Logic

- False logic low: $\Delta V_{\text{DD}} > V_{\text{tp}}$
- Latch-up: $\Delta V_{\text{DD}} > V_{\text{ss}}$

V$_{\text{DC}}$-Hopping

- Two hopping levels are sufficient.

Dithering Between Supply Levels

- Done with switched-capacitor DC-DC converters which efficiently work only at discrete levels

Next Lecture

- Low-power design
  - Clock gating
  - Power gating