EE241B : Advanced Digital Circuits

Lecture 21 – DVS II

Borivoje Nikolić

April 8, NY Times: Computers Already Learn From Us. But Can They Teach Themselves?

Scientists are exploring approaches that would help machines develop their own sort of common sense

Features Pieter Abbeel and Sergey Levine from UC Berkeley

Announcements

- Assignment 4 due next Friday.

- Reading
  - T. Burd, et al, JSSC, Nov 2000.

Outline

- Module 5
  - Dynamic voltage and frequency scaling

5.F Dynamic Voltage Scaling

Power /Energy Optimization Space

	Constant Throughput/Latency		Variable Throughput/Latency
Energy	**Design Time**	**Sleep Mode**	**Run Time**
Active	Logic design Scaled V_{DD} Trans. sizing Multi-V_{DD}	Clock gating	DFS, DVS
Leakage	Stack effects Trans sizing Scaling V_{DD} + Multi-V_{Th}	Sleep T's Multi-V_{DD} Variable V_{Th} + Input control	DVS Variable V_{Th}

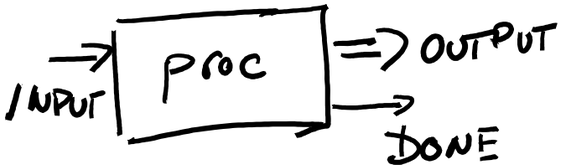
Quiz

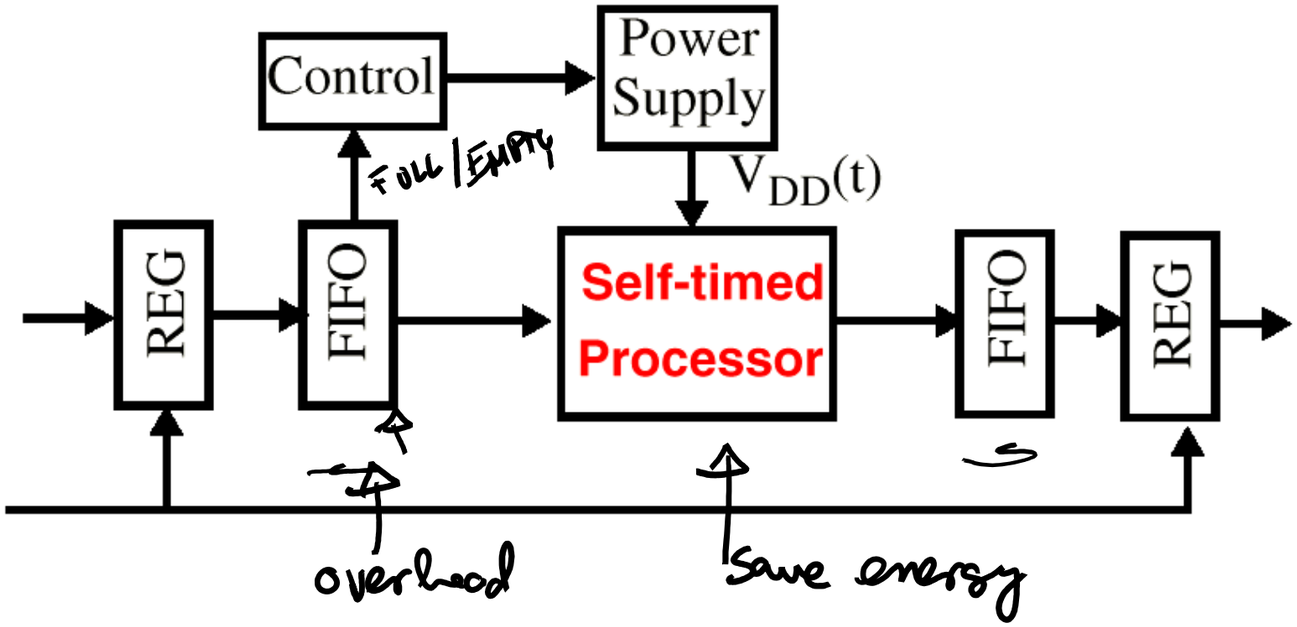
- www.yellkey.com/wonder

Reducing supply by 1% around nominal levels:

- Lowers energy consumption by 1%
- Lowers energy consumption by 2%
- Lowers power by 2%
- Lowers performance by 1%
- Lowers performance by 2%
- Improves energy efficiency
- Lowers energy efficiency

Adaptive Supply Voltages



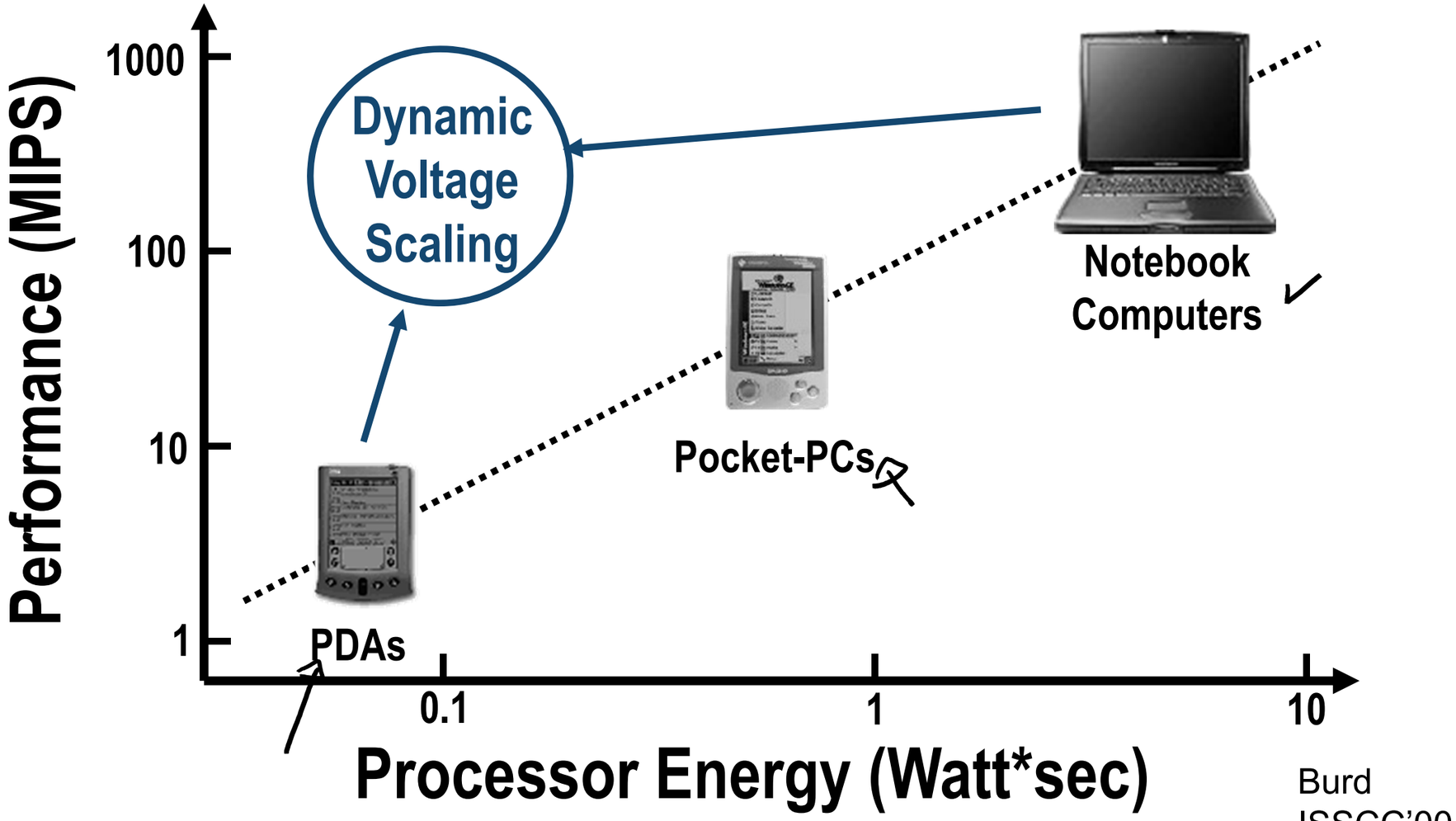


Exploit Data Dependent Computation Times To Vary the Supply

from [Nielsen94]

(*IEEE Transactions on VLSI Systems*)

Processors for Portable Devices



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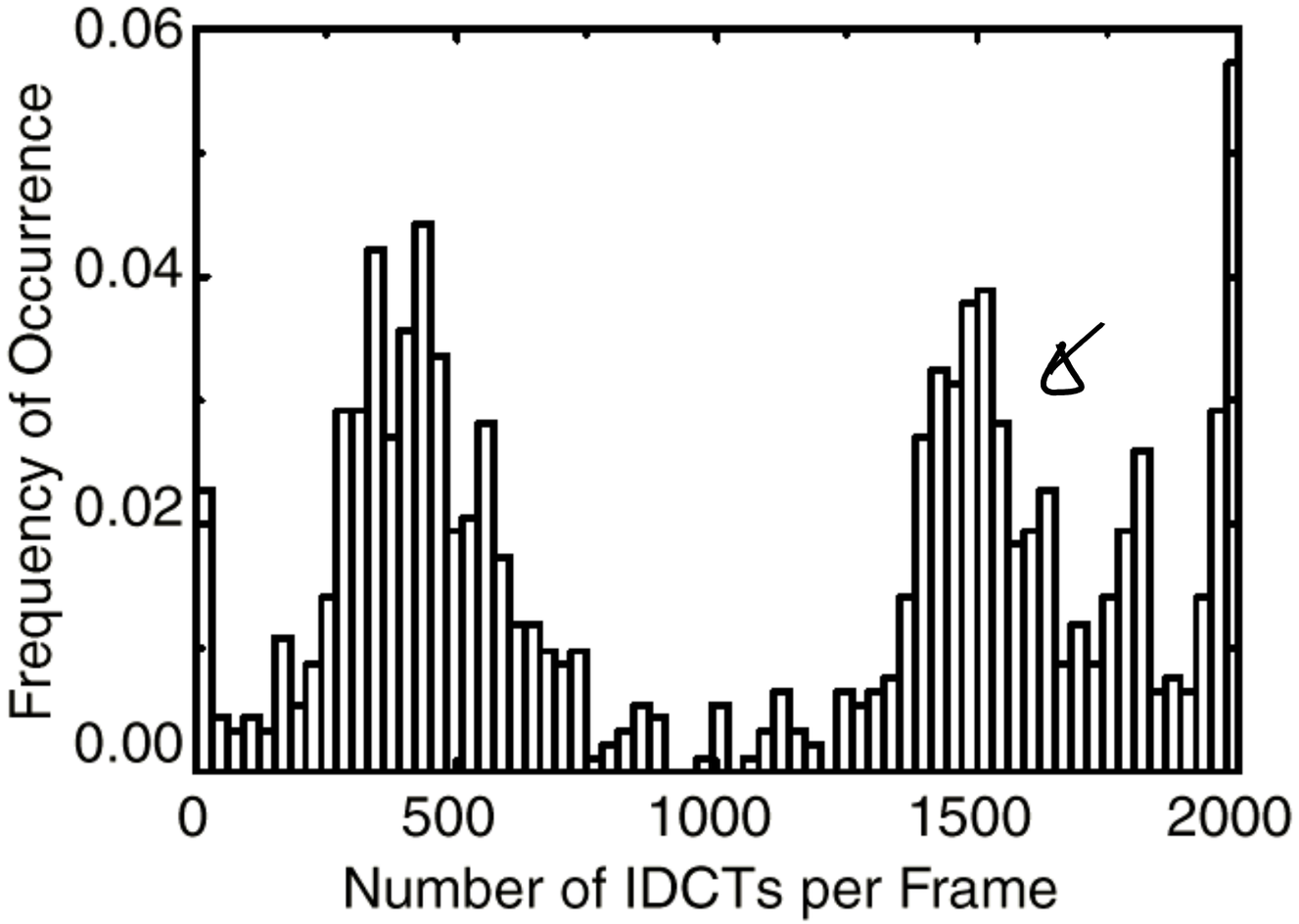
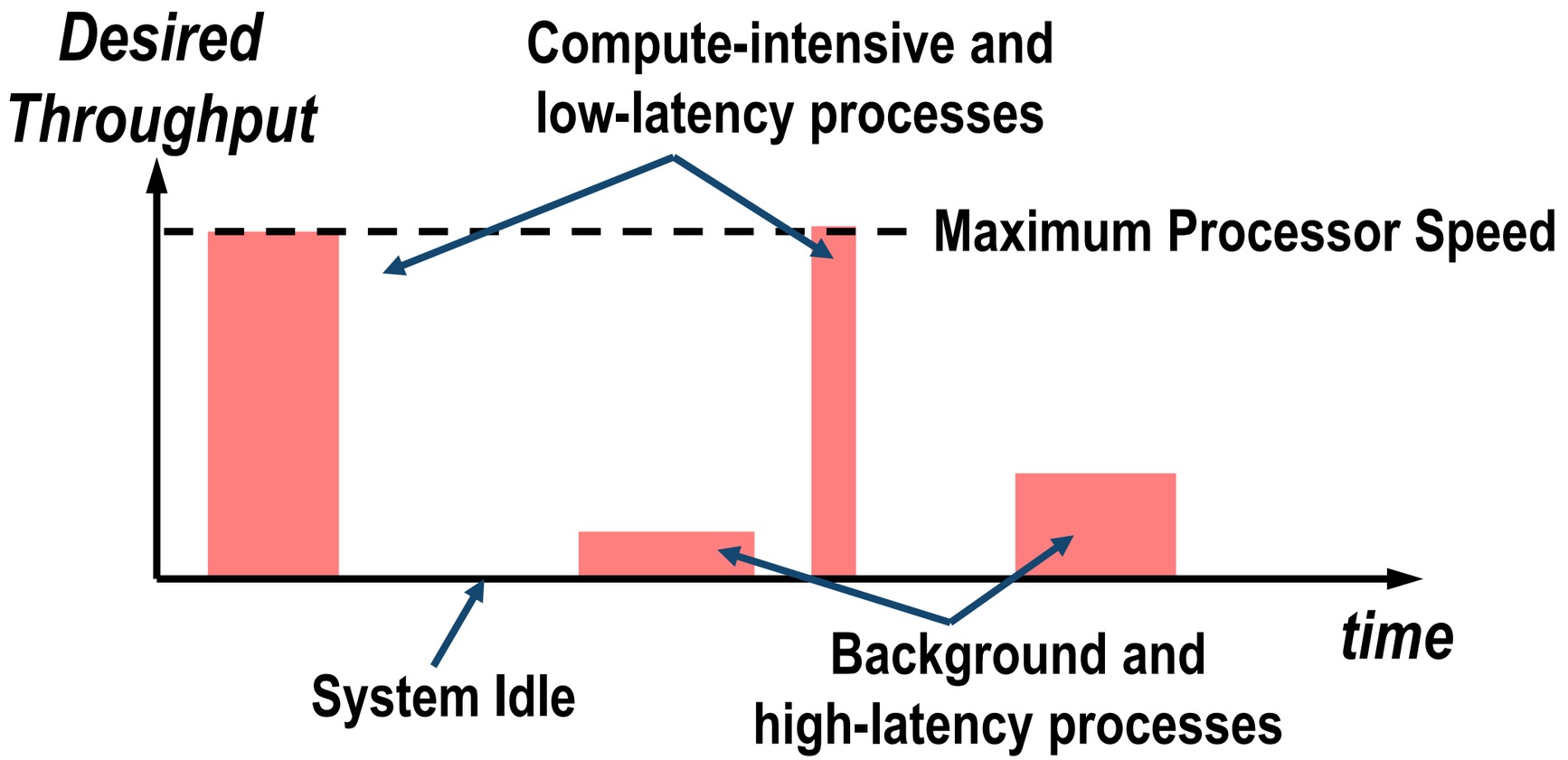
- **Eliminate performance ↔ energy trade-off**

Typical MPEG IDCT Histogram



└ inv. discrete cosine transform

Processor Usage Model



System Optimizations:

- **Maximize Peak Throughput**
- **Minimize Average Energy/operation**

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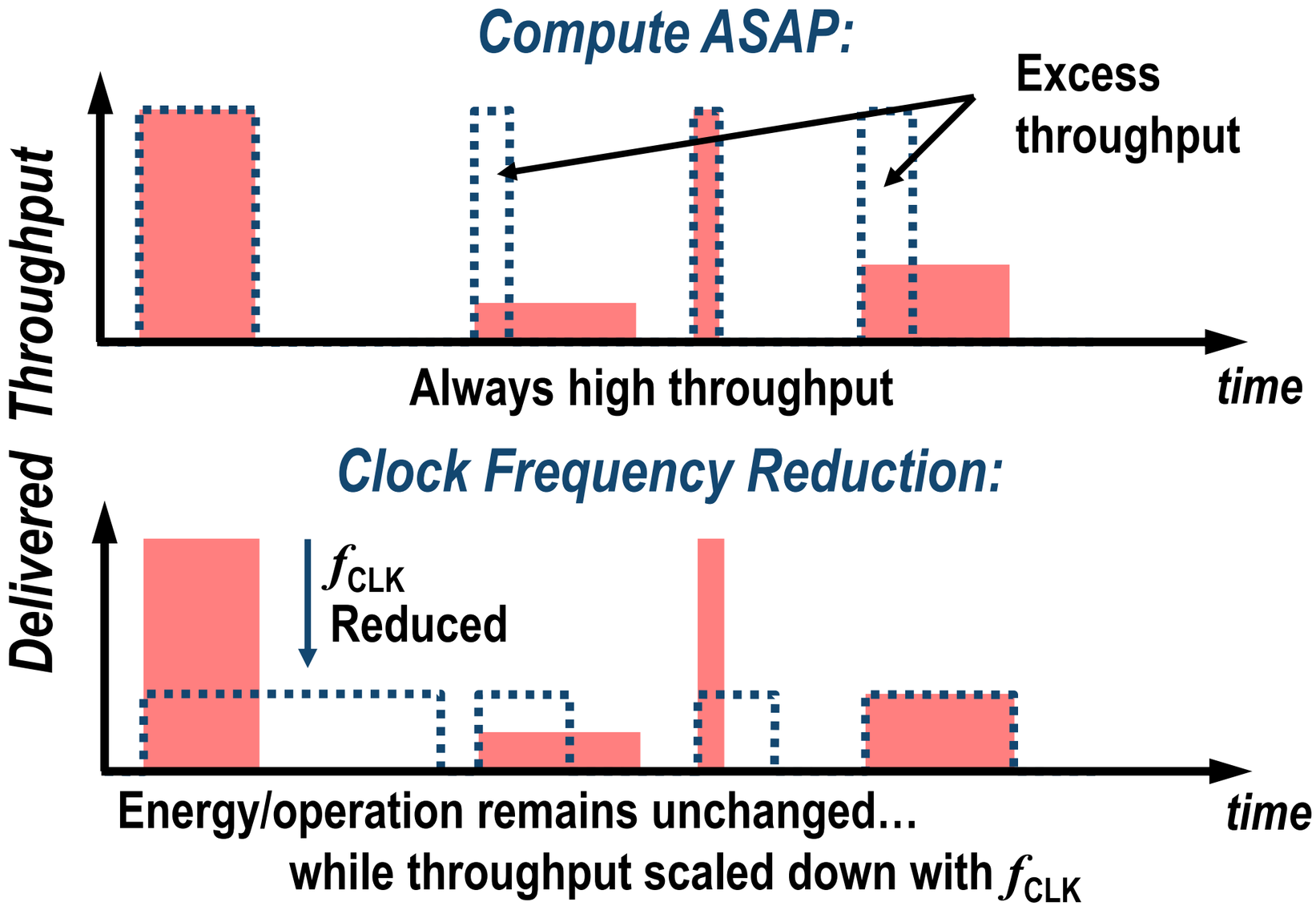
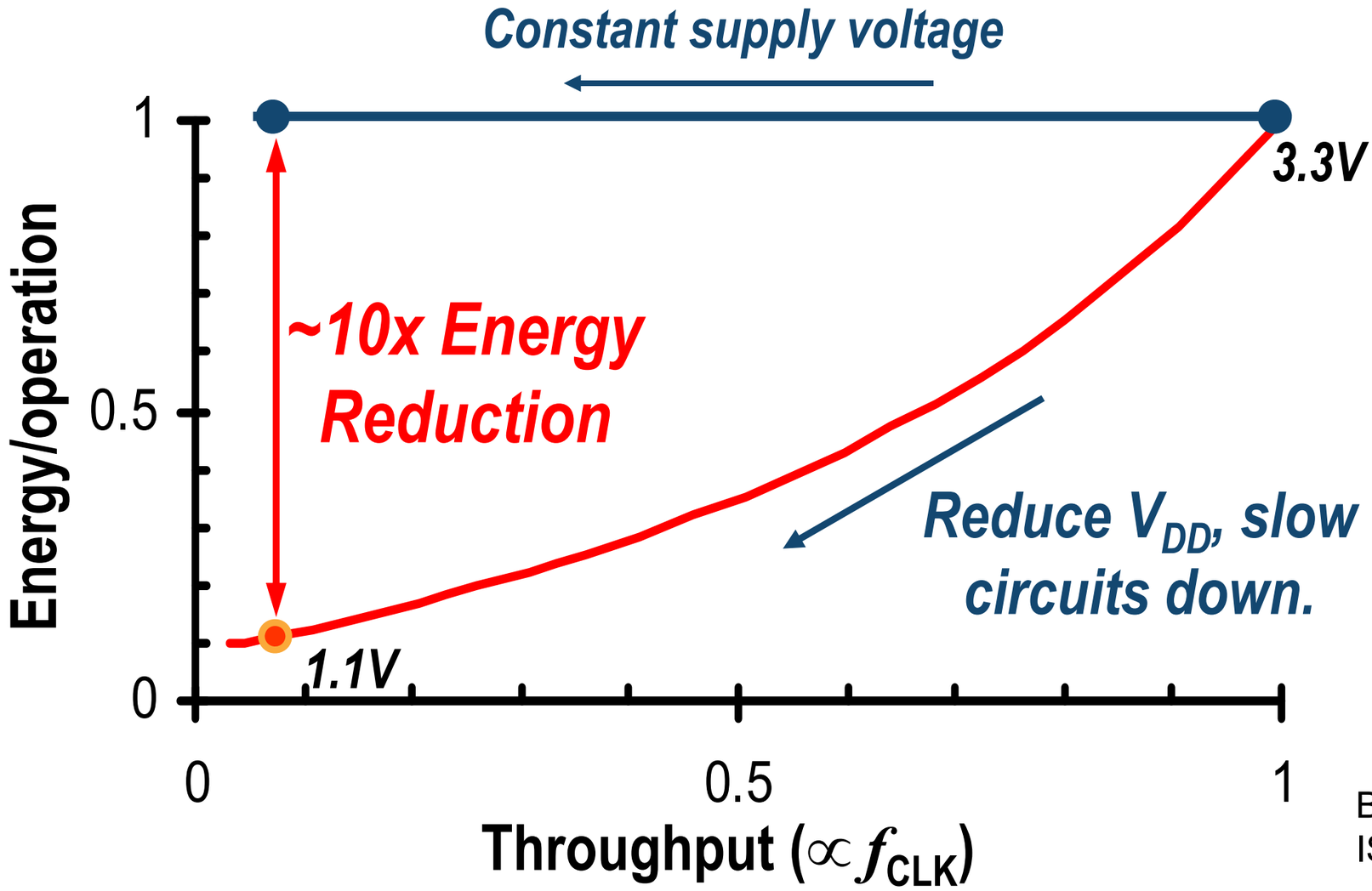
Common Design Approaches (Fixed VDD)



Scale V_{DD} with Clock Frequency



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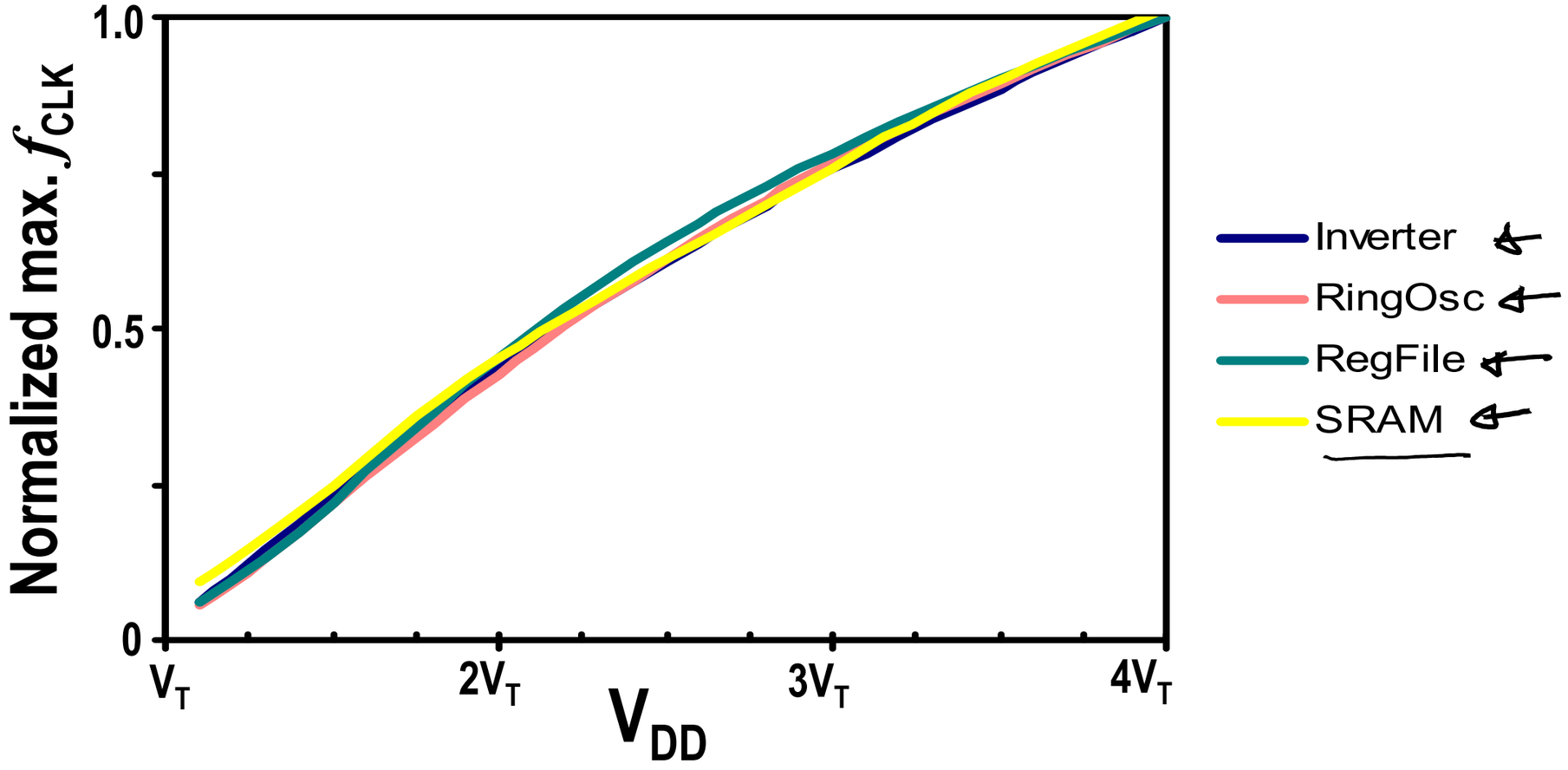
CMOS Circuits Track Over V_{DD}



← Delay tracks within +/- 10% →

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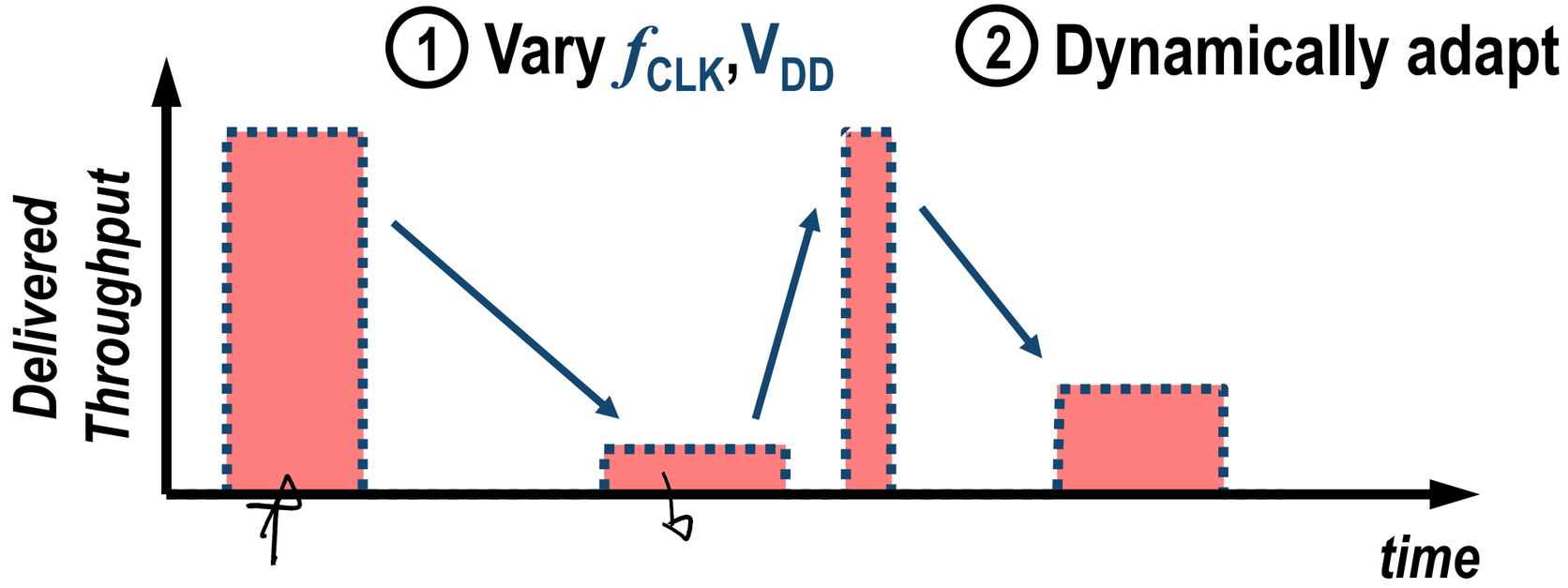
Dynamic Voltage Scaling (DVS)



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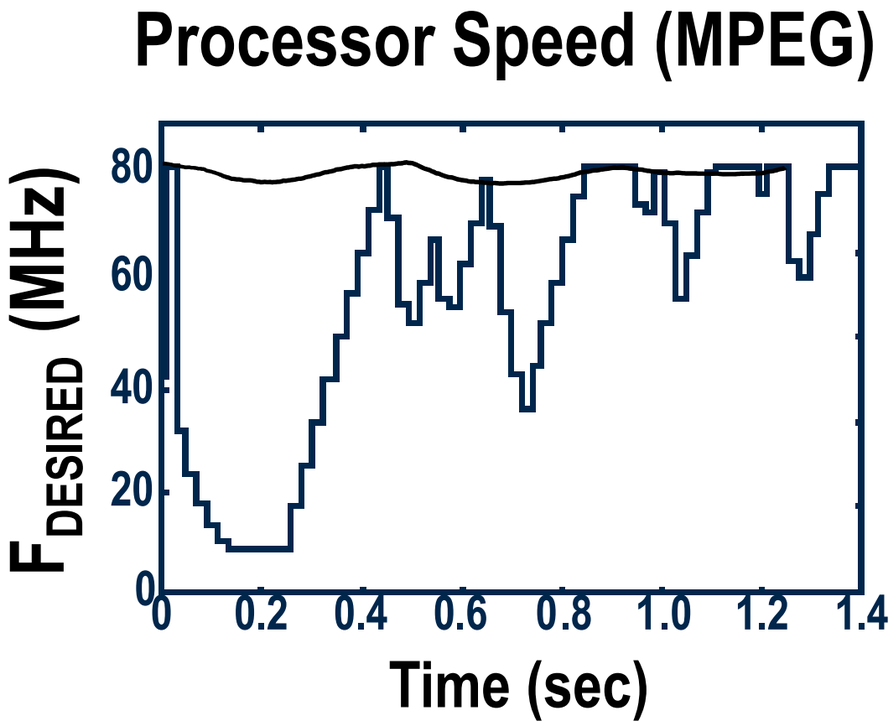
- Dynamically scale energy/operation with throughput.
- Always minimize speed → minimize average energy/operation.
- Extend battery life up to 10x with the exact same hardware!

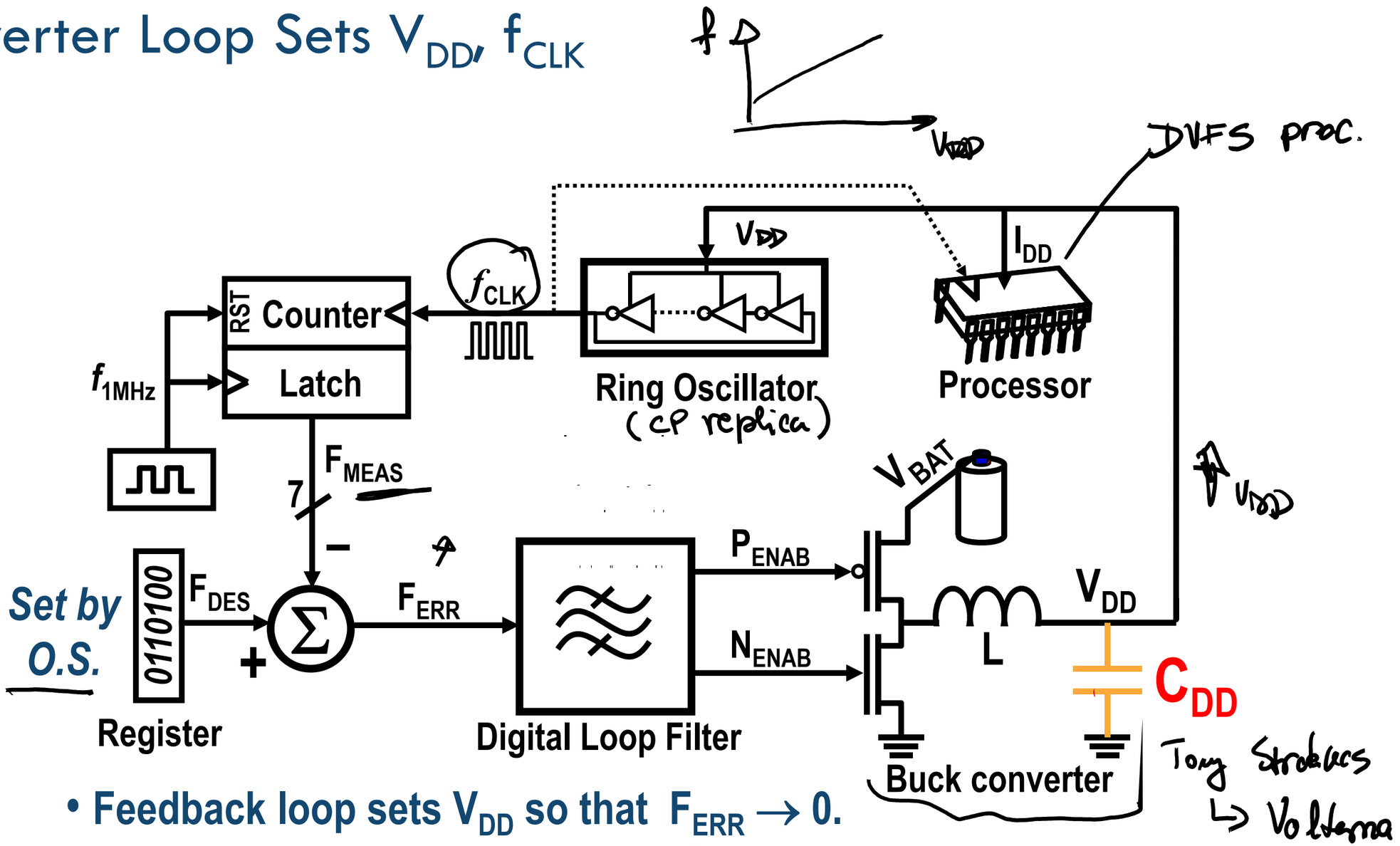
Operating System Sets Processor Speed

- DVS requires a *voltage scheduler* (VS).
- VS predicts workload to estimate CPU cycles.
- Applications supply completion deadlines.

$$\frac{CPU\ cycles}{\Delta\ time} = F_{DESIRED}$$



Converter Loop Sets V_{DD}, f_{CLK}



- Feedback loop sets V_{DD} so that $F_{ERR} \rightarrow 0$.
- Ring oscillator delay-matched to CPU critical paths.
- Custom loop implementation → Can optimize C_{DD}.

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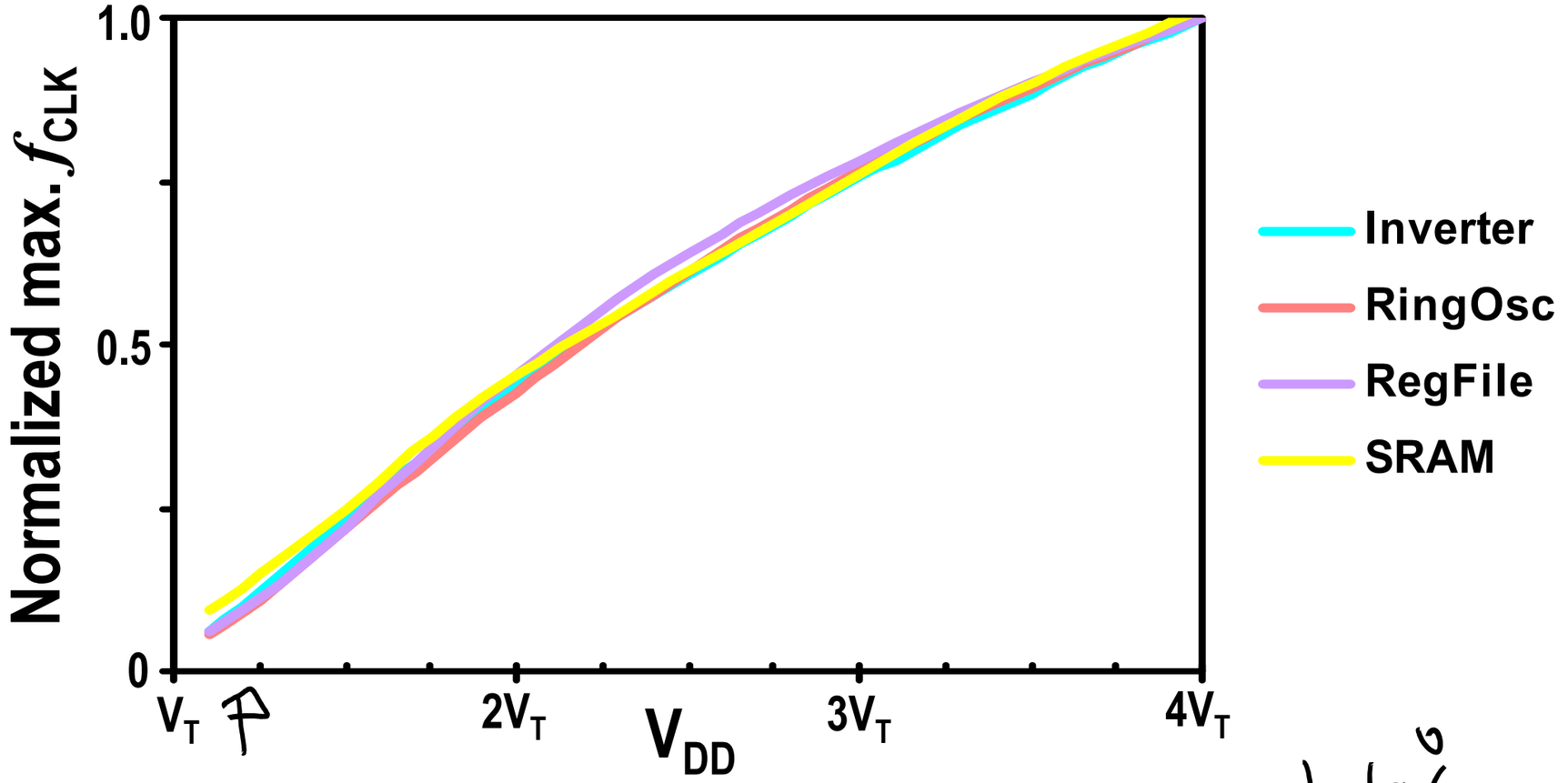
Design Over Wide Range of Voltages

- **Circuit design constraints. (Functional verification)**
- **Circuit delay variation. (Timing verification)**
- **Noise margin reduction. (Power grid, coupling)**
- **Delay sensitivity. (Local power distribution)**

Design verification complexity similar to high-performance processor design @ fixed V_{DD}

Delay Variation & Circuit Constraints



- Cannot use NMOS pass gates – fails for $V_{DD} < 2V_T$.
- Functional verification only needed at one V_{DD} value.

± 10%

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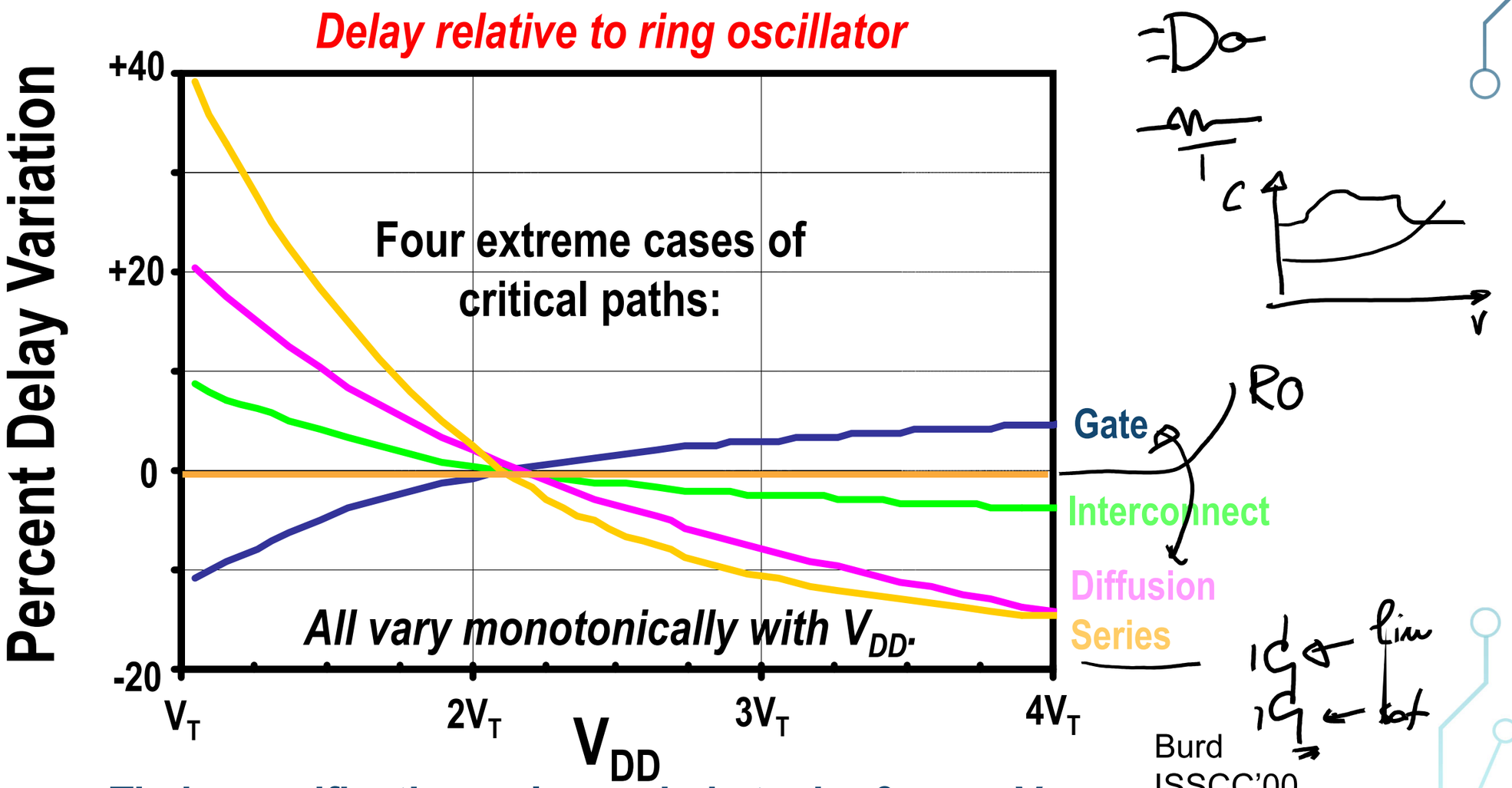
Relative Delay Variation



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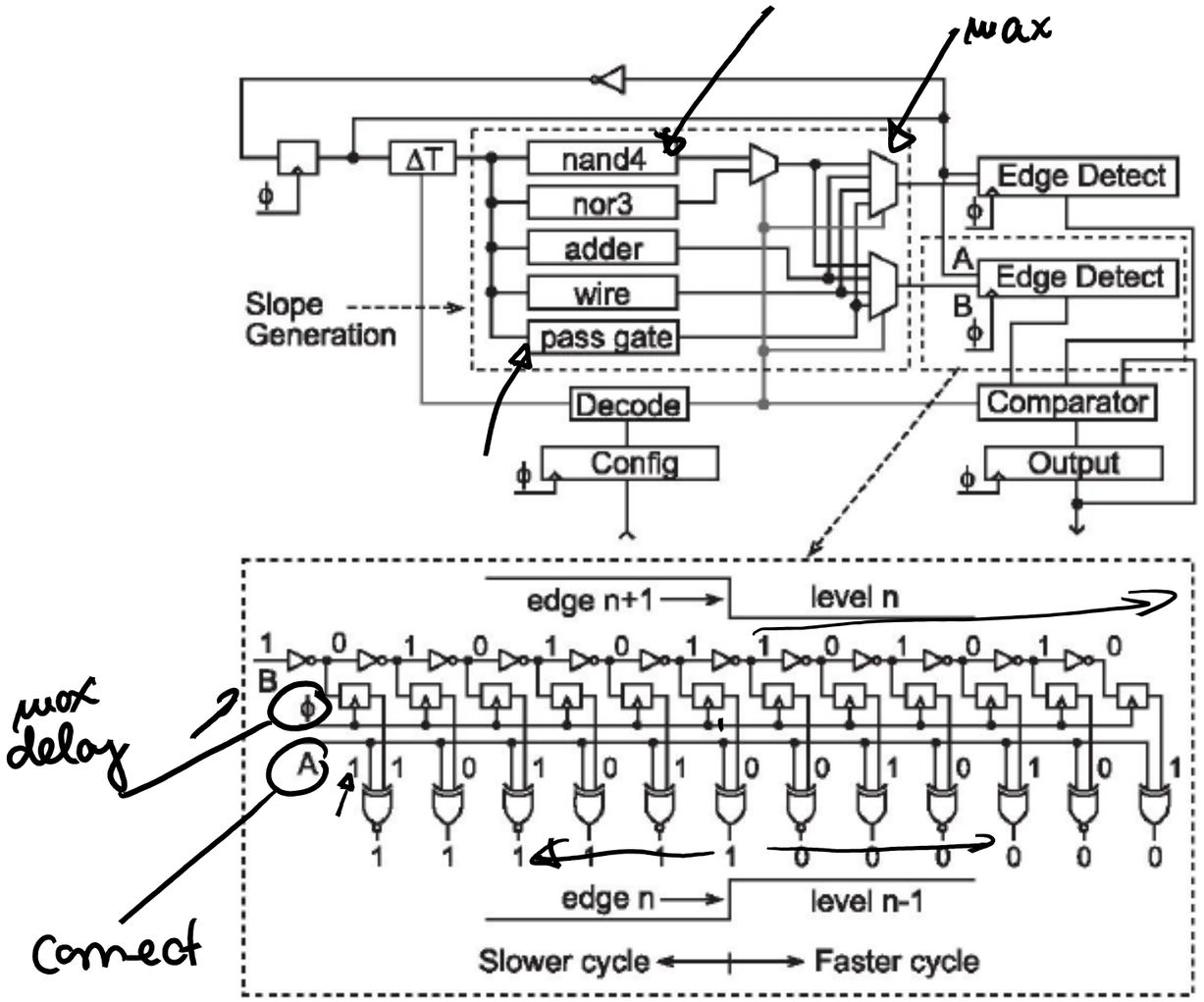
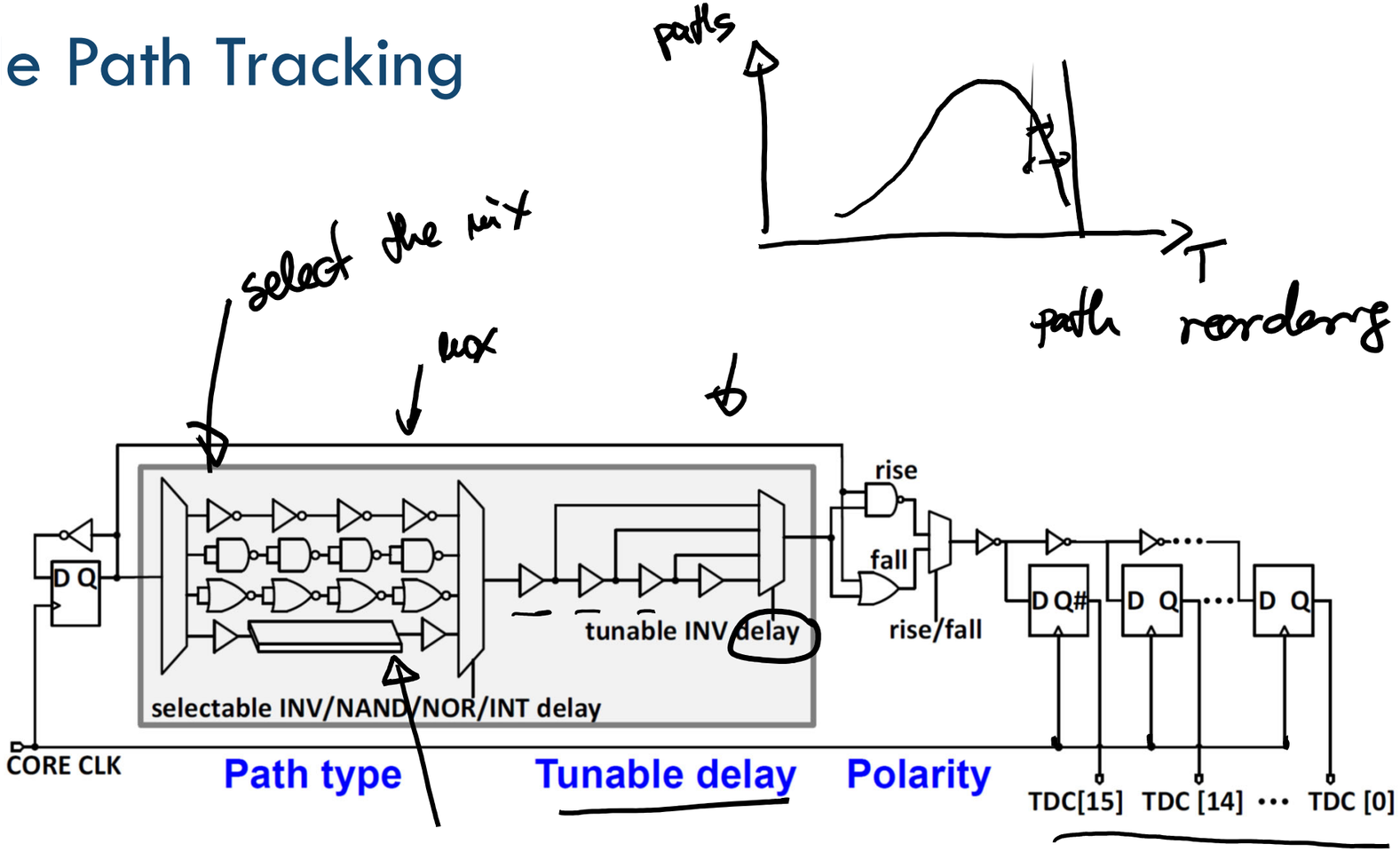
- Timing verification only needed at min. & max. V_{DD}.

Multiple Path Tracking



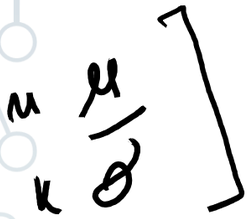
A. Drake, ISSCC'07

Multiple Path Tracking

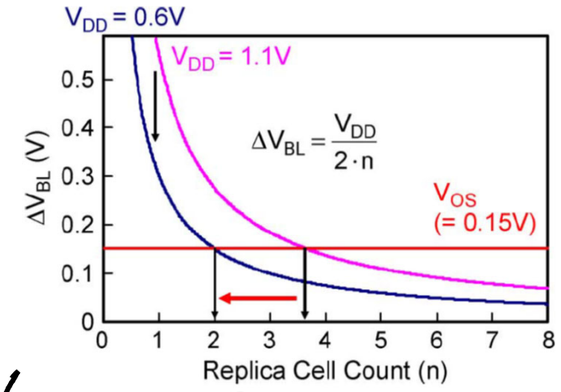


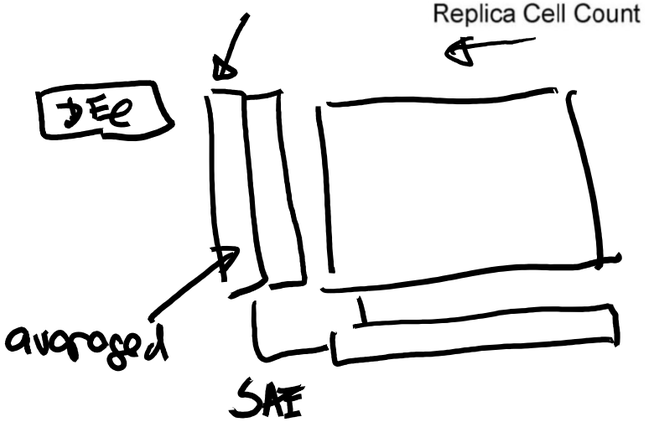
Cho, ISSCC'16

Tracking with SRAM in Critical Path



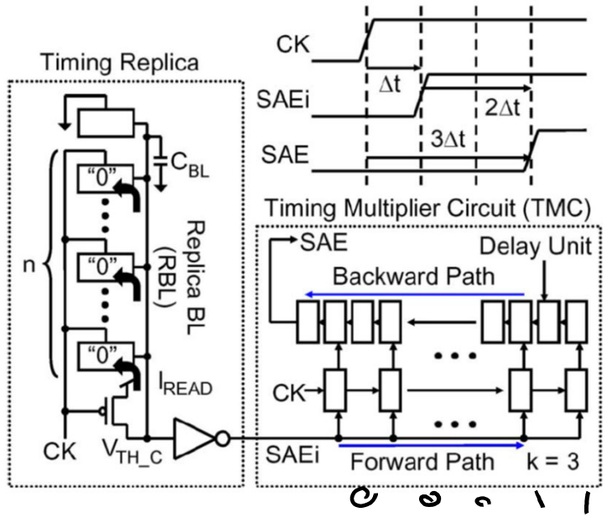
- **Mismatch between logic and SRAM**

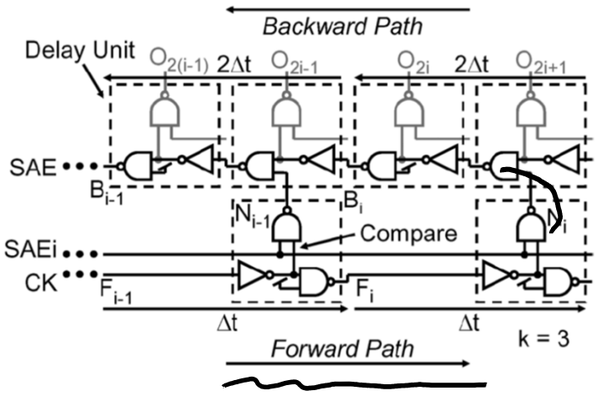




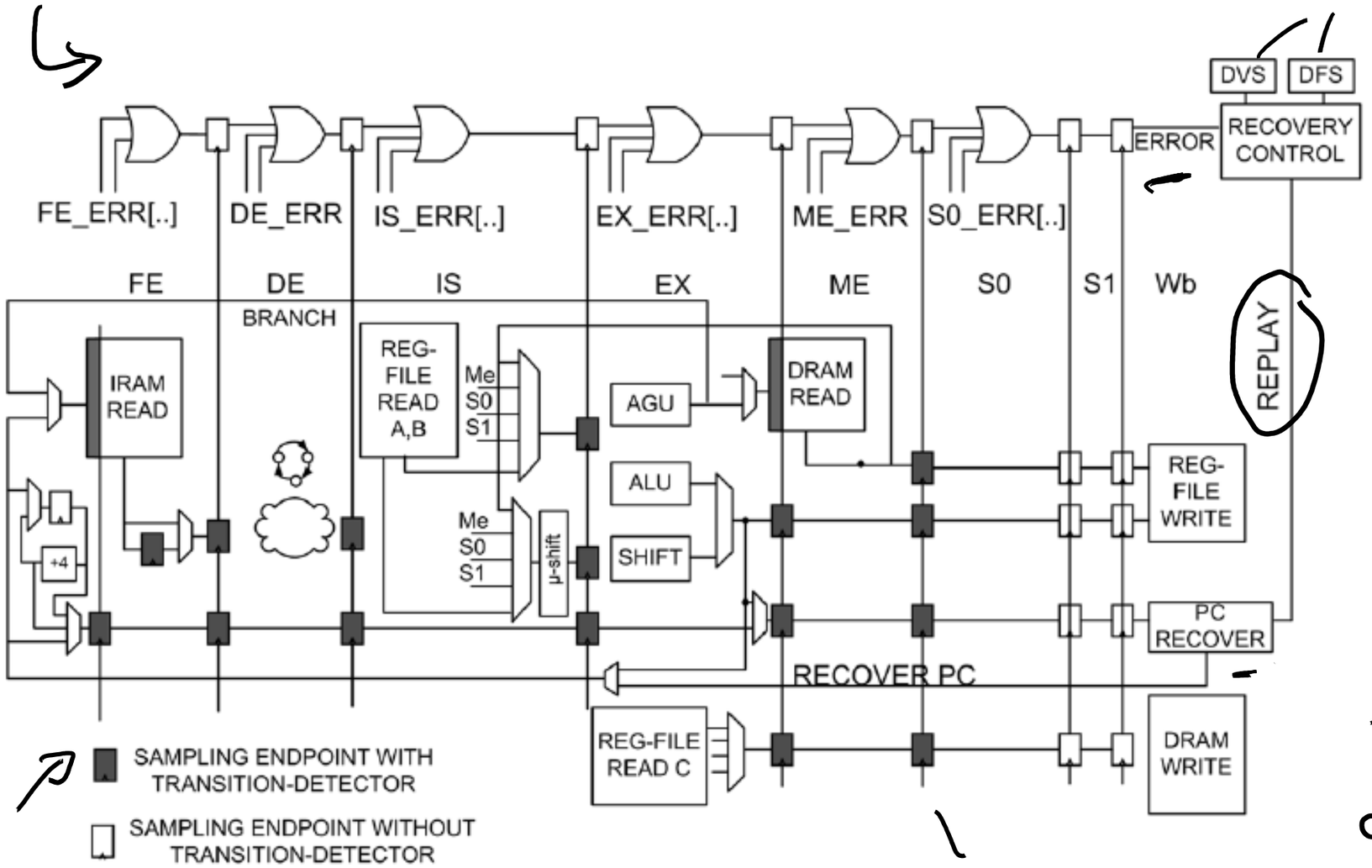
Niki, JSSC'11

- **SRAM multiplictive replica**





Alternative: Error Detection



Bull, ISSCC'2010

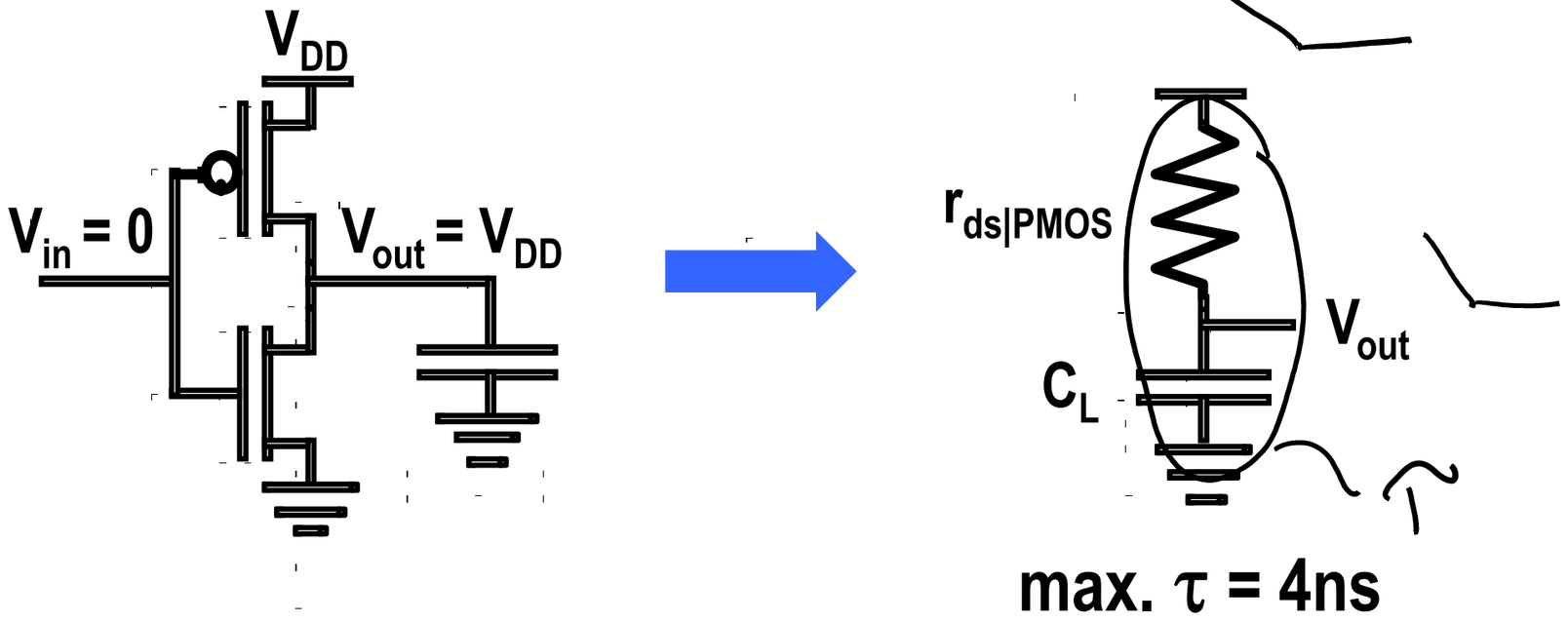
Design for Dynamically Varying VDD

- **Static CMOS logic.**
- **Ring oscillator.**
- **Dynamic logic (& tri-state busses).**
- **Sense amp (& memory cell).**

Max. allowed $|dV_{DD}/dt| \rightarrow$ Min. C_{DD} = 100nF (0.6μm)

Circuits continue to properly operate as V_{DD} changes

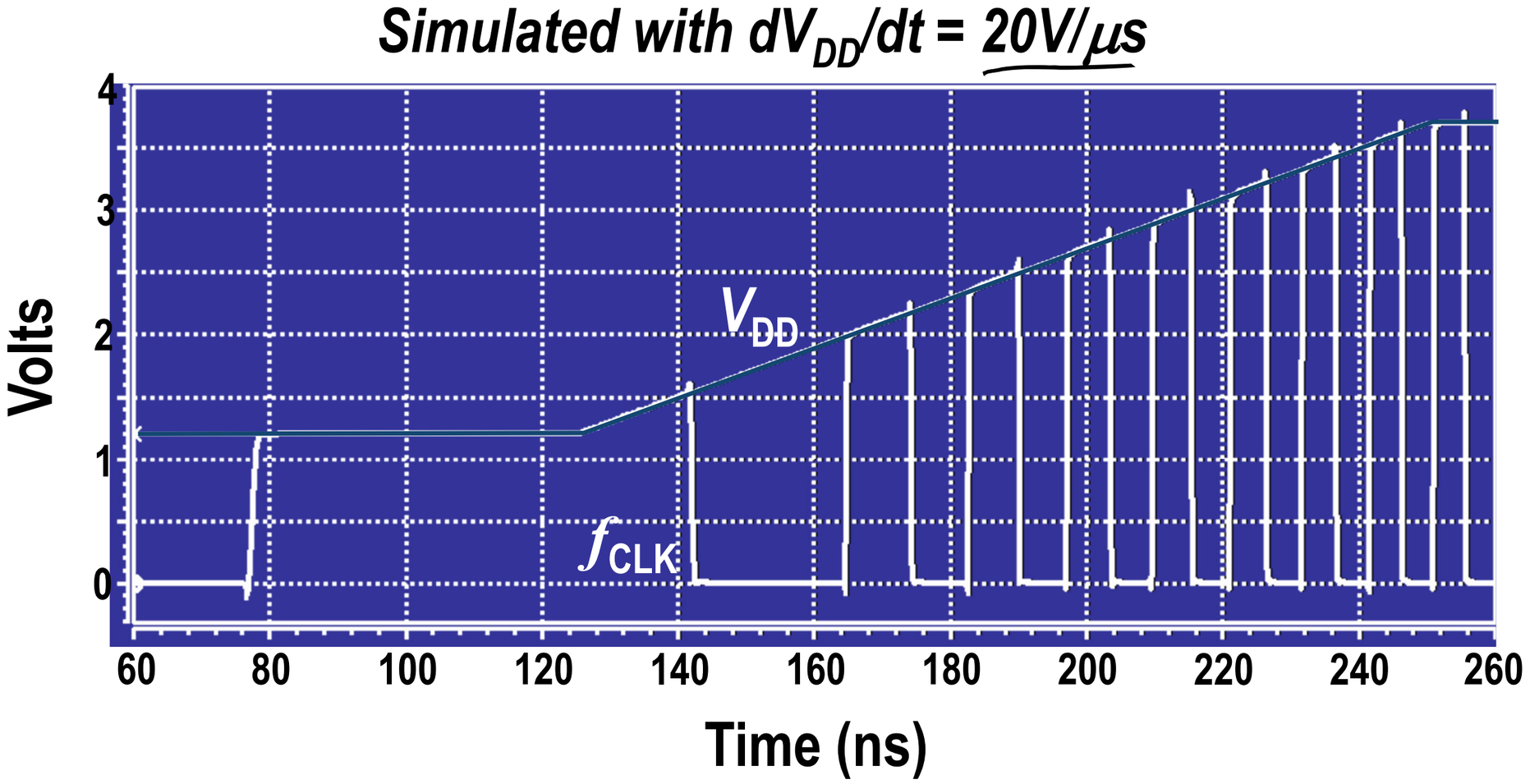
Static CMOS Logic



0.6μm CMOS: $|dV_{DD}/dt| < 200V/\mu s$

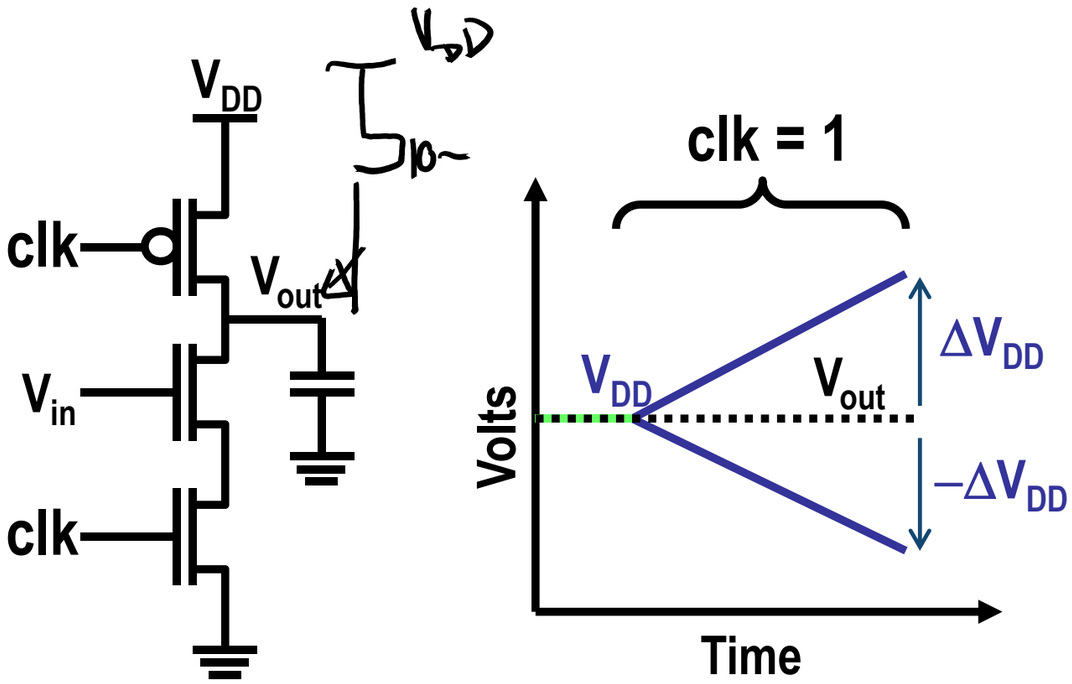
- **Static CMOS robustly operates with varying V_{DD}.**

Ring Oscillator



- Output f_{CLK} instantaneously adapts to new V_{DD}.

Dynamic Logic



Errors

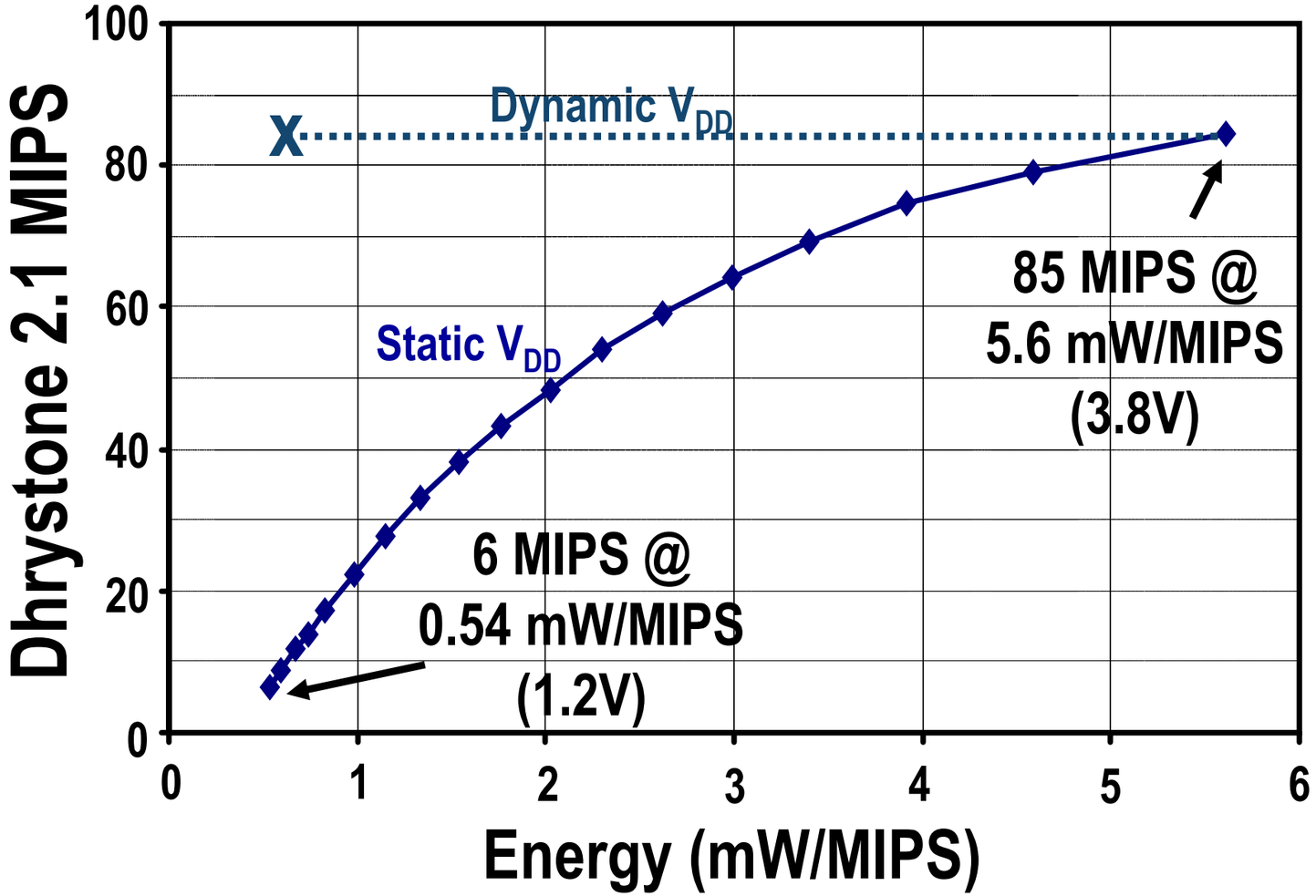
False logic low: $\Delta V_{DD} > V_{TP}$

Latch-up: $\Delta V_{DD} > V_{be}$

0.6μm CMOS: $|dV_{DD}/dt| < 20V/\mu s$

- Cannot gate clock in evaluation state.
- Tri-state busses fail similarly → Use hold circuit.

Measured System Performance & Energy



- **Dynamic operation can increase energy efficiency > 10x.**

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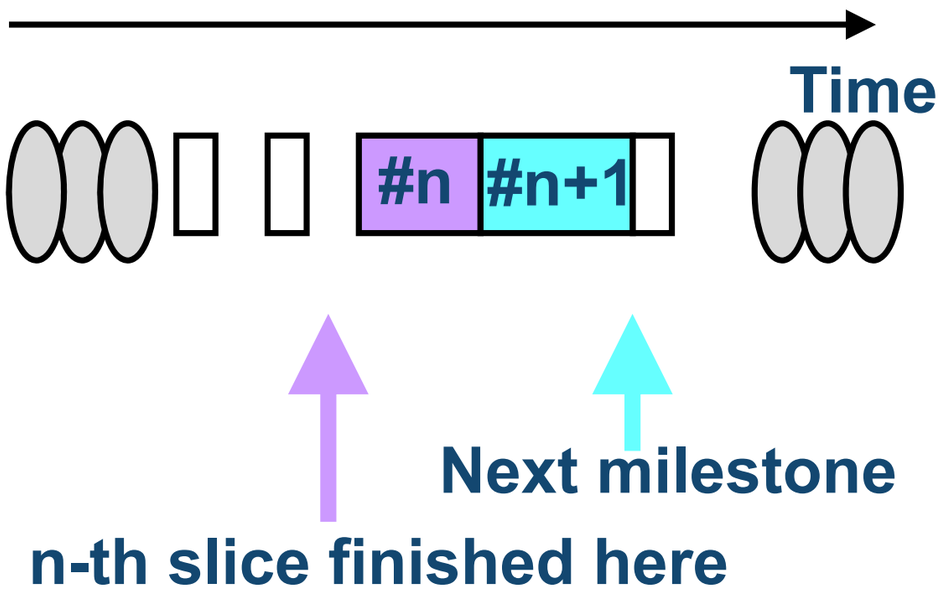
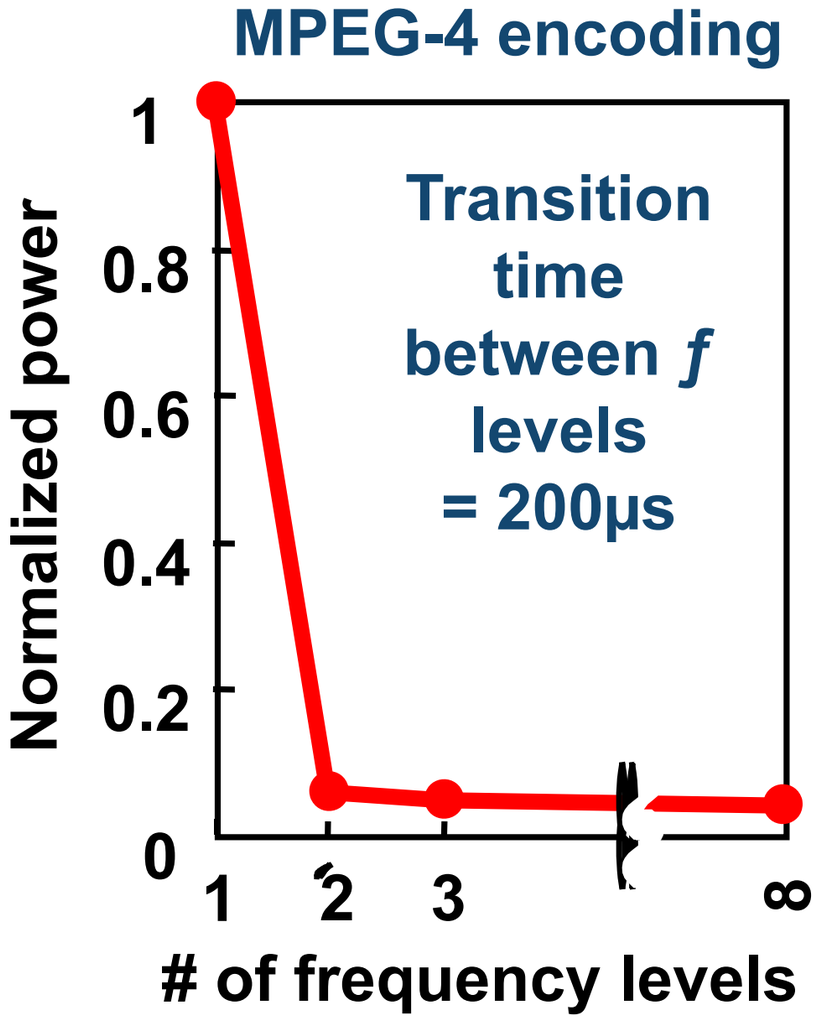
V_{DD}-Hopping

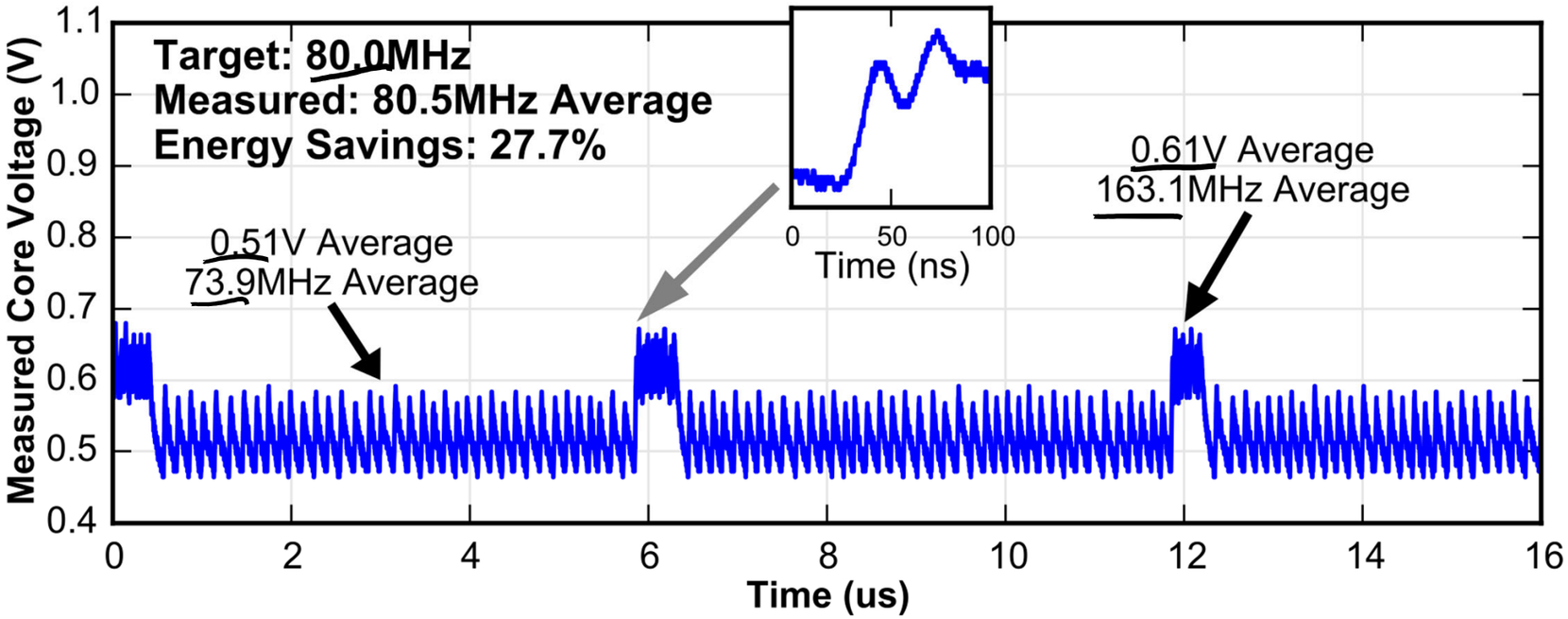




Application slicing and software feedback guarantee real-time operation.

Two hopping levels are sufficient.

Dithering Between Supply Levels



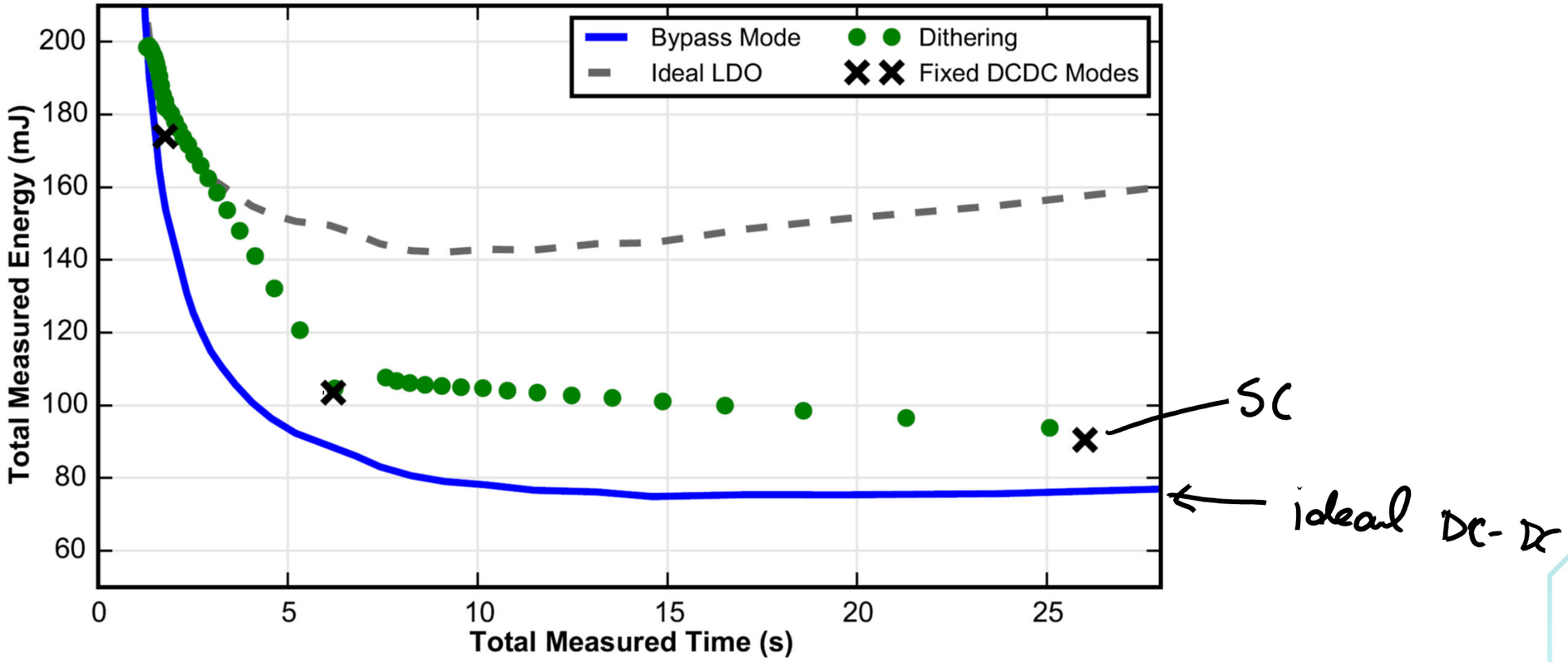
- Done with switched-capacitor DC-DC converters which efficiently work only at discrete levels

Keller et al, ESSCIRC'16

Dithering Between Supply Levels

- Dithering fills in between fixed DC-DC modes

matrix - matrix mult



Keller et al, ESSCIRC'16

Next Lecture

- Low-power design
  - Clock gating
  - Power gating

Low power

2 supply + clk

Thu 4/30

Projects May 4 or 5